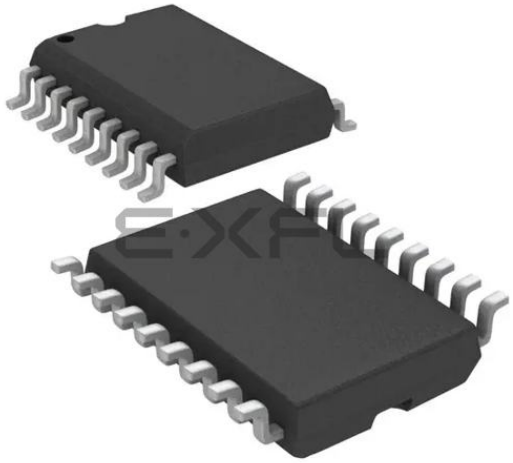

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	PWM, WDT
Number of I/O	13
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00110ssg

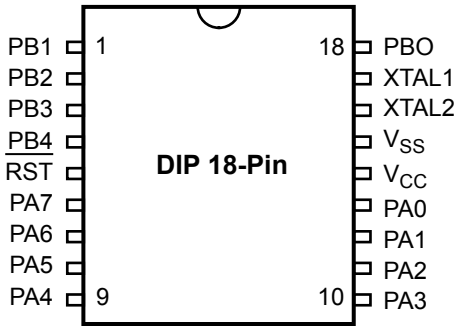

Figure 4. 18-Pin DIP/SOIC Pin Identification

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	Input/Output
5	RESET	Reset	Input
6-9	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Osc. Clock	Output
17	XTAL1	Crystal Osc. Clock	Input
18	PB0	Port B, Pin 0	Input/Output

PIN DESCRIPTION (Continued)

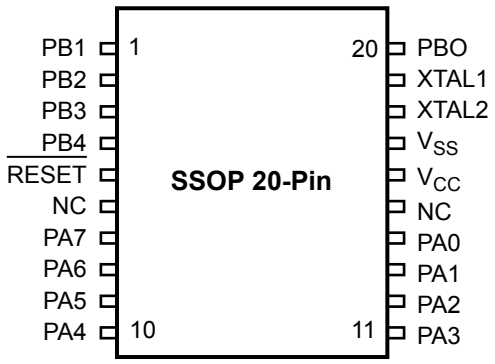

Figure 5. 20-Pin SSOP Pin Identification

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	Input/Output
5	RESET	Reset	Input
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Osc. Clock	Output
19	XTAL1	Crystal Osc. Clock	Input
20	PB0	Port B, Pin 0	Input/Output

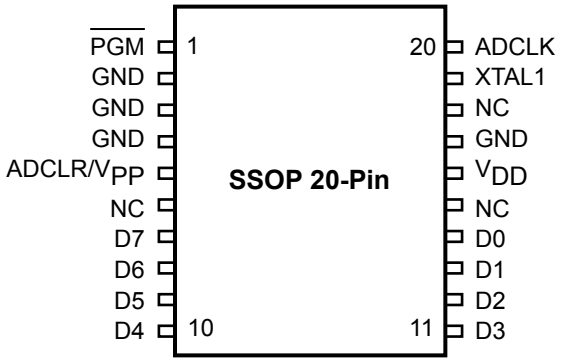

Figure 6. 20-Pin SSOP Pin Identification/EPROM Programming Mode

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Prog Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clk./Prog Volt.	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	Input/Output
11–14	D3–D0	Data 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1MHz Clock	Input
20	ADCLK	Address Clock	Input

AC ELECTRICAL CHARACTERISTICS

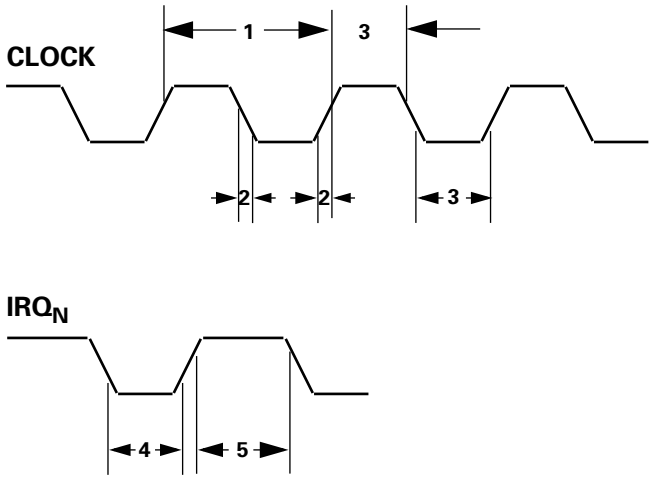

Figure 8. AC Electrical Timing Diagram

Table 3. Additional Timing

				T_A = 0°C to +70°C T_A = –40°C to +105°C @ 10 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.5V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	TrC,TfC	Clock Input Rise and Fall Times	3.5V		15	ns	2
			5.5V		15	ns	2
3	TwC	Input Clock Width	3.5V	50		ns	2
			5.5V	50		ns	2
4	TwIL	Int. Request Input Low Time	3.5V	70		ns	2
			5.5V	70		ns	2
5	TwIH	Int. Request Input High Time	3.5V	5TpC			2
			5.5V	5TpC			2
6	Twsm	STOP Mode Recovery Width Spec.	3.5V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	3.5V		5TpC		
			5.5V		5TpC		

Notes:
1. The V_{DD} voltage specification of 3.5V guarantees 3.5V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

Z8PLUS CORE

The Z8E001 is based on the ZiLOG Z8Plus Core Architecture. This core is capable of addressing up to 64KBytes of program memory and 4KBytes of RAM. Register RAM is accessed as either 8 or 16 bit registers using a combination of 4, 8, and 12 bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions using six addressing modes. See the Z8Plus User's Manual for more information.

RESET

This section describes the Z8E001 reset conditions, reset timing, and register initialization procedures. Reset is generated by the Reset Pin, Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8E001 into a known state. To initialize the chip's internal logic, the RESET input must be held Low for at least 30 XTAL clock cycles. The control registers and ports are reset to their default conditions after a reset from the RESET pin. The control registers and ports are not reset to their default conditions after wakeup from Stop Mode or WDT timeout.

During $\overline{\text{RESET}}$, the program counter is loaded with 0020H. I/O ports and control registers are configured to their default reset state. Resetting the Z8E001 does not affect the contents of the general-purpose registers.

RESET PIN OPERATION

The Z8E001 hardware $\overline{\text{RESET}}$ pin initializes the control and peripheral registers, as shown in Table 4. Specific reset values are shown by 1 or 0, while bits whose states are unchanged or unknown from Power-Up are indicated by the letter U.

$\overline{\text{RESET}}$ must be held Low until the oscillator stabilizes, for an additional 30 XTAL clock cycles, in order to be sure that the internal reset is complete. The RESET pin has a Schmitt-Trigger input with a trip point. There is no High side protection diode. The user should place an external diode from $\overline{\text{RESET}}$ to V_{CC}. A pull-up resistor on the $\overline{\text{RESET}}$ pin is approximately 500 KΩ, typical.

Program execution starts 10 XTAL clock cycles after $\overline{\text{RESET}}$ has returned High. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration, followed by initialization of the remaining control registers.

Table 4. Control and Peripheral Registers

		Bits								
Register (HEX)	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by RESET
FE	Reserved									
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by RESET
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by RESET
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by $\overline{\text{RESET}}$
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by RESET
F9–F0	Reserved									
EF–E0	Virtual Copy									Virtual Copy of the Current Working Register Set
DF–D8	Reserved									

RESET PIN OPERATION (Continued)

Table 4. Control and Peripheral Registers (Continued)

		Bits								
Register (HEX)	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**
D7	Port B Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET
D6	Port B Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortB after RESET
D5	Port B Output	U	U	U	U	U	U	U	U	Output register not affected by RESET
D4	Port B Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET
D3	Port A Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET
D2	Port A Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after RESET
D1	Port A Output	U	U	U	U	U	U	U	U	Output register not affected by RESET
D0	Port A Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET
CF	Reserved									
CE	Reserved									
CD	T1VAL	U	U	U	U	U	U	U	U	
CC	T0VAL	U	U	U	U	U	U	U	U	
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	T1ARHI	U	U	U	U	U	U	U	U	
C6	T0ARHI	U	U	U	U	U	U	U	U	
C5	T1ARLO	U	U	U	U	U	U	U	U	
C4	T0ARLO	U	U	U	U	U	U	U	U	
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT Enabled in HALT Mode, WDT timeout at maximum value, STOP Mode disabled
C0	TCTLLO	0	0	0	0	0	0	0	0	All standard timers are disabled

Note: *The SMR and WDT flags are set indicating the source of the $\overline{\text{RESET}}$.

RESET PIN OPERATION (Continued)

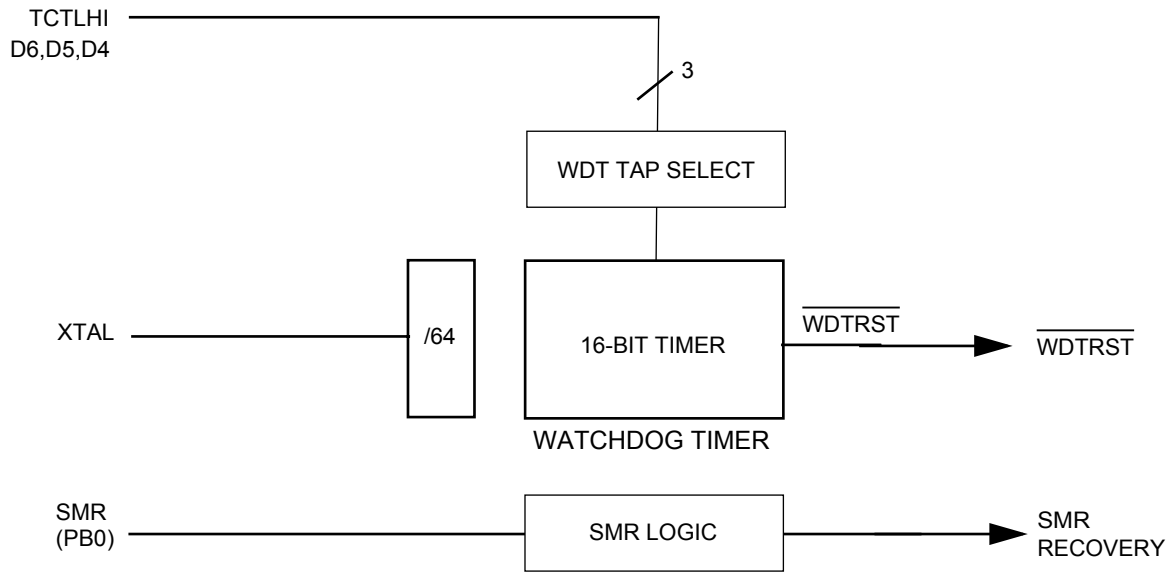

Figure 11. Z8E001 Reset Circuitry with WDT and SMR

Note: The WDT can only be disabled via software if the first instruction out of RESET performs this function. Logic within the Z8E001 detects that it is in the process of executing the first instruction after the part leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware does not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 6 indicates the range of timeout values that can be obtained. The default values of D6, D5, and D4 are all 1, thus setting the WDT to its maximum timeout period when coming out of RESET.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. A 0 prevents the WDT from resetting the part while halted.Coming out of reset, the WDT is enabled during HALT Mode.

STOP MODE (D3). Coming out of RESET, the Z8E001 STOP Mode is disabled. If an application requires use of STOP Mode, bit D3 must be cleared immediately upon leaving RESET. If bit D3 is set, the STOP instruction executes as a NOP. If bit D3 is cleared, the STOP instruction enters Stop Mode. Whenever the Z8E001 wakes up after having been in STOP Mode, the STOP Mode is again disabled.

Bits 2, 1 and 0. These bits are reserved and must be 0.

Table 6. WDT Time-Out

D6	D5	D4	Crystal Clocks* to Timeout	Time-Out Using a 10 MHZ Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	4,194,304 TpC	419.43 ms

Note:
*TpC=XTAL clock cycle. The default on reset is D6=D5=D4=1.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E001 MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter the HALT Mode, the Z8E001 only requires a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F      HALT            ; enter HALT Mode
```

The HALT Mode can be exited by servicing an interrupt (either externally or internally) generated. Upon completion of the interrupt service routine, the user program continues from the instruction after the HALT instruction.

The HALT Mode can also be exited via a RESET activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution restarts at the reset restart address 0020H.

OSCILLATOR OPERATION

The Z8E001 MCU uses a Pierce oscillator with an internal feedback resistor (Figure 14). The advantages of this circuit are low-cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements (A x B = 1; where $A = V_o/V_i$ is the gain of the amplifier and $B = V_i/V_o$ is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees). V_{IN} must be in phase with itself; therefore, the amplifier/inverter provides a 180-degree phase shift, and the feedback element is forced to provide the other 180-degree phase shift.

R1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and provide the start-up transition.

Capacitor C_2, combined with the amplifier output resistance, provides a small phase shift. It also provides some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides an additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

Layout

Traces connecting crystal, caps, and the Z8E001 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E001.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E001 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8E001 V_{SS} (GND) pin. It should not be shared with any other system ground trace or components except at the Z8E001 device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

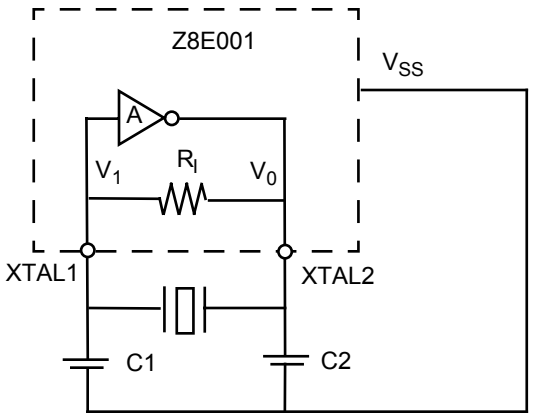

Figure 14. Pierce Oscillator with Internal Feedback Circuit

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. To fix the problem, the capacitors C1/C2 require reduction. The amplifier gain is either not adequate at frequency, or the crystal Rs are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At that point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller, or a low-resistance crystal should be used.

Circuit Board Design Rules

The following circuit board design rules are suggested:

- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E001 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.

OSCILLATOR OPERATION (Continued)

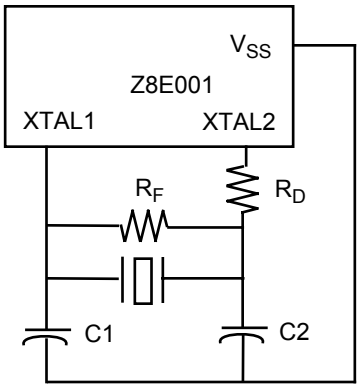

Figure 16. Crystal/Ceramic Resonator Oscillator

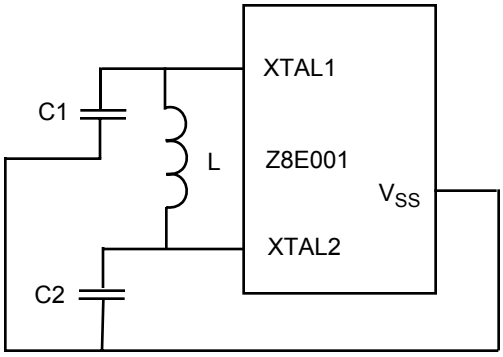

Figure 17. LC Clock

In most cases, the R_D is 0 Ohms and R_F is infinite. These specifications are determined and specified by the crystal/ceramic resonator manufacturer. The R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. It can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. The R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8E001 oscillator already has an internal shunt resistor in parallel to the crystal/ceramic resonator.

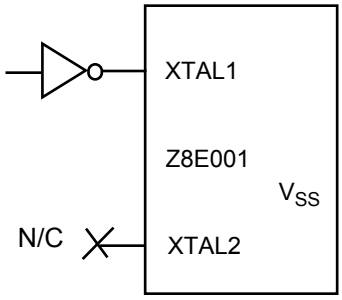

Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8E001. This requirement assures that no system noise is injected into the Z8E001 clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8E001.

Note: A parallel resonant crystal or resonator data sheet specifies a load capacitor value that is a series combination of C_1 and C_2, including all parasitics (PCB and holder).

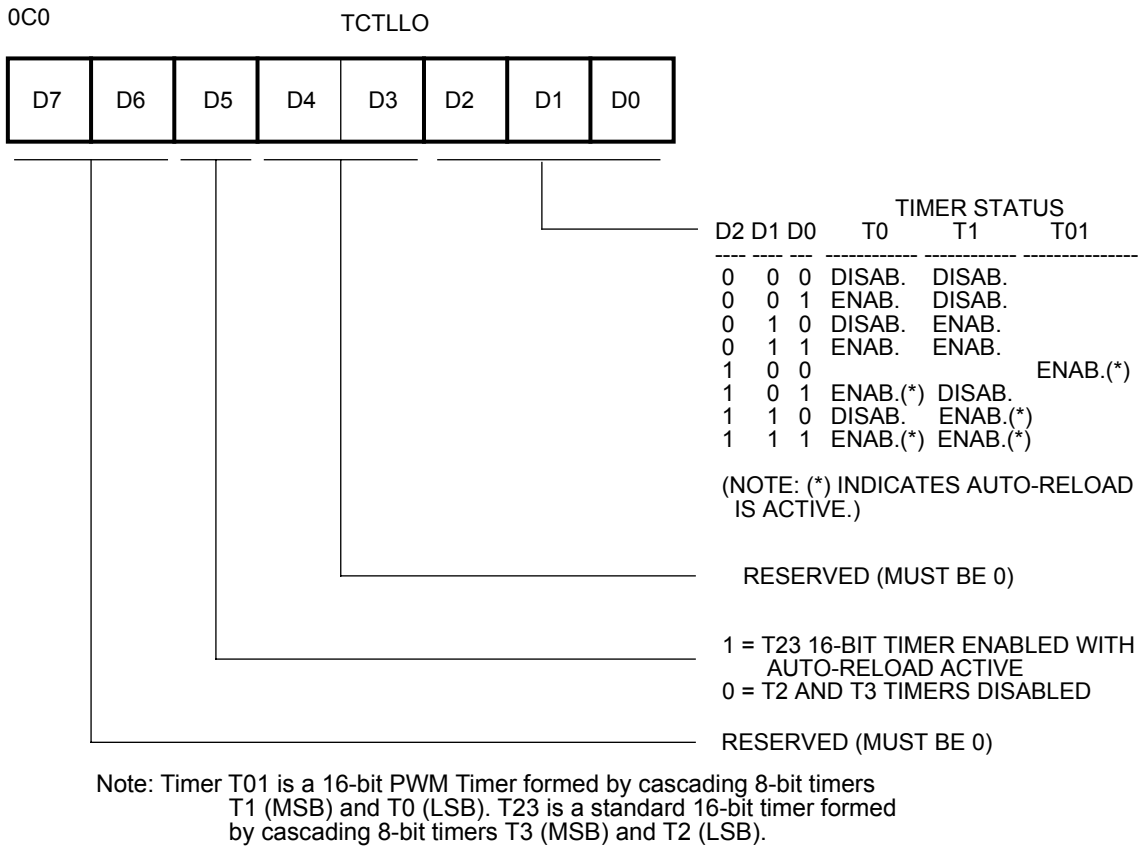

Figure 22. TCTLLO Register

Each 8-bit timer is provided a pair of registers, which are both readable and writable. One of the registers is defined to contain the auto-initialization value for the timer, while the second register contains the current value for the timer. When a timer is enabled, the timer decrements whatever value is currently held in its count register, and then continues decrementing until it reaches 0. At this time, an interrupt is generated and the contents of the auto-initialization register optionally copy into the count value register. If auto-initialization is not enabled, the timer stops counting upon reaching 0, and control logic clears the appropriate control register bit to disable the timer. This operation is referred to as "single-shot". If auto-initialization is enabled, the timer continues counting from the initialization value. Software should not attempt to use registers that are defined as having timer functionality.

Software is allowed to write to any register at any time, but care should be taken if timer registers are updated while the timer is enabled. If software updates the count value while the timer is in operation, the timer continues counting based upon the software-updated value.

Note: Strange behavior can result if the software update occurred at exactly the point that the timer was reaching 0 to trigger an interrupt and/or reload.

Similarly, if software updates the initialization value register while the timer is active, the next time that the timer reaches 0, it initializes using the updated value.

Note: Strange behavior could result if the initialization value register is being written while the timer is in the process of being initialized.

Whether initialization is done with the new or old value is a function of the exact timing of the write operation. In all cases, the Z8E001 prioritizes the software write above that of a decrementer writeback; however, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit overrides a software write. Reading either register can be done

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read returns the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register takes effect based upon the timing of the internal instruction pipeline, but is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others; however, care should be taken when updating the directional control and special function registers.

When updating a Directional Control Register, the Special Function Register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately, and all initialization has been completed.

PORT A

Port A is a general-purpose port. Figure 26 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 27. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27).

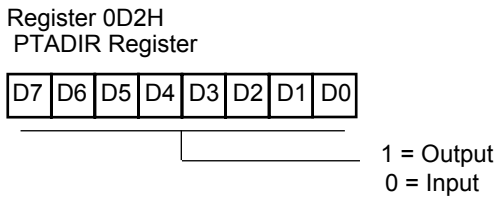

Figure 26. Port A Directional Control Register

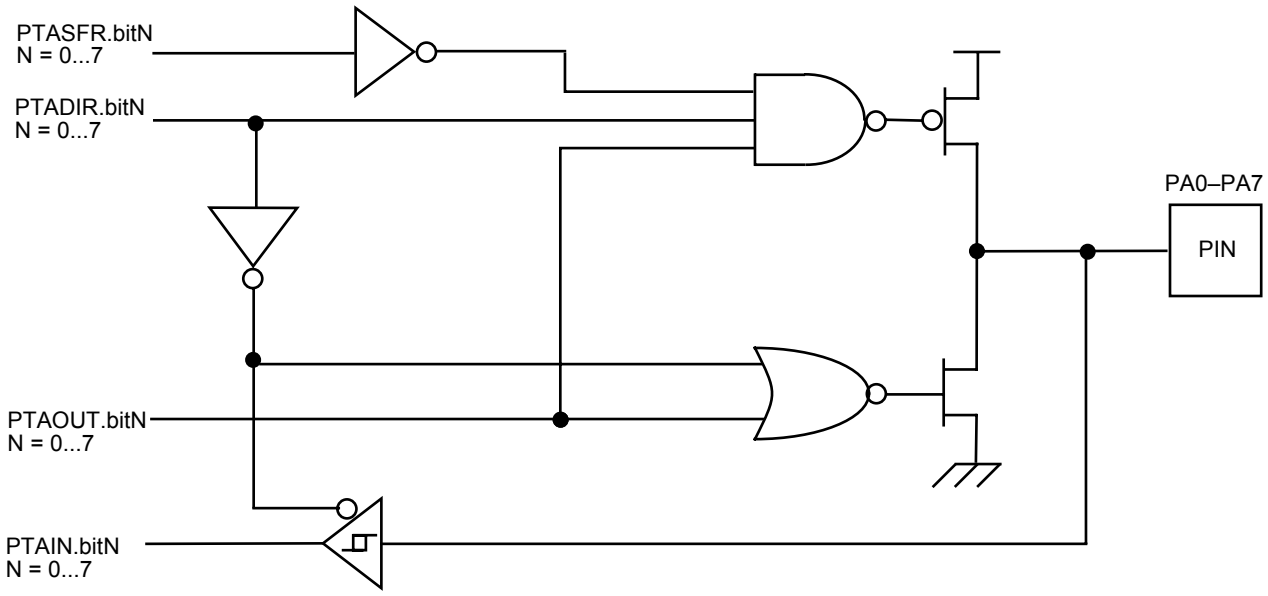

Figure 27. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

PORT A REGISTER DIAGRAMS

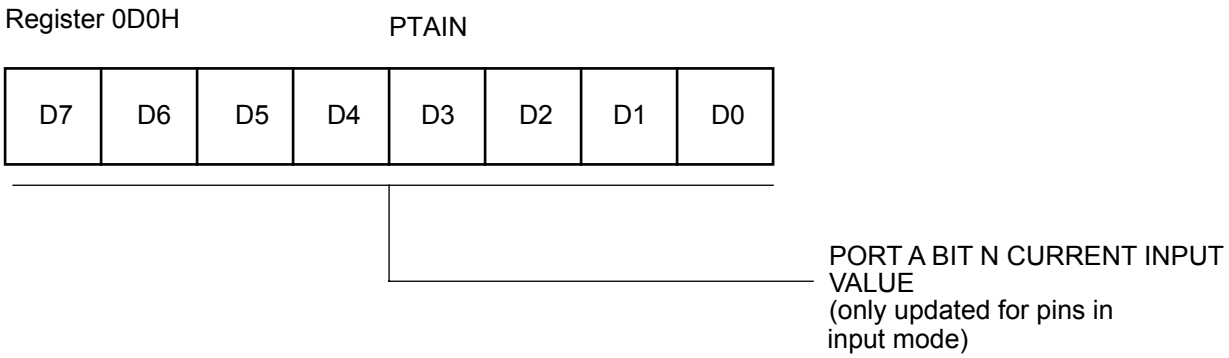

Figure 28. Port A Input Value Register

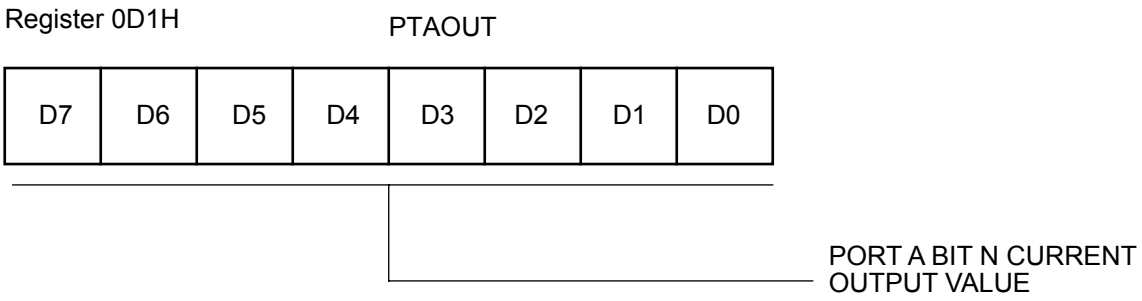

Figure 29. Port A Output Value Register

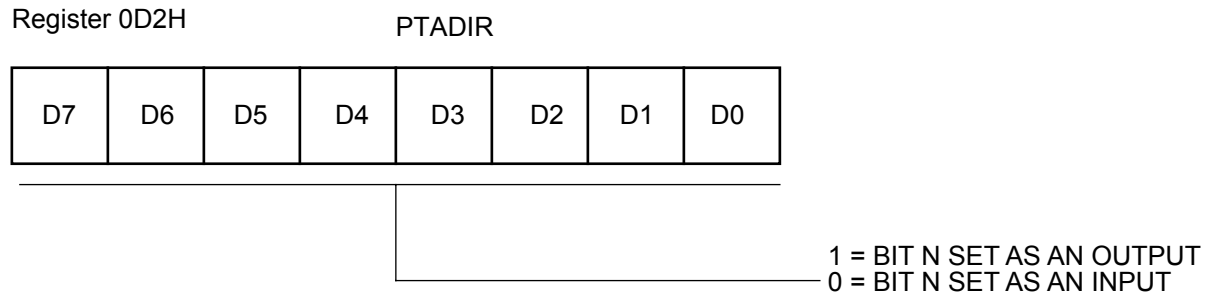

Figure 30. Port A Directional Control Register

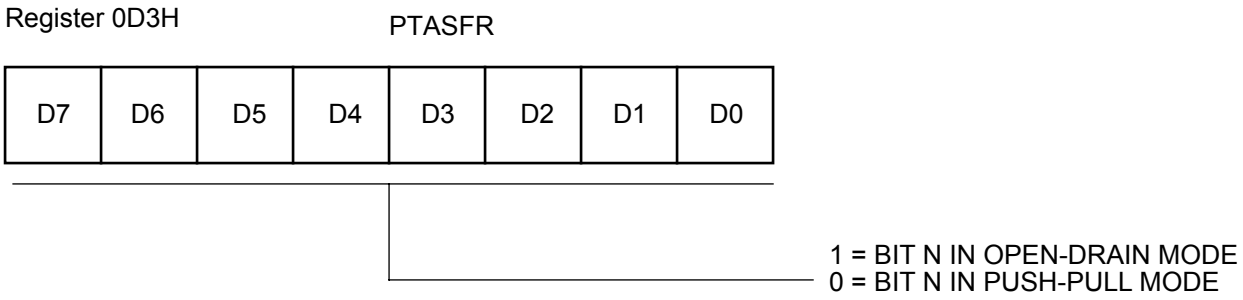

Figure 31. Port A Special Function Register

PORT B—PIN 0 CONFIGURATION

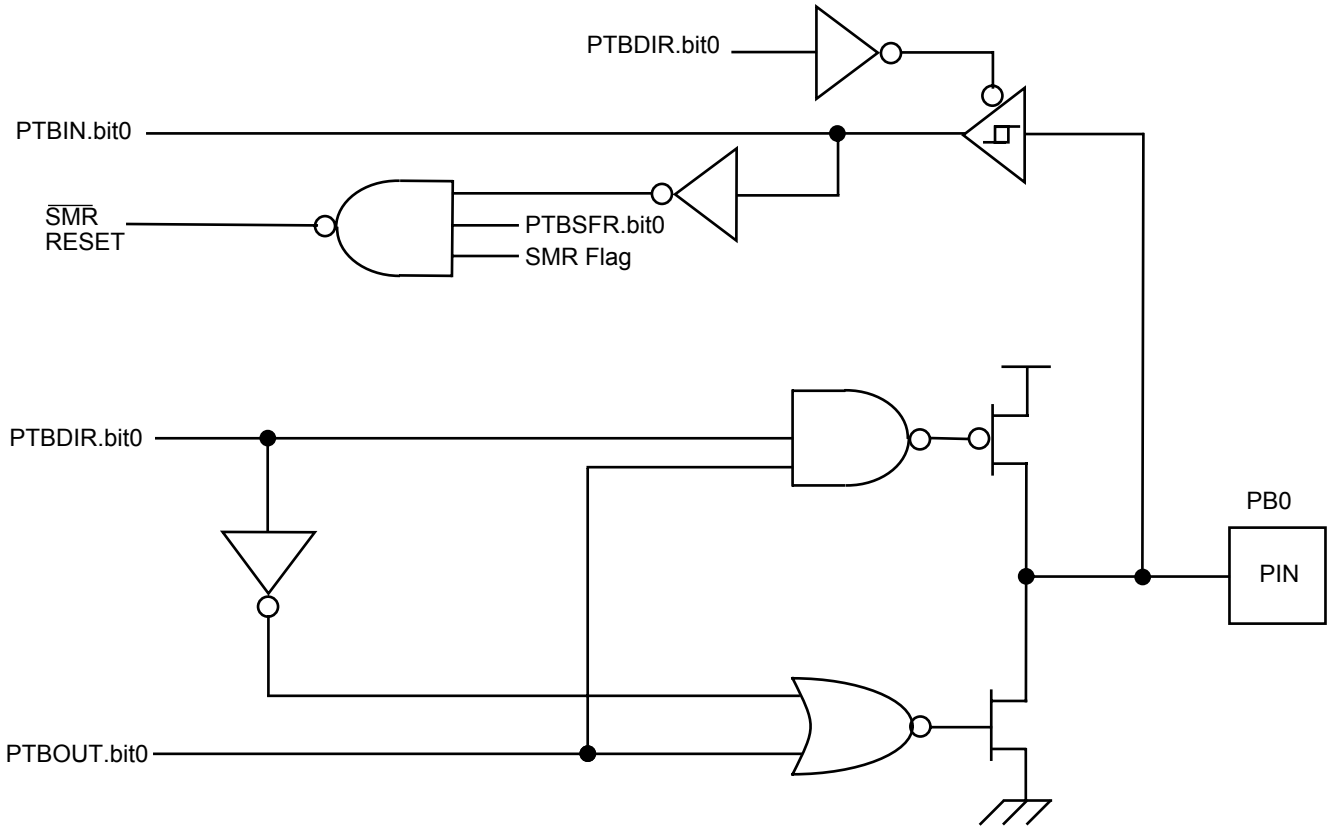

Figure 33. Port B Pin 0 Diagram

PORT B—PIN 1 CONFIGURATION

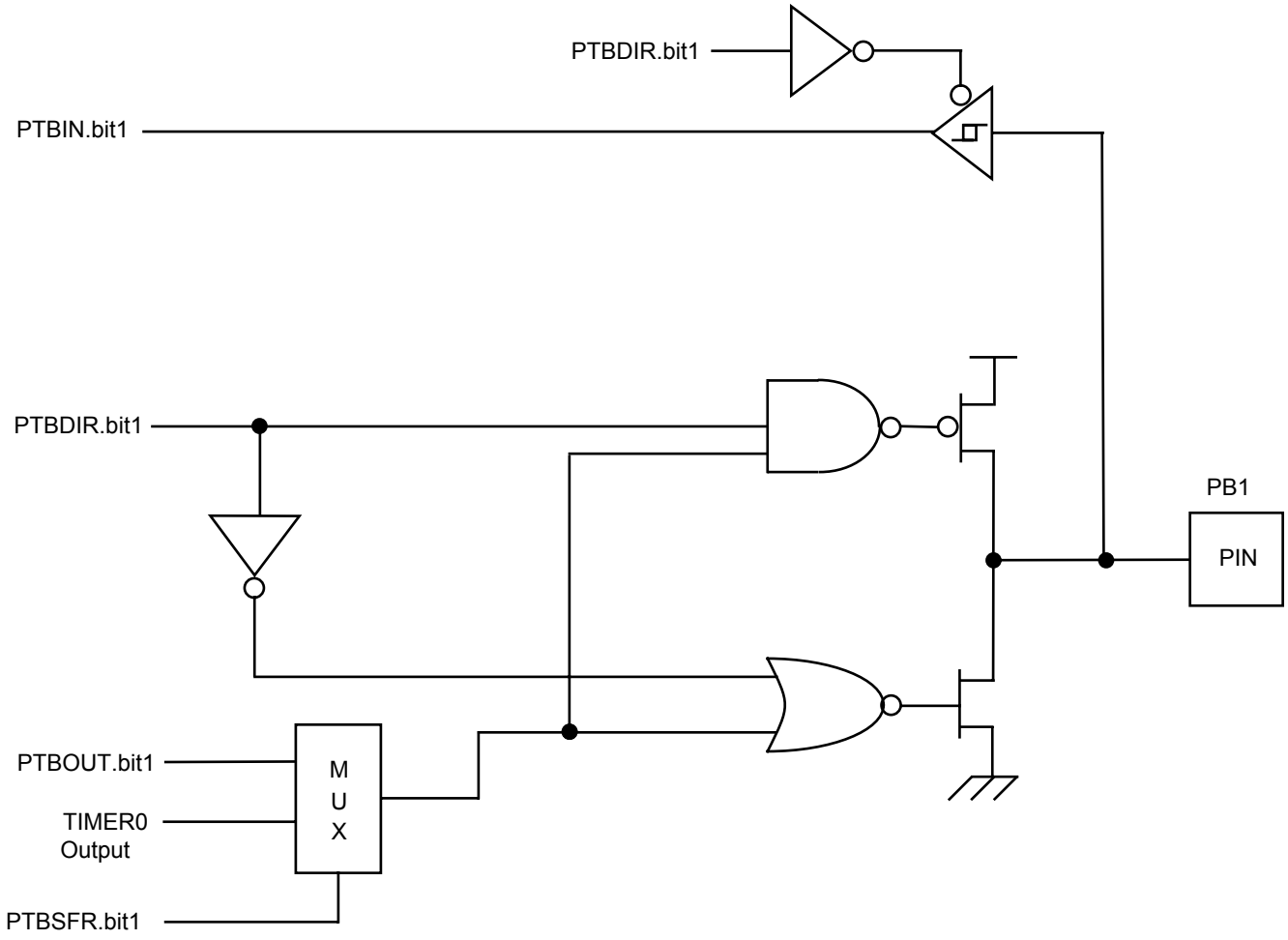

Figure 34. Port B Pin 1 Diagram

PORT B—PIN 2 CONFIGURATION

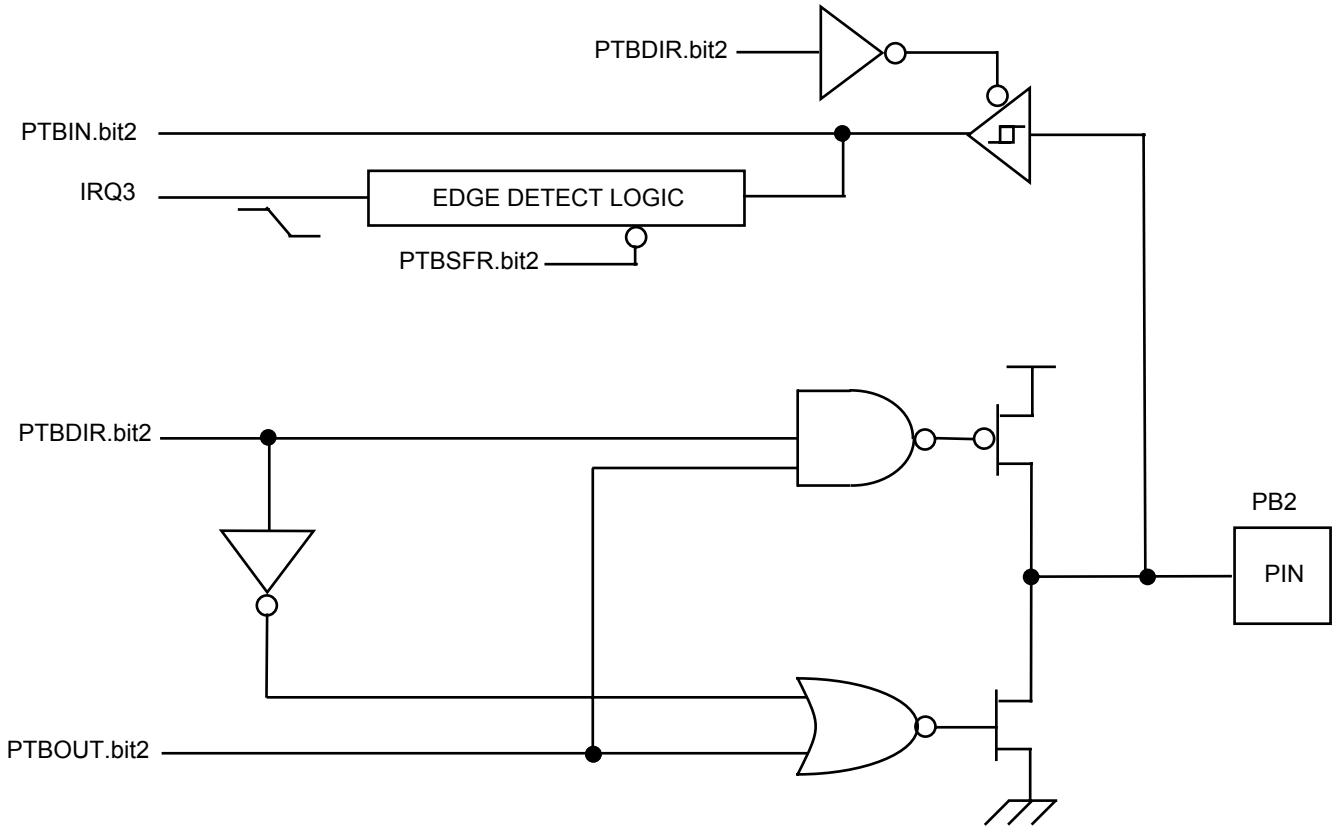

Figure 35. Port B Pin 2 Diagram

PORT B CONTROL REGISTERS

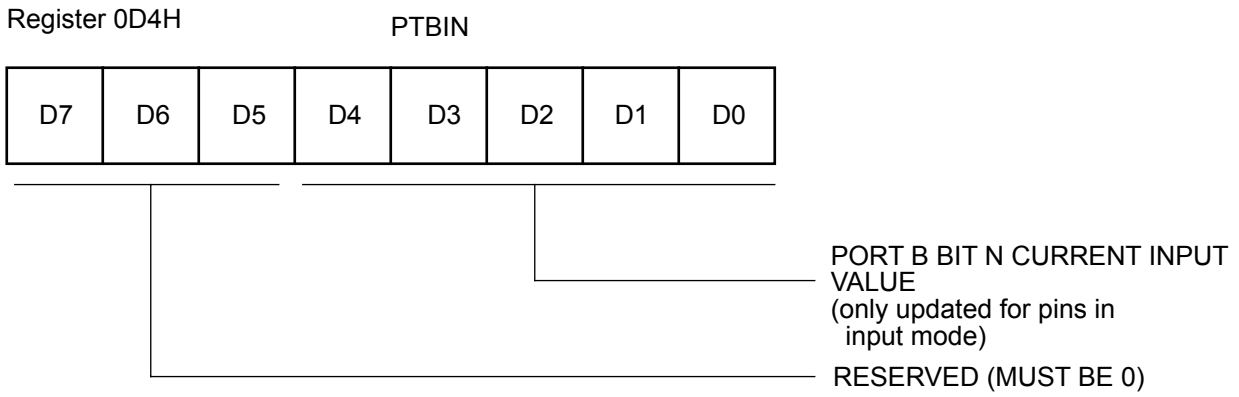

Figure 37. Port B Input Value Register

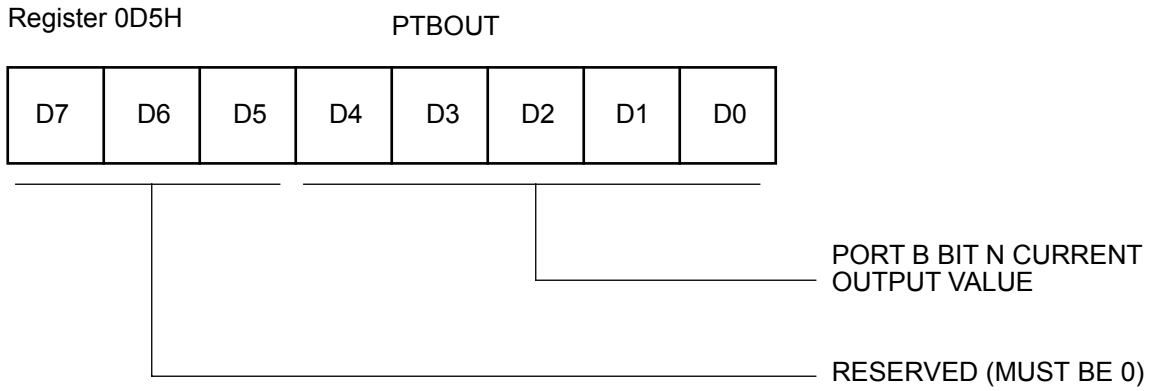

Figure 38. Port B Output Value Register

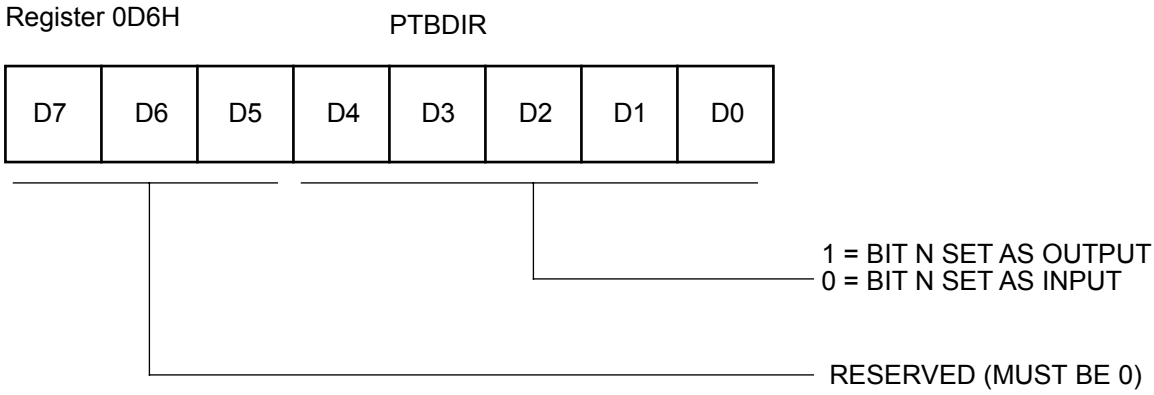

Figure 39. Port B Directional Control Register

I/O PORT RESET CONDITIONS

Full Reset

Port A and Port B output value registers are not affected by RESET.

On $\overline{\text{RESET}}$, the Port A and Port B directional control registers is cleared to all zeros, which defines all pins in both ports as inputs.

On $\overline{\text{RESET}}$, the directional control registers redefine all pins as inputs, and the Port A and Port B input value registers overwrites the previously held data with the current sample of the input pins.

On $\overline{\text{RESET}}$, the Port A and Port B special function registers is cleared to all zeros, which deactivates all port special functions.

Note: The SMR and WDT timeout events are NOT full device resets. The port control registers are not affected by either of these events.

ANALOG COMPARATOR

The Z8E001 includes one on-chip analog comparator. Pin PB4 has a comparator front end. The comparator reference voltage is on pin PB3.

Comparator Description

The on-chip comparator can process an analog signal on PB4 with reference to the voltage on PB3. The analog function is enabled by programming the Port B Special Function Register bits 3 and 4.

When the analog comparator function is enabled, bit 4 of the input register is defined as holding the synchronized output of the comparator, while bit 3 retains a synchronized sample of the reference input.

If the interrupts for PB4 are enabled when the comparator special function is selected, the output of the comparator generates interrupts.

COMPARATOR OPERATION

The comparator output reflects the relationship between the analog input to the reference input. If the voltage on the analog input is higher than the voltage on the reference input, then the comparator output is at a High state. If the voltage on the analog input is lower than the voltage on the reference input, then the analog output will be at a Low state.

Comparator Definitions

V_{ICR}

The usable voltage range for the positive input and reference input is called the common mode voltage range (V_{ICR}).

Note: The comparator is not guaranteed to work if the input is outside of the V_{ICR} range.

V_{OFFSET}

The absolute value of the voltage between the positive input and the reference input required to make the comparator output voltage switch is the input offset voltage (V_{OFFSET}).

I_{IO}

For the CMOS voltage comparator input, the input offset current (I_{IO}) is the leakage current of the CMOS input gate.

HALT Mode

The analog comparator is functional during HALT Mode. If the interrupts are enabled, an interrupt generated by the comparator will cause a return from HALT Mode.

STOP Mode

The analog comparator is disabled during STOP Mode. The comparator is powered down to prevent it from drawing any current.

INPUT PROTECTION

All I/O pins on the Z8E001 have diode input protection. There is a diode from the I/O pad to V_{CC} and V_{SS} (Figure 41).

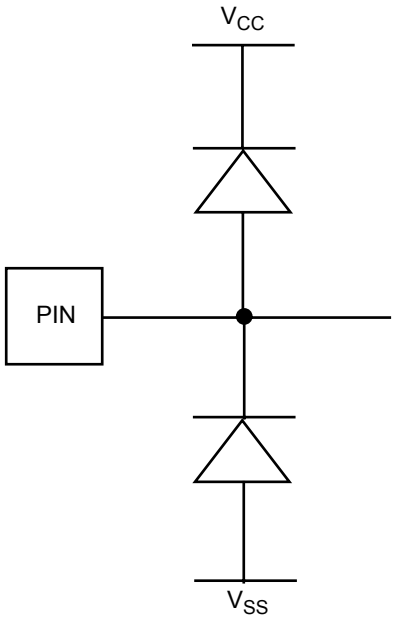

Figure 41. I/O Pin Diode Input Protection

However, on the Z8E001, the $\overline{\text{RESET}}$ pin has only the input protection diode from pad to V_{SS} (Figure 42).

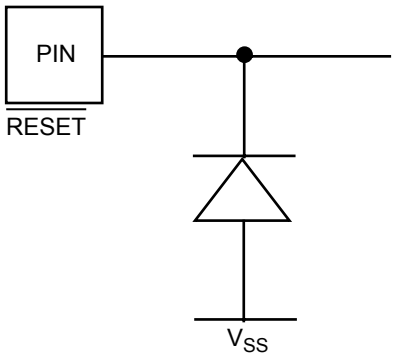

Figure 42. $\overline{\text{RESET}}$ Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{CC} from this pin can be required to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.