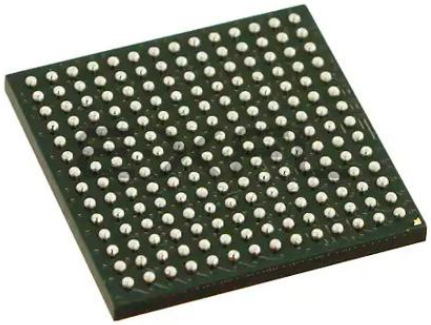

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Product Status	Not For New Designs
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
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Peripherals	DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf53721cvm240

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Table 1. MCF537*x* Family Configurations (continued)

Module	MCF5372	MCF5372L	MCF53721	MCF5373	MCF5373L
Static RAM (SRAM)	32 Kbytes				
SDR/DDR SDRAM Controller	•	•	•	•	•
USB 2.0 Host	—	•	•	—	•
USB 2.0 On-the-Go	—	•	•	—	•
Synchronous Serial Interface (SSI)	•	•	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•
Cryptography Hardware Accelerators	—	—	—	•	•
Embedded Voice-over-IP System Solution	—	—	•	—	—
FlexCAN 2.0B communication module	—	—	•	—	—
UARTs	3	3	3	3	3
I^2C	•	•	•	•	•
QSPI	•	•	•	•	•
PWM Module	—	•	•	—	•
Real Time Clock	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2	2
16-channel Direct Memory Access (DMA)	•	•	•	•	•
FlexBus External Interface	•	•	•	•	•
General Purpose I/O (GPIO)	up to 46	up to 62	up to 62	up to 46	up to 62
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•
Package	160 QFP	196 MAPBGA	196 MAPBGA	160 QFP	196 MAPBGA

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF5372CAB180	MCF5372 RISC Microprocessor	160 QFP	180 MHz	–40° to +85° C
MCF5372LCVM240	MCF5372 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C
MCF53721CVM240	MCF53721 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C
MCF5373CAB180	MCF5373 RISC Microprocessor	160 QFP	180 MHz	–40° to +85° C
MCF5373LCVM240	MCF5373 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C

3 Hardware Design Considerations

3.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 2 should be connected between the board V_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

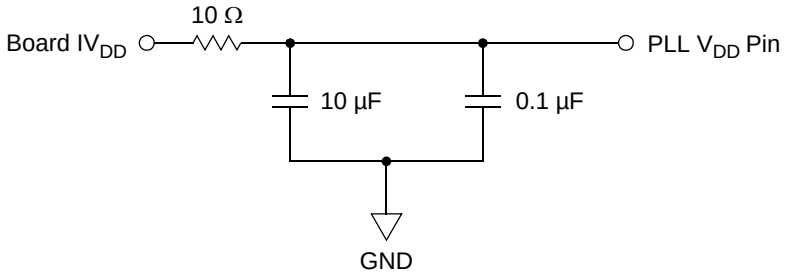

Figure 2. System PLL V_{DD} Power Filter

3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 3 should be connected between the board EV_{DD} or IV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

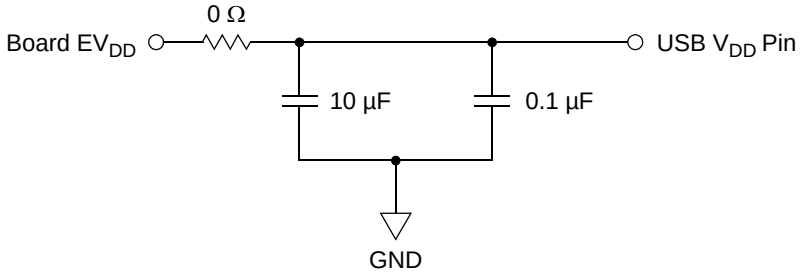

Figure 3. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

3.3 Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

3.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must powered up. IV_{DD} should not lead the EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or there is

high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

3.3.2 Power Down Sequence

If IV_{DD}/$PLLV_{DD}$ are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLLV_{DD}$ power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or there is undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/$PLLV_{DD}$ to 0 V.
2. Drop EV_{DD}/SDV_{DD} supplies.

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF537*x* pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to Section 7, "Package Information," for package diagrams. For a more detailed discussion of the MCF537*x* signals, consult the *MCF5373 Reference Manual* (MCF5373RM).

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., A23), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO default to their GPIO functionality.

Table 3. MCF5372/3 Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
Reset							
$\overline{\text{RESET}}$[2]	—	—	—	I	EVDD	95	K13
$\overline{\text{RSTOUT}}$	—	—	—	O	EVDD	86	L12
Clock							
EXTAL	—	—	—	I	EVDD	91	L14
XTAL[2]	—	—	—	O	EVDD	93	K14
EXTAL32K	—	—	—	I	EVDD	—	P13
XTAL32K	—	—	—	O	EVDD	—	N13
FB_CLK	—	—	—	O	SDVDD	40	N1

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
SD_CLK	—	—	—	O	SDVDD	37	L1
$\overline{\text{SD\_CLK}}$	—	—	—	O	SDVDD	38	M1
$\overline{\text{SD\_CS0}}$	—	—	—	O	SDVDD	15	F3
SD_DQS3	—	—	—	O	SDVDD	25	H1
SD_DQS2	—	—	—	O	SDVDD	55	N5
$\overline{\text{SD\_SCAS}}$	—	—	—	O	SDVDD	44	M3
$\overline{\text{SD\_SRAS}}$	—	—	—	O	SDVDD	45	M4
SD_SDR_DQS	—	—	—	O	SDVDD	35	L2
$\overline{\text{SD\_WE}}$	—	—	—	O	SDVDD	13	E1
External Interrupts Port[5]							
$\overline{\text{IRQ7}}$[2]	PIRQ7[2]	—	—	I	EVDD	102	F13
$\overline{\text{IRQ6}}$[2]	PIRQ6[2]	USBHOST_ VBUS_EN	—	I	EVDD	—	F12
$\overline{\text{IRQ5}}$[2]	PIRQ5[2]	USBHOST_ VBUS_OC	—	I	EVDD	—	F11
$\overline{\text{IRQ4}}$[2]	PIRQ4[2]	SSI_MCLK	—	I	EVDD	101	G14
$\overline{\text{IRQ3}}$[2]	PIRQ3[2]	—	—	I	EVDD	—	G13
$\overline{\text{IRQ2}}$[2]	PIRQ2[2]	USB_CLKIN	—	I	EVDD	—	G12
$\overline{\text{IRQ1}}$[2]	PIRQ1[2]	$\overline{\text{DREQ1}}$[2]	SSI_CLKIN	I	EVDD	100	G11
FEC							
FEC_MDC	PFECI2C3	I2C_SCL[2]	—	O	EVDD	4	B1
FEC_MDIO	PFECI2C2	I2C_SDA[2]	—	I/O	EVDD	3	A1
FEC_COL	PFECH7	—	—	I	EVDD	144	B6
FEC_CRS	PFECH6	—	—	I	EVDD	145	A6
FEC_RXCLK	PFECH5	—	—	I	EVDD	146	A5
FEC_RXDV	PFECH4	—	—	I	EVDD	147	B5
FEC_RXD[3:0]	PFECH[3:0]	—	—	I	EVDD	148–151	C5, D5, A4, B4
FEC_RXER	PFECL7	—	—	I	EVDD	152	C4
FEC_TXCLK	PFECL6	—	—	I	EVDD	153	A3
FEC_TXEN	PFECL5	—	—	O	EVDD	154	B3
FEC_TXER	PFECL4	—	—	O	EVDD	155	A2
FEC_TXD[3:0]	PFECL[3:0]	—	—	O	EVDD	157, 158, 1, 2	D4, C3, B2, C2

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
Test							
TEST[8]	—	—	—	I	EVDD	124	E10
Power Supplies							
EVDD	—	—	—	—	—	9, 69, 71, 81, 94, 103, 139, 160	E6, E7, F5–F7, G5, H10, J8, K8–K9
IVDD	—	—	—	—	—	36, 79, 97, 125, 156	E5, J9, K5, K10
PLL_VDD	—	—	—	—	—	99	J10
SD_VDD	—	—	—	—	—	11, 39, 41, 67, 105, 121, 137	E8–E9, F8–F10, J4–J7, H5, K6, K7
USB_VDD	—	—	—	—	—	—	H12
VSS	—	—	—	—	—	10, 42, 68, 82, 89, 104, 122, 138, 159	G6–G9, H6–H9
PLL_VSS	—	—	—	—	—	98	H11
USB_VSS	—	—	—	—	—	—	J14

1 Refers to pin's primary function.

2 Pull-up enabled internally on this signal for this mode.

3 The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.

4 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.

5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

6 MCF53721 only.

7 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

8 Pull-down enabled internally on this signal for this mode.

NOTE

4.2 Pinout—196 MAPBGA

The pinout for the MCF5373LCVM240, MCF5372LCVM240, and MCF53721CVM240 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	FEC_ MDIO	FEC_ TXER	FEC_ TXCLK	FEC_ RXD1	FEC_ RXCLK	FEC_ CRS	U1TXD	FB_CS2	A23	A19	A15	A12	A10	A9	A
B	FEC_ MDC	FEC_ TXD1	FEC_ TXEN	FEC_ RXD0	FEC_ RXDV	FEC_ COL	U1RXD	FB_CS3	A22/	A18	A14	A11	A7	A8	B
C	DT2IN	FEC_ TXD0	FEC_ TXD2	FEC_ RXER	FEC_ RXD3	U1CTS	FB_CS0	FB_CS4	A21	A17	A13	A6	A3	A4	C
D	DT3IN	DT1IN	DT0IN	FEC_ TXD3	FEC_ RXD2	U1RTS	FB_CS1	FB_CS5	A20	A16	A5	A0	A1	A2	D
E	SD_WE	TS	I2C_SCL	I2C_SDA	IVDD	EVDD	EVDD	SD_VDD	SD_VDD	TEST	PWM3	PWM5	PWM7	TA	E
F	D14	D15	SD_CS0	SD_CKE	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	IRQ5	IRQ6	IRQ7	PWM1	F
G	D10	D11	D12	D13	EVDD	VSS	VSS	VSS	VSS	JTAG_ EN	IRQ1	IRQ2	IRQ3	IRQ4	G
H	SD_ DQS3	BE/ BWE1	D8	D9	SD_VDD	VSS	VSS	VSS	VSS	EVDD	PLL_ VSS	USBOTG _VDD	USB OTG_P	USB OTG_M	H
J	D30	D31	BE/ BWE3	SD_VDD	SD_VDD	SD_VDD	SD_VDD	EVDD	IVDD	PLL_ VDD	DRAM SEL	USB HOST_P	USB HOST_M	USBHOST _VSS	J
K	D26	D27	D28	D29	IVDD	SD_VDD	SD_VDD	EVDD	EVDD	IVDD	TRST/ DSCLK	TDI/DSI	RESET	XTAL	K
L	SD_CLK	SD_DR_ DQS	D24	D25	D19	D7	D3	R/W	DDATA3	PST3	TDO/ DSO	RSTOUT	TMS/ BKPT	EXTAL	L
M	SD_CLK	SD_A10	SD_CAS	SD_RAS	BE/ BWE2	D6	D2	OE	DDATA2	PST2	QSPI_ CS0	QSPI_ CS1	U0RTS	U0CTS	M
N	FB_CLK	D23	D20	D17	SD_ DQS2	D5	D1	TCLK/ PSTCLK	DDATA1	PST1	QSPI_ DOUT	QSPI_ CS2	XTAL 32K	U0TXD	N
P	D22	D21	D18	D16	BE/ BWE0	D4	D0	RCON	DDATA0	PST0	QSPI_ DIN	QSPI_ CLK	EXTAL 32K	U0RXD	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 4. MCF5373LCVM240, MCF5372LCVM240, and MCF53721CVM240 Pinout Top View (196 MAPBGA)

4.3 Pinout—160 QFP

The pinout for the MCF5372CAB180 and MCF5373CAB180 packages is shown below.

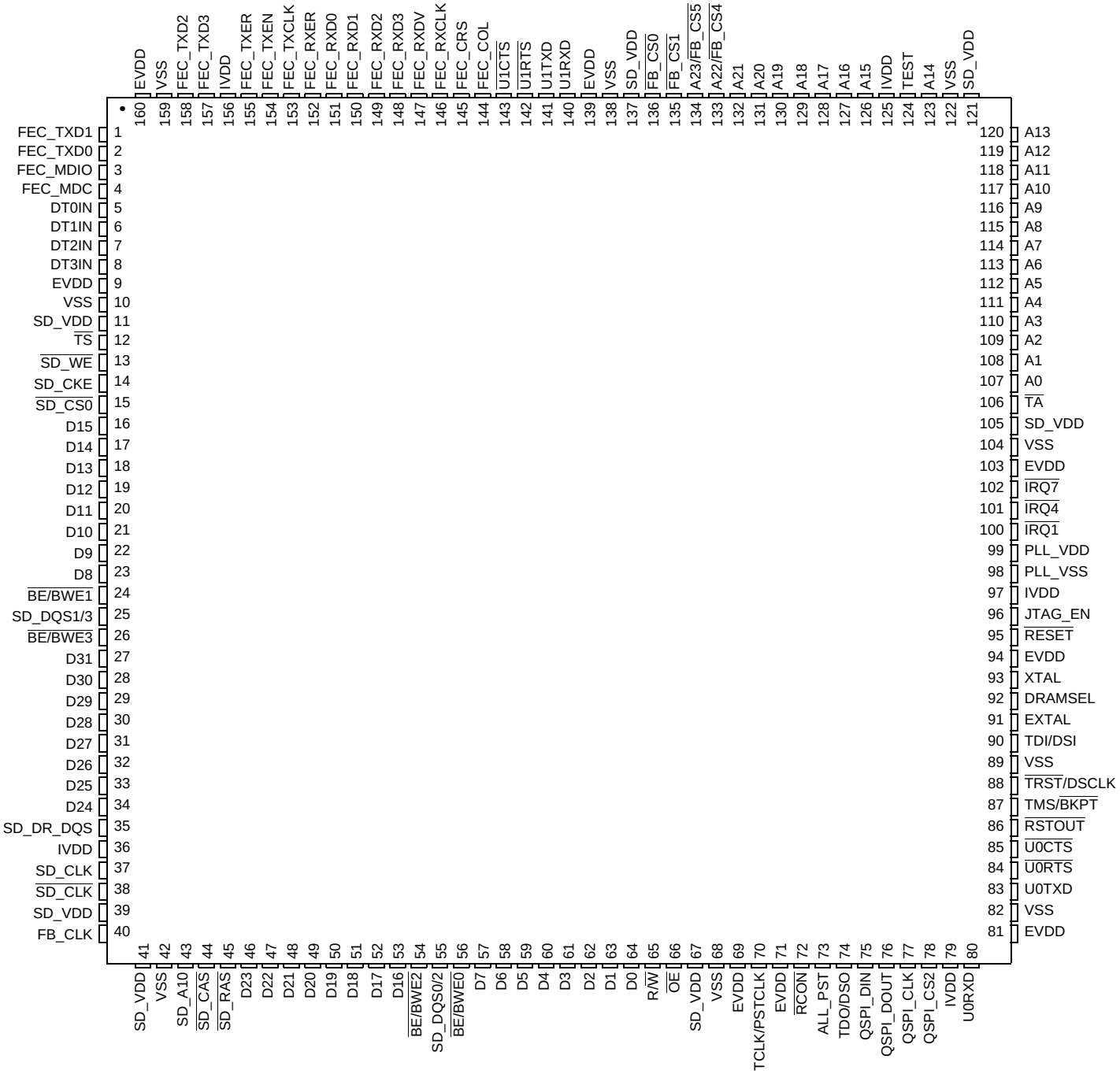

Figure 5. MCF5372CAB180 and MCF5373CAB180 Pinout Top View (160 QFP)

5.2 Thermal Characteristics

Table 5. Thermal Characteristics

Characteristic		Symbol	256MBGA	196MBGA	160QFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	37[1,2]	42[1,2]	49[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	34[1,2]	38[1,2]	44[1,2]	°C/W
Junction to board		θ_{JB}	27[3]	32[3]	40[3]	°C/W
Junction to case		θ_{JC}	16[4]	19[4]	39[4]	°C/W
Junction to top of package		Ψ_{jt}	4[1,5]	5[1,5]	12[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = P_{INT} + $P_{I/O}$
P_{INT} = I_{DD} × IV_{DD}, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

* The timings are also valid for inputs sampled on the negative clock edge.

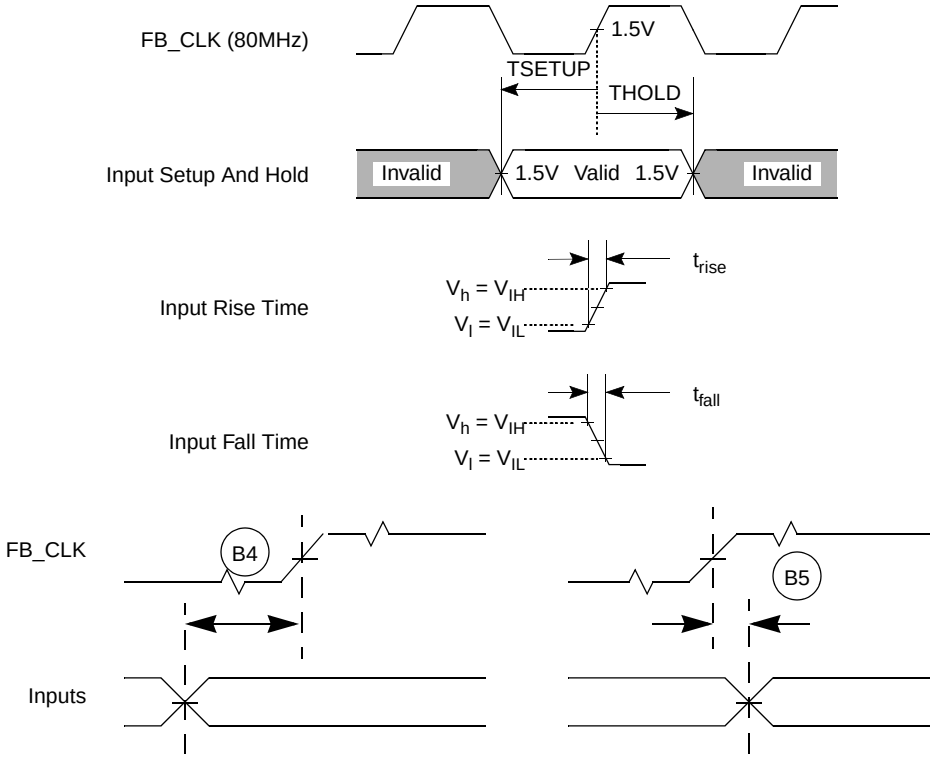

Figure 6. General Input Timing Requirements

5.6.1 FlexBus

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{FB\_CS}$[5:0]) which can be configured to be distributed between the FlexBus or SDRAM memory interfaces. Chip-select, $\overline{FB\_CS0}$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM/flash memories.

5.6.1.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the system clock.

Table 9. FlexBus AC Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit
—	Frequency of Operation	$f_{sys/3}$	—	80	Mhz
FB1	Clock Period (FB_CLK)	t_{FBCK} (t_{cyc})	12.5	—	ns
FB2	Address, Data, and Control Output Valid (A[23:0], D[31:0], $\overline{FB\_CS}$[5:0], R/$\overline{W}$, $\overline{TS}$, $\overline{BE/BWE}$[3:0] and $\overline{OE}$)[1]	$t_{FBCHDCV}$	—	7.0	ns
FB3	Address, Data, and Control Output Hold (A[23:0], D[31:0], $\overline{FB\_CS}$[5:0], R/$\overline{W}$, $\overline{TS}$, $\overline{BE/BWE}$[3:0], and $\overline{OE}$)[1, 2]	$t_{FBCHDCI}$	1	—	ns

Table 9. FlexBus AC Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
FB4	Data Input Setup	t_{DVFBCH}	3.5	—	ns
FB5	Data Input Hold	t_{DIFBCH}	0	—	ns
FB6	Transfer Acknowledge ($\overline{TA}$) Input Setup	t_{CVFBCH}	4	—	ns
FB7	Transfer Acknowledge ($\overline{TA}$) Input Hold	t_{CIFBCH}	0	—	ns

1 Timing for chip selects only applies to the $\overline{FB\_CS}$[5:0] signals. Please see Section 5.7.2, "DDR SDRAM AC Timing Characteristics" for SD_CS[3:0] timing.

2 The FlexBus supports programming an extension of the address hold. Please consult the *Reference Manual* for more information.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

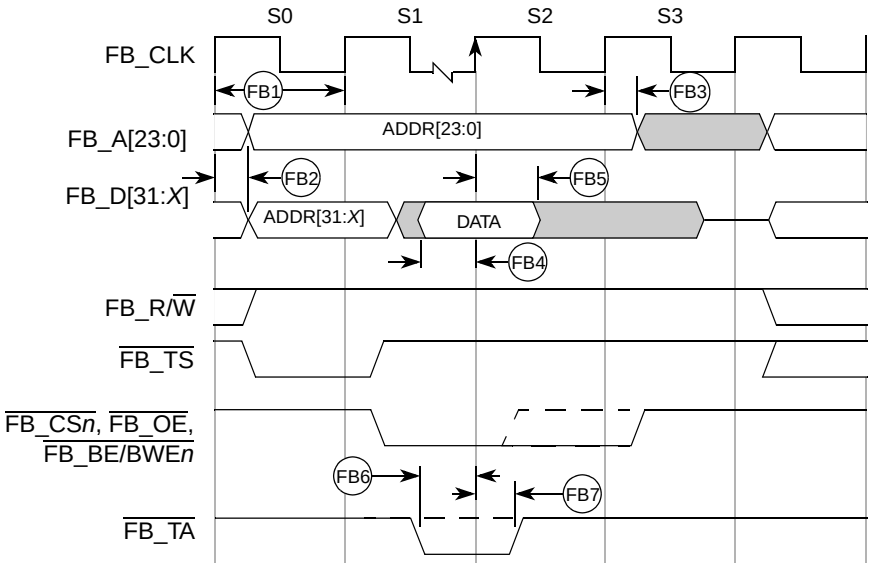

Figure 7. FlexBus Read Timing

Table 11. DDR Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)[6]	t_{DQDMI}	1.0	—	ns
DD9	Input Data Skew Relative to DQS (Input Setup)[7]	t_{DVDQ}	—	1	ns
DD10	Input Data Hold Relative to DQS[8]	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns
DD12	DQS input read preamble width	t_{DQRPRE}	0.9	1.1	SD_CLK
DD13	DQS input read postamble width	t_{DQRPST}	0.4	0.6	SD_CLK
DD14	DQS output write preamble width	t_{DQWPRE}	0.25		SD_CLK
DD15	DQS output write postamble width	t_{DQWPST}	0.4	0.6	SD_CLK

1 SD_CLK is one SDRAM clock in (ns).

2 Pulse width high plus pulse width low cannot exceed min and max clock period.

3 Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.

4 This specification relates to the required input setup time of today's DDR memories. The processor's output setup should be larger than the input setup of the DDR memories. If it is not larger, the input setup on the memory is in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].

5 The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

6 This specification relates to the required hold time of today's DDR memories. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].

7 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

8 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

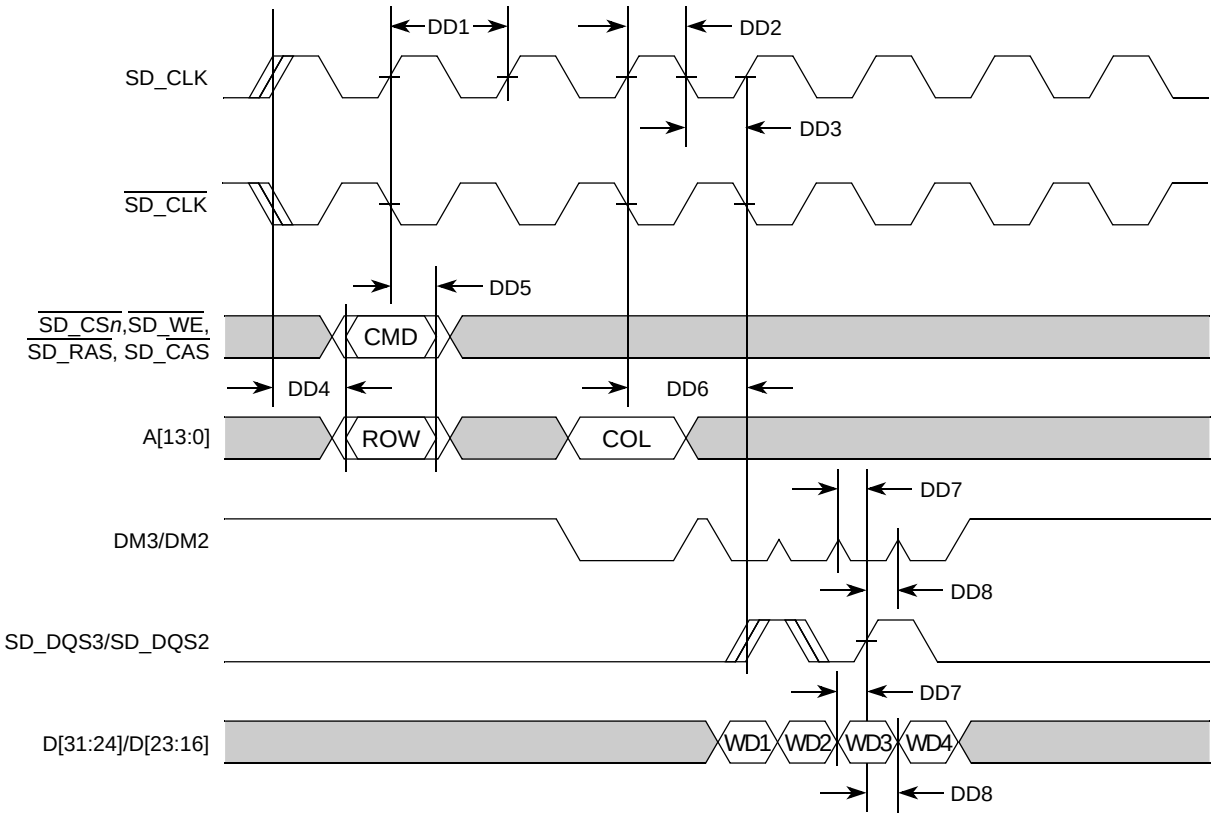

Figure 11. DDR Write Timing

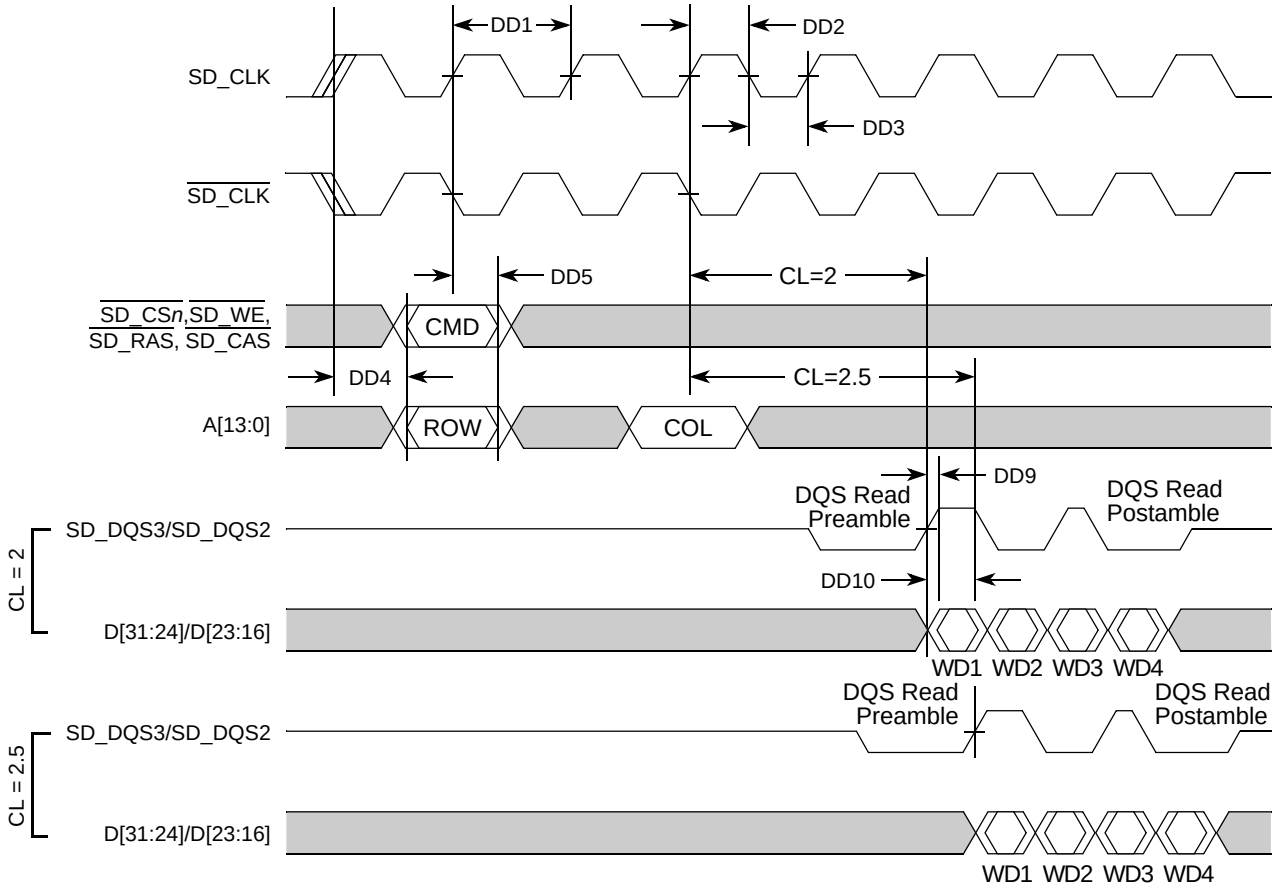

Figure 12. DDR Read Timing

5.8 General Purpose I/O Timing

Table 12. GPIO Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	FB_CLK High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	t_{PVCH}	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

1 GPIO pins include: $\overline{IRQn}$, PWM, UART, FlexCAN, and Timer pins.

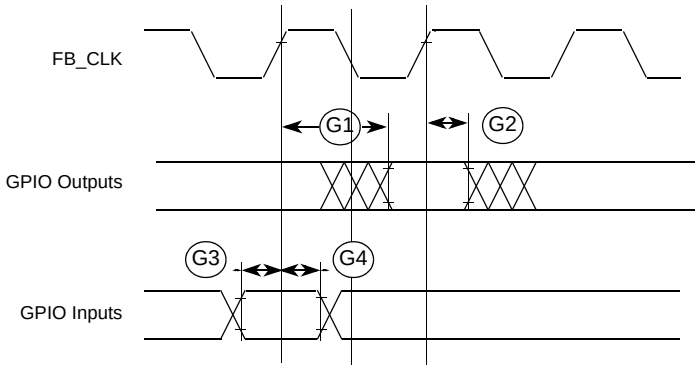

Figure 13. GPIO Timing

5.9 Reset and Configuration Override Timing

Table 13. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

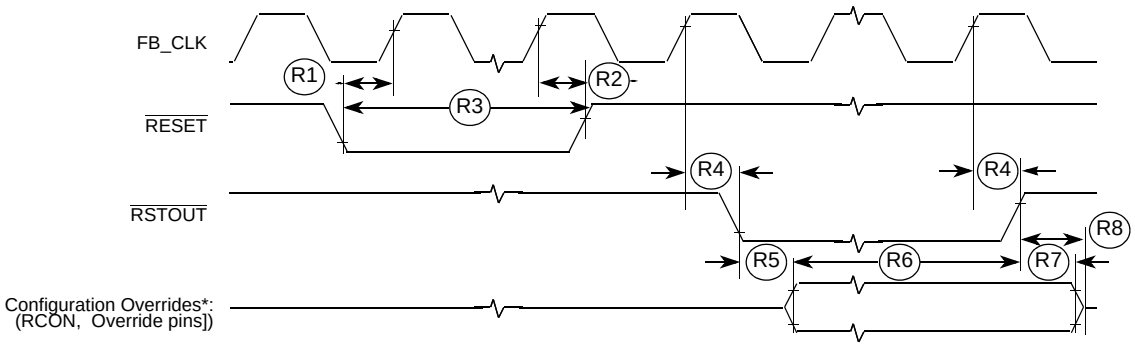

Figure 14. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF5373 Reference Manual* for more information.

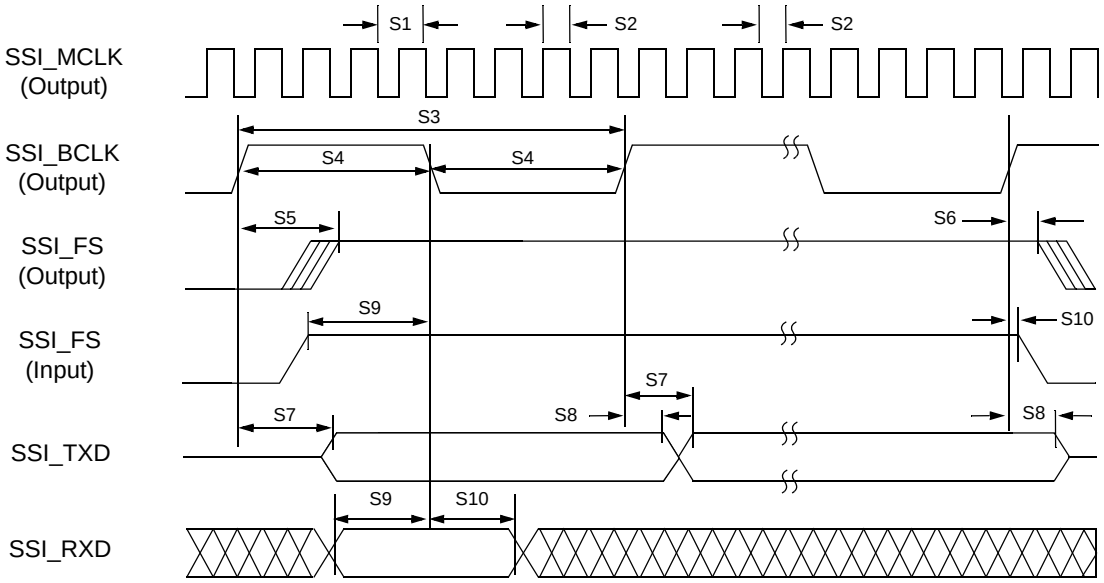

Figure 15. SSI Timing – Master Modes

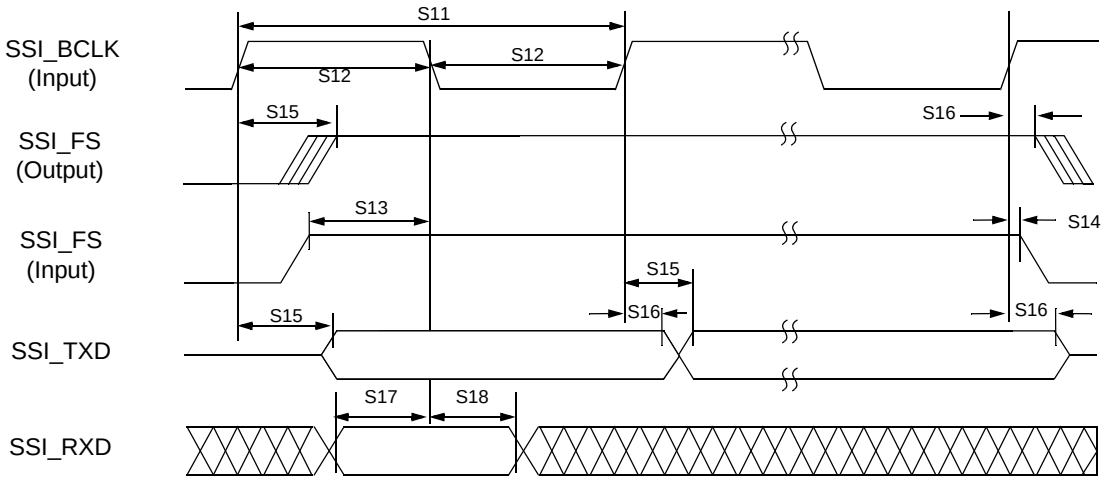

Figure 16. SSI Timing – Slave Modes

5.12 I²C Input/Output Timing Specifications

Table 16 lists specifications for the I²C input timing parameters shown in Figure 17.

Table 16. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

5.13 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at 5.0 V or 3.3 V.

5.13.1 MII Receive Signal Timing

The receiver functions correctly up to a FEC_RXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC_RXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RXDV, FEC_RXER to FEC_RXCLK setup	5	—	ns
M2	FEC_RXCLK to FEC_RXD[3:0], FEC_RXDV, FEC_RXER hold	5	—	ns
M3	FEC_RXCLK pulse width high	35%	65%	FEC_RXCLK period
M4	FEC_RXCLK pulse width low	35%	65%	FEC_RXCLK period

Figure 18 shows MII receive signal timings listed in Table 18.

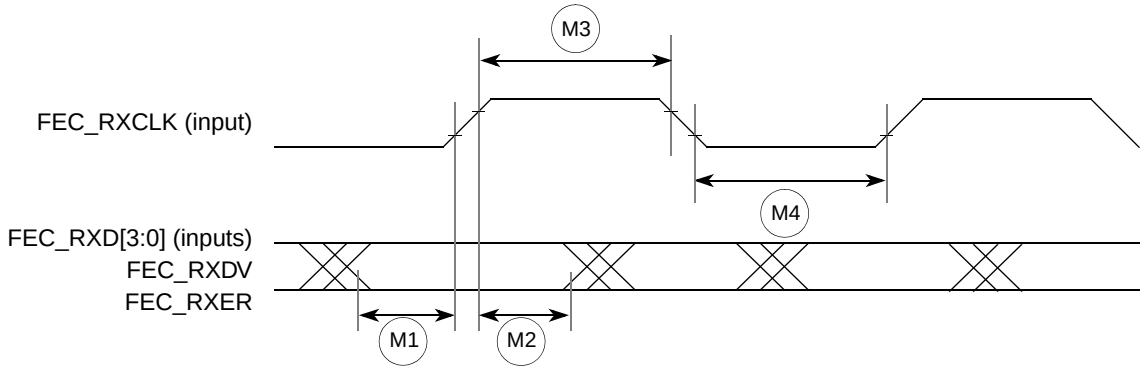

Figure 18. MII Receive Signal Timing Diagram

5.13.2 MII Transmit Signal Timing

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC_TXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC_TXCLK frequency.

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER invalid	5	—	ns
M6	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER valid	—	25	ns
M7	FEC_TXCLK pulse width high	35%	65%	FEC_TXCLK period
M8	FEC_TXCLK pulse width low	35%	65%	FEC_TXCLK period

Figure 19 shows MII transmit signal timings listed in Table 19.

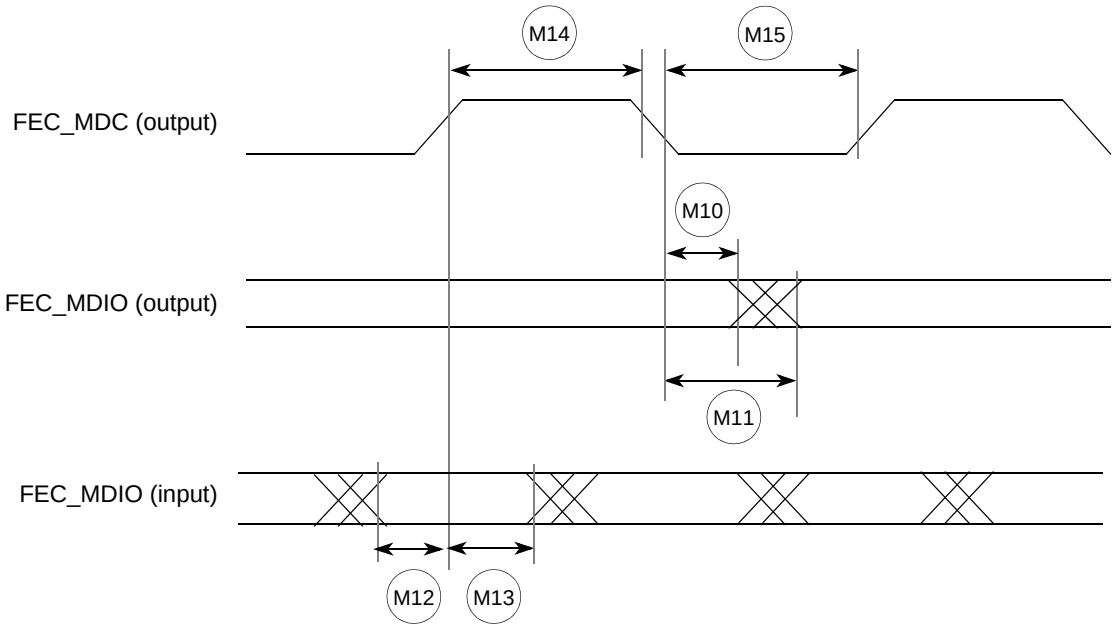

Figure 21. MII Serial Management Channel Timing Diagram

5.14 32-Bit Timer Module Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.15 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

8 Revision History

Table 28. MCF5373DS Document Revision History

Rev. No.	Substantive Changes	Date of Release
0	• Initial release	11/2005
0.1	• Swapped pin locations PLL_VSS (J11->H11) and DRAMSEL (H11->J11) in Table 1. Figure 4 is correct.	12/2005
0.2	• Added not to Section 7, “Package Information.” • Added “top view” and “bottom view” where appropriate in mechanical drawings and pinout figures. • Figure 6: Corrected “FB_CLK (75MHz)” label to “FB_CLK (80MHz)”	3/2006
0.3	• Changed 160QFP pinouts in Figure 5 and Table 2: Removed IRQ3 pin, shifted pins 89–99 up one pin to 90–100. Pin 89 is now VSS. • Table 2: Rearranged GPIO signal names for FEC pins. • Removed ULPI specifications as the device does not support ULPI.	4/2006
1	• Updated thermal characteristic values in Table 7. • Updated DC electricals values in Table 7. • Updated Section 3.3, “Supply Voltage Sequencing and Separation Cautions” and subsections. • Updated and added Oscillator/PLL characteristics in Table 8. • Table 9: Swapped min/max for FB1; Removed FB8 & FB9. • Updated SDRAM write timing diagram, Figure 9. • Table 11: Added values for frequency of operation and DD1. • Replaced figure & table Section 5.11, “SSI Timing Specifications,” with slave & master mode versions. • Removed second sentence from Section 5.13.2, “MII Transmit Signal Timing,” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 5.13.2, “MII Transmit Signal Timing,” as this feature is not supported on this device. • Updated figure & table Section 5.17, “Debug AC Timing Specifications.” • Renamed & moved previous version’s Section 5.5 “Power Consumption” to Section 6, “Current Consumption.” Added additional real-world data to this section as well.	7/2007
2	• Added MCF53721 device information throughout: features list, family configuration table, ordering information table, signals description table, and relevant package diagram titles • Remove Footnote 1 from Table 11. • Changed document type from Advance Information to Technical Data.	8/2007