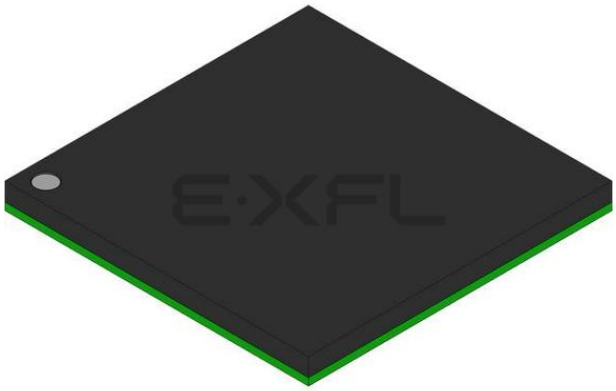

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5372lcvm240j

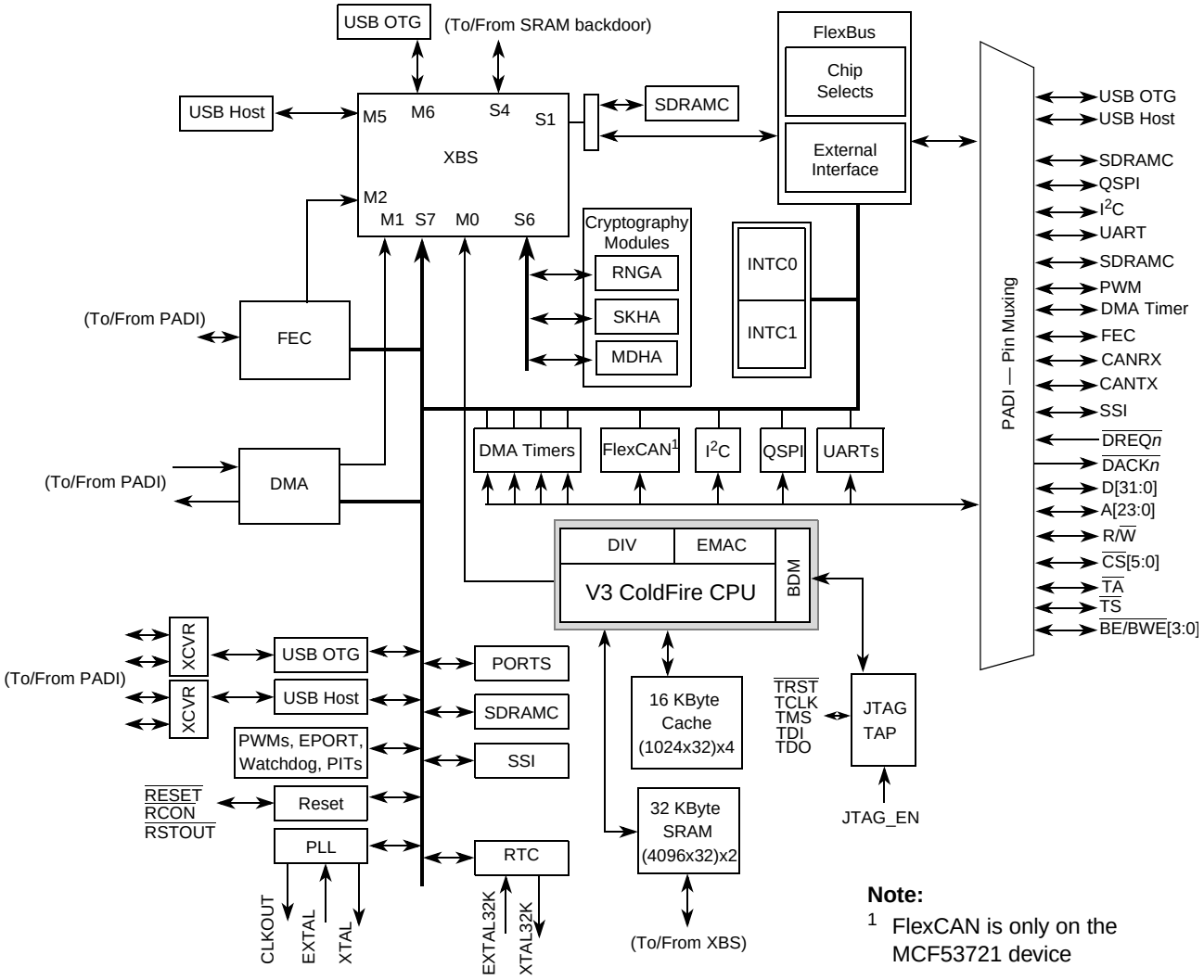


Figure 1. MCF5373 Block Diagram

1 MCF537*x* Family Comparison

The following table compares the various device derivatives available within the MCF537*x* family.

Table 1. MCF537*x* Family Configurations

Module	MCF5372	MCF5372L	MCF53721	MCF5373	MCF5373L
ColdFire Version 3 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•
Core (System) Clock	up to 180 MHz	up to 240 MHz		up to 180 MHz	up to 240 MHz
Peripheral and External Bus Clock (Core clock ÷ 3)	up to 60 MHz	up to 80 MHz		up to 60 MHz	up to 80 MHz
Performance (Dhrystone/2.1 MIPS)	up to 158	up to 211		up to 158	up to 211
Instruction/Data Cache	16 Kbytes				

Table 1. MCF537*x* Family Configurations (continued)

Module	MCF5372	MCF5372L	MCF53721	MCF5373	MCF5373L
Static RAM (SRAM)	32 Kbytes				
SDR/DDR SDRAM Controller	•	•	•	•	•
USB 2.0 Host	—	•	•	—	•
USB 2.0 On-the-Go	—	•	•	—	•
Synchronous Serial Interface (SSI)	•	•	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•
Cryptography Hardware Accelerators	—	—	—	•	•
Embedded Voice-over-IP System Solution	—	—	•	—	—
FlexCAN 2.0B communication module	—	—	•	—	—
UARTs	3	3	3	3	3
I^2C	•	•	•	•	•
QSPI	•	•	•	•	•
PWM Module	—	•	•	—	•
Real Time Clock	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2	2
16-channel Direct Memory Access (DMA)	•	•	•	•	•
FlexBus External Interface	•	•	•	•	•
General Purpose I/O (GPIO)	up to 46	up to 62	up to 62	up to 46	up to 62
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•
Package	160 QFP	196 MAPBGA	196 MAPBGA	160 QFP	196 MAPBGA

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF5372CAB180	MCF5372 RISC Microprocessor	160 QFP	180 MHz	–40° to +85° C
MCF5372LCVM240	MCF5372 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C
MCF53721CVM240	MCF53721 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C
MCF5373CAB180	MCF5373 RISC Microprocessor	160 QFP	180 MHz	–40° to +85° C
MCF5373LCVM240	MCF5373 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
USB Host & USB On-the-Go							
USBOTG_M	—	—	—	I/O	USB VDD	—	H14
USBOTG_P	—	—	—	I/O	USB VDD	—	H13
USBHOST_M	—	—	—	I/O	USB VDD	—	J13
USBHOST_P	—	—	—	I/O	USB VDD	—	J12
FlexCAN (MCF53721 only)							
CANRX and CANTX do not have dedicated bond pads. Please refer to the following pins for muxing: I2C_SDA for CANRX and I2C_SCL for CANTX.							
PWM							
PWM7	PPWM7	—	—	I/O	EVDD	—	E13
PWM5	PPWM5	—	—	I/O	EVDD	—	E12
PWM3	PPWM3	DT3OUT	DT3IN	I/O	EVDD	—	E11
PWM1	PPWM1	DT2OUT	DT2IN	I/O	EVDD	—	F14
SSI							
The SSI signals do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{IRQ4}}$ for SSI_MCLK, $\overline{\text{IRQ1}}$ for SSI_CLKIN, $\overline{\text{U1CTS}}$ for SSI_BCLK, $\overline{\text{U1RTS}}$ for SSI_FS, U1RXD for SSI_RXD, and U1TXD for SSI_TXD							
I²C							
I2C_SCL[2]	PFECI2C1	CANTX[6]	U2TXD	I/O	EVDD	—	E3
I2C_SDA[2]	PFECI2C0	CANRX[6]	U2RXD	I/O	EVDD	—	E4
DMA							
$\overline{\text{DACK}}$[1:0] and $\overline{\text{DREQ}}$[1:0] do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ for $\overline{\text{DACK0}}$, DT0IN for $\overline{\text{DREQ0}}$, DT1IN for $\overline{\text{DACK1}}$, and $\overline{\text{IRQ1}}$ for $\overline{\text{DREQ1}}$.							
QSPI							
QSPI_CS2	PQSPI5	$\overline{\text{U2RTS}}$	—	O	EVDD	78	N12
QSPI_CS1	PQSPI4	PWM7	USBOTG_PU_EN	O	EVDD	—	M12
QSPI_CS0	PQSPI3	PWM5	—	O	EVDD	—	M11
QSPI_CLK	PQSPI2	I2C_SCL[2]	—	O	EVDD	77	P12
QSPI_DIN	PQSPI1	$\overline{\text{U2CTS}}$	—	I	EVDD	75	P11
QSPI_DOUT	PQSPI0	I2C_SDA[2]	—	O	EVDD	76	N11

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5373 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5373.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. However, for production silicon, these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	– 0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	– 0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	– 0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to +85	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

1 Functional operating conditions are given in Section 5.4, “DC Electrical Specifications.” Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 5. Thermal Characteristics

Characteristic		Symbol	256MBGA	196MBGA	160QFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	37[1,2]	42[1,2]	49[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	34[1,2]	38[1,2]	44[1,2]	°C/W
Junction to board		θ_{JB}	27[3]	32[3]	40[3]	°C/W
Junction to case		θ_{JC}	16[4]	19[4]	39[4]	°C/W
Junction to top of package		Ψ_{jt}	4[1,5]	5[1,5]	12[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = P_{INT} + $P_{I/O}$
P_{INT} = I_{DD} × IV_{DD}, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

* The timings are also valid for inputs sampled on the negative clock edge.

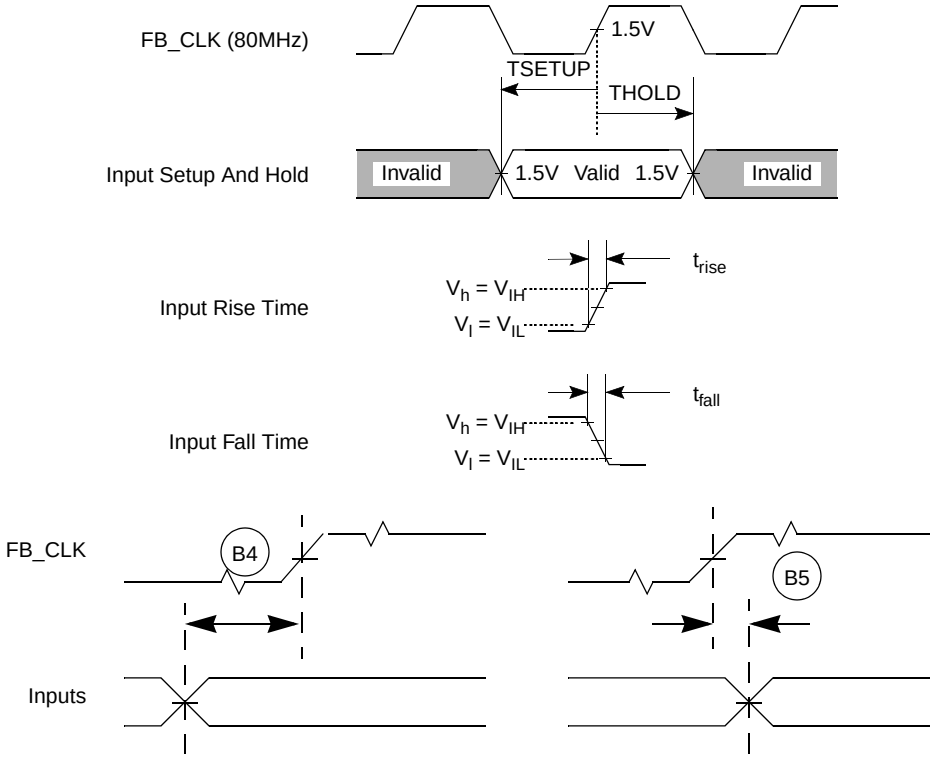


Figure 6. General Input Timing Requirements

5.6.1 FlexBus

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{FB\_CS}$[5:0]) which can be configured to be distributed between the FlexBus or SDRAM memory interfaces. Chip-select, $\overline{FB\_CS0}$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM/flash memories.

5.6.1.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the system clock.

Table 9. FlexBus AC Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit
—	Frequency of Operation	$f_{sys/3}$	—	80	Mhz
FB1	Clock Period (FB_CLK)	t_{FBCK} (t_{cyc})	12.5	—	ns
FB2	Address, Data, and Control Output Valid (A[23:0], D[31:0], $\overline{FB\_CS}$[5:0], R/$\overline{W}$, $\overline{TS}$, $\overline{BE/BWE}$[3:0] and $\overline{OE}$)[1]	$t_{FBCHDCV}$	—	7.0	ns
FB3	Address, Data, and Control Output Hold (A[23:0], D[31:0], $\overline{FB\_CS}$[5:0], R/$\overline{W}$, $\overline{TS}$, $\overline{BE/BWE}$[3:0], and $\overline{OE}$)[1, 2]	$t_{FBCHDCI}$	1	—	ns

Table 9. FlexBus AC Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
FB4	Data Input Setup	t_{DVFBCH}	3.5	—	ns
FB5	Data Input Hold	t_{DIFBCH}	0	—	ns
FB6	Transfer Acknowledge ($\overline{TA}$) Input Setup	t_{CVFBCH}	4	—	ns
FB7	Transfer Acknowledge ($\overline{TA}$) Input Hold	t_{CIFBCH}	0	—	ns

1 Timing for chip selects only applies to the $\overline{FB\_CS}$[5:0] signals. Please see Section 5.7.2, "DDR SDRAM AC Timing Characteristics" for SD_CS[3:0] timing.

2 The FlexBus supports programming an extension of the address hold. Please consult the *Reference Manual* for more information.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

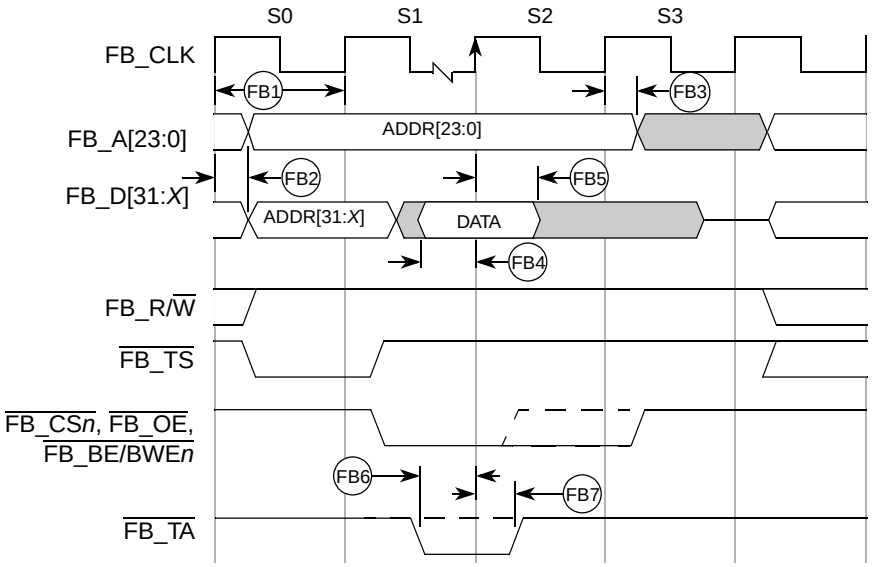


Figure 7. FlexBus Read Timing

Table 10. SDR Timing Specifications (continued)

Symbol	Characteristic	Symbol	Min	Max	Unit
SD9	SD_DQS[3:2] input hold relative to SD_CLK[7]	$t_{DQISDCH}$	Does not apply. 0.5×SD_CLK fixed width.		
SD10	Data (D[31:0]) Input Setup relative to SD_CLK (reference only)[8]	t_{DVSDCH}	0.25 × SD_CLK	—	ns
SD11	Data Input Hold relative to SD_CLK (reference only)	t_{DISDCH}	1.0	—	ns
SD12	Data (D[31:0]) and Data Mask(SD_DQM[3:0]) Output Valid	$t_{SDCHDMV}$	—	0.75 × SD_CLK + 0.5	ns
SD13	Data (D[31:0]) and Data Mask (SD_DQM[3:0]) Output Hold	$t_{SDCHDMI}$	1.5	—	ns

1 The FlexBus and SDRAM clock operates at the same frequency of the internal bus clock. See the PLL chapter of the *MCF5373 Reference Manual* for more information on setting the SDRAM clock rate.

2 SD_CLK is one SDRAM clock in (ns).

3 Pulse width high plus pulse width low cannot exceed min and max clock period.

4 Pulse width high plus pulse width low cannot exceed min and max clock period.

5 SD_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SD_DQS only pulses during a read cycle and one pulse occurs for each data beat.

6 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS only pulses during a read cycle and one pulse occurs for each data beat.

7 The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.

8 Because a read cycle in SDR mode uses the DQS circuit within the device, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens results in successful SDR reads. The input setup spec is provided as guidance.

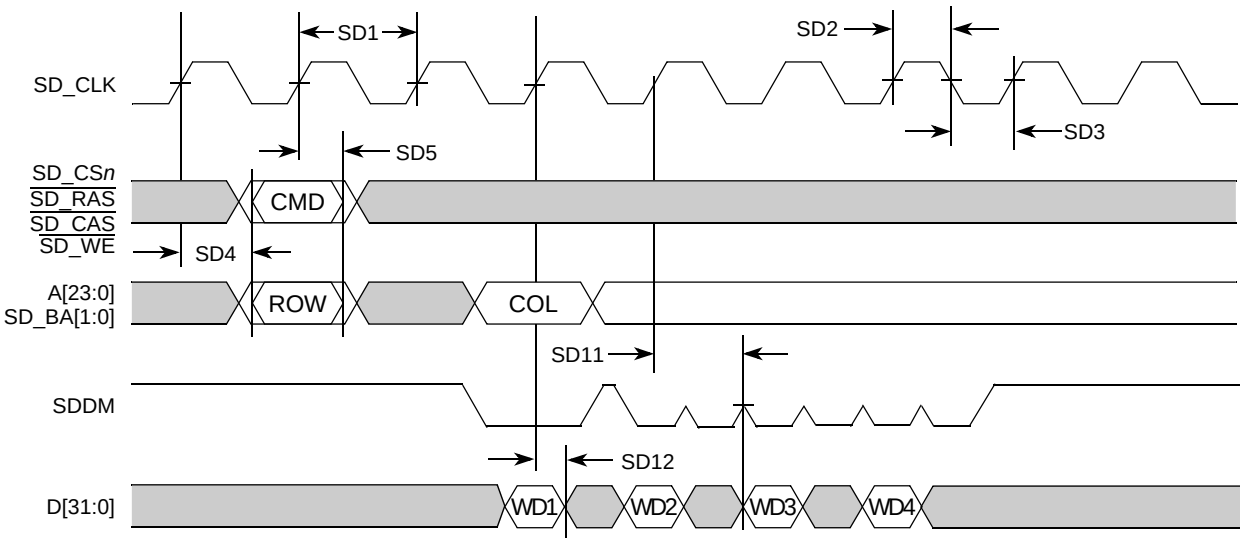


Figure 9. SDR Write Timing

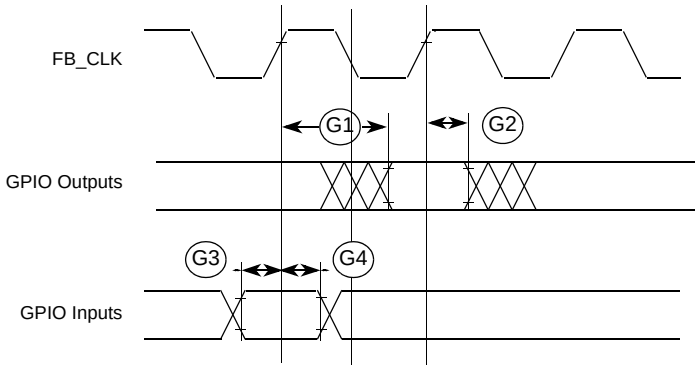


Figure 13. GPIO Timing

5.9 Reset and Configuration Override Timing

Table 13. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

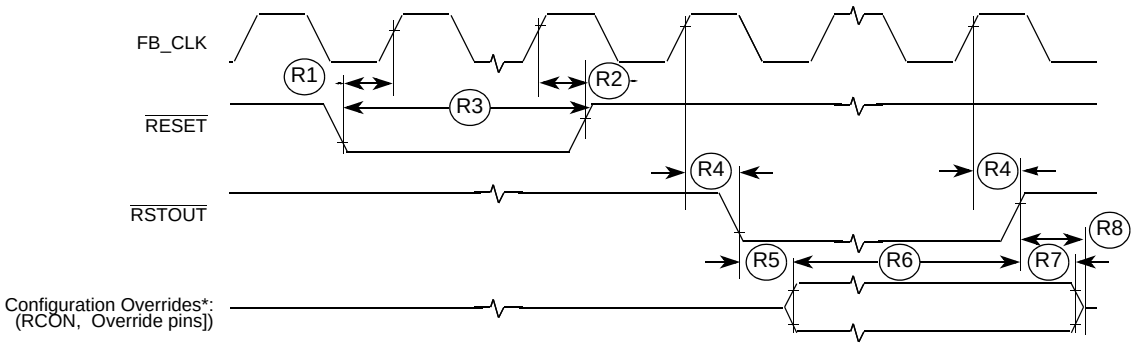


Figure 14. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF5373 Reference Manual* for more information.

5.10 USB On-The-Go

The MCF5373 device is compliant with industry standard USB 2.0 specification.

5.11 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 14. SSI Timing – Master Modes[1]

Num	Description	Symbol	Min	Max	Units
S1	SSI_MCLK cycle time[2]	t_{MCLK}	$8 \times t_{SYS}$	—	ns
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}
S3	SSI_BCLK cycle time[3]	t_{BCLK}	$8 \times t_{SYS}$	—	ns
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}
S5	SSI_BCLK to SSI_FS output valid		—	15	ns
S6	SSI_BCLK to SSI_FS output invalid		-2	—	ns
S7	SSI_BCLK to SSI_TXD valid		—	15	ns
S8	SSI_BCLK to SSI_TXD invalid / high impedence		-4	—	ns
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		15	—	ns
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns

1 All timings specified with a capactive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (SYSCLK).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of SYSCLK. If the SYSCLK is used, the minimum divider is 6. If the SSI_CLKIN input is used, the programmable dividers must be set to ensure that SSI_BCLK does not exceed 4 x f_{SYS}.

Table 15. SSI Timing – Slave Modes[1]

Num	Description	Symbol	Min	Max	Units
S11	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns
S12	SSI_BCLK pulse width high/low		45%	55%	t_{BCLK}
S13	SSI_FS input setup before SSI_BCLK		10	—	ns
S14	SSI_FS input hold after SSI_BCLK		3	—	ns
S15	SSI_BCLK to SSI_TXD/SSI_FS output valid		—	15	ns
S16	SSI_BCLK to SSI_TXD/SSI_FS output invalid/high impedence		-2	—	ns
S17	SSI_RXD setup before SSI_BCLK		10	—	ns
S18	SSI_RXD hold after SSI_BCLK		3	—	ns

1 All timings specified with a capactive load of 25pF.

Table 16. I²C Input Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Units
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 17 lists specifications for the I²C output timing parameters shown in Figure 17.

Table 17. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 17. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 17 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 17 shows timing for the values in Table 17 and Table 16.

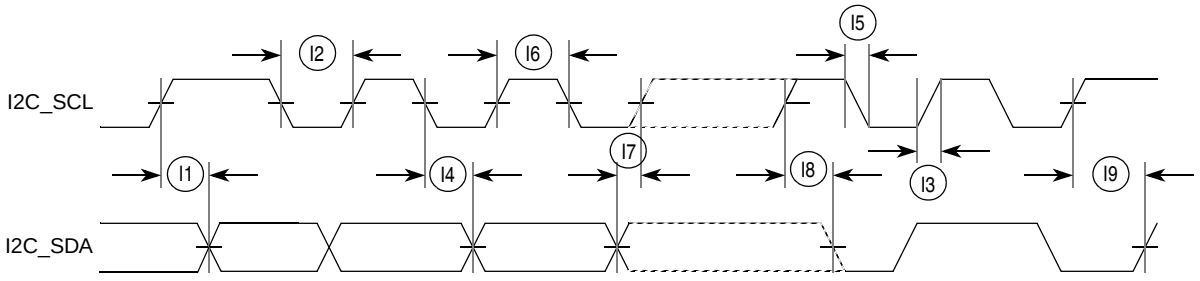


Figure 17. I²C Input/Output Timings

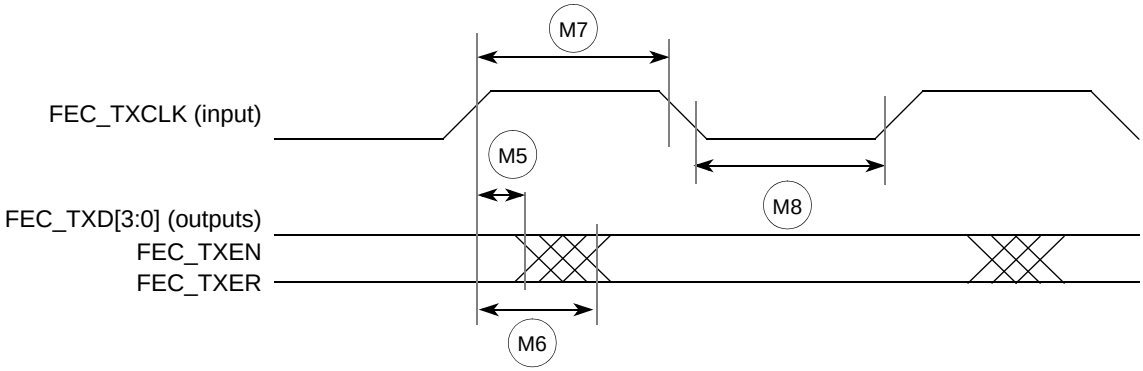


Figure 19. MII Transmit Signal Timing Diagram

5.13.3 MII Async Inputs Signal Timing

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TXCLK period

Figure 20. MII Async Inputs Timing Diagram

5.13.4 MII Serial Management Channel Timing

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max prop delay)	—	25	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	10	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

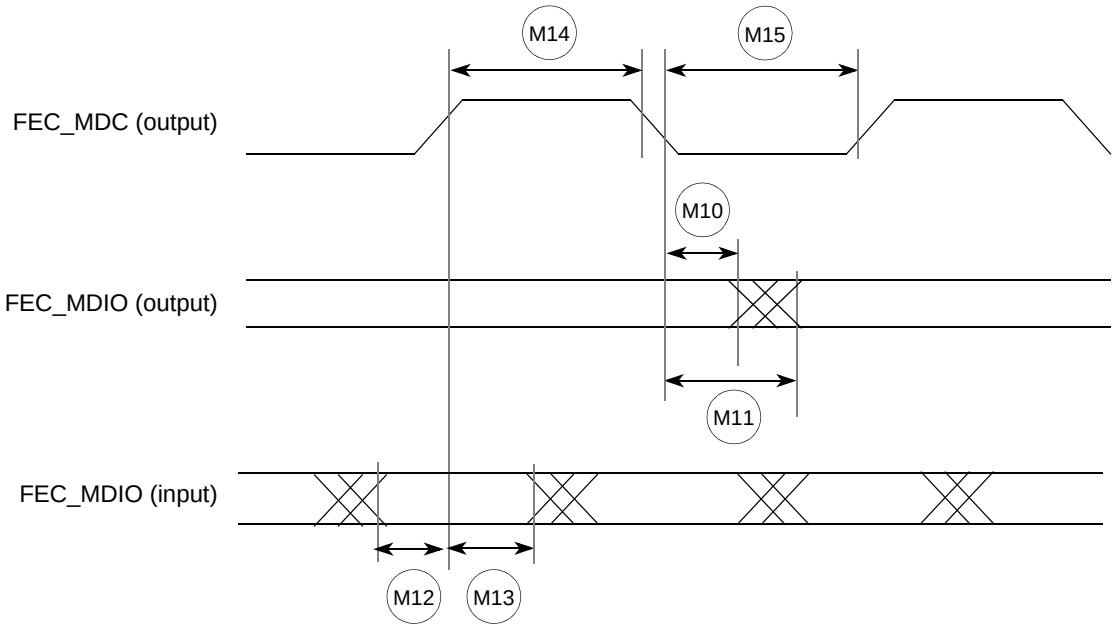


Figure 21. MII Serial Management Channel Timing Diagram

5.14 32-Bit Timer Module Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.15 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

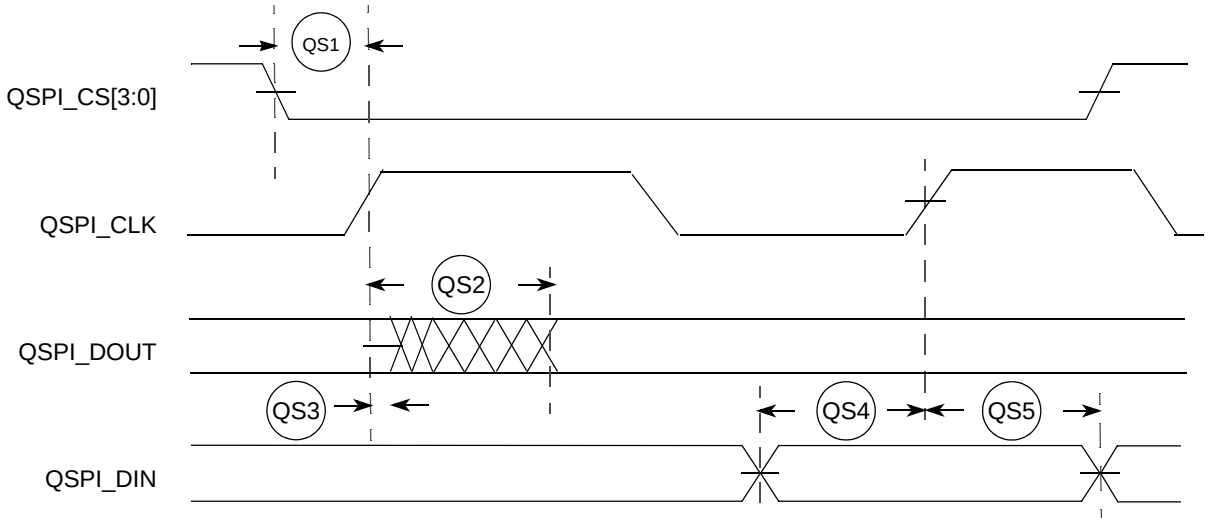


Figure 22. QSPI Timing

5.16 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/3}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

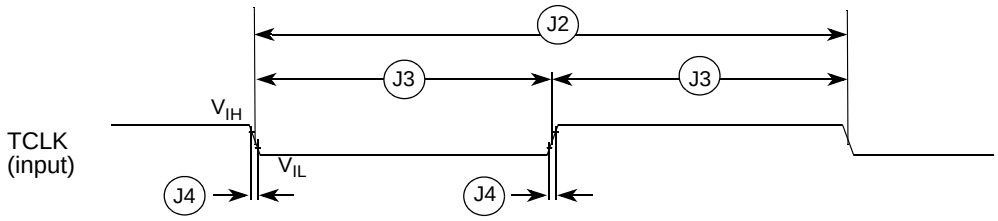


Figure 23. Test Clock Input Timing

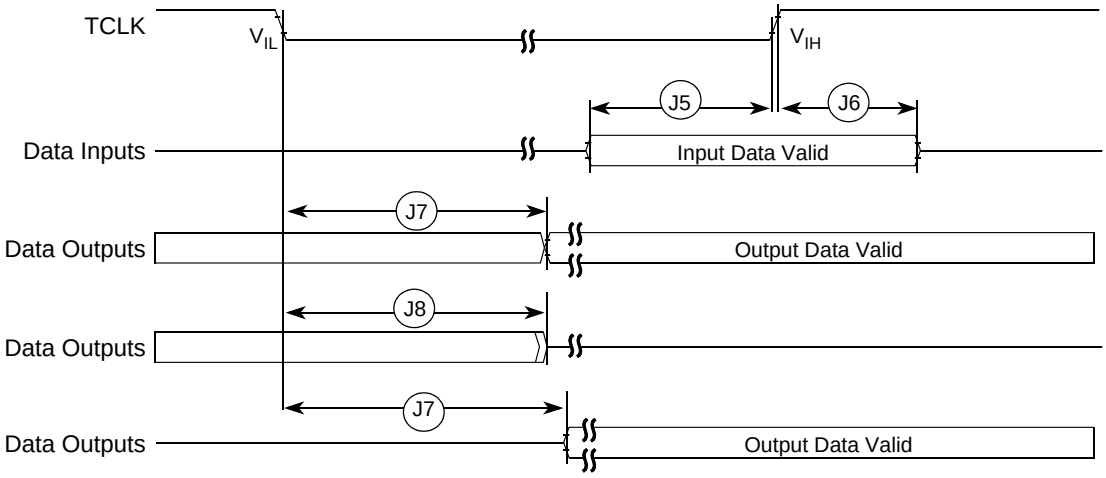


Figure 24. Boundary Scan (JTAG) Timing

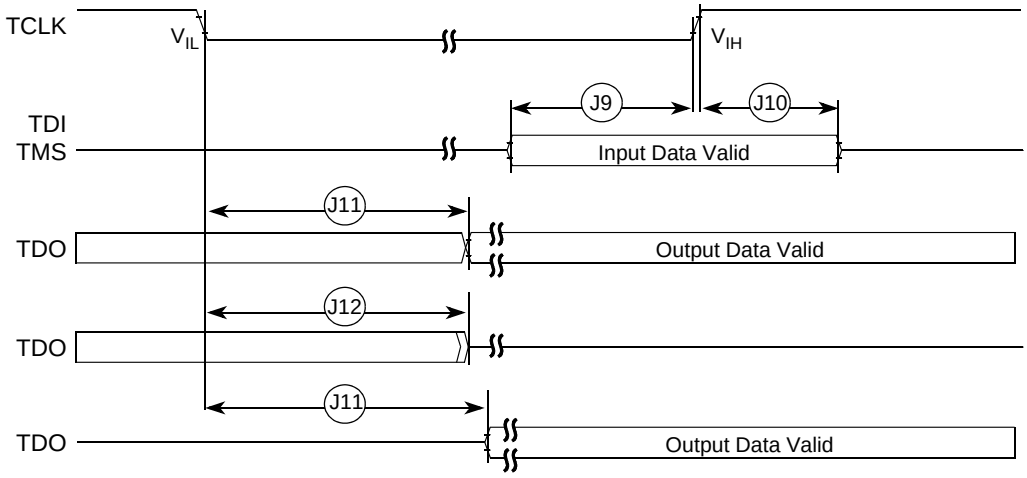


Figure 25. Test Access Port Timing

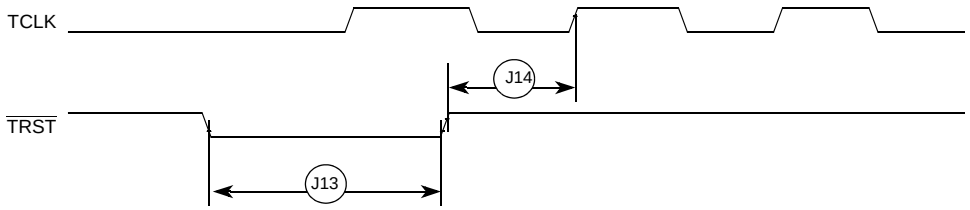


Figure 26. $\overline{\text{TRST}}$ Timing

5.17 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 27.

Table 25. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	2	2	$t_{SYS} = 1/f_{SYS}$
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

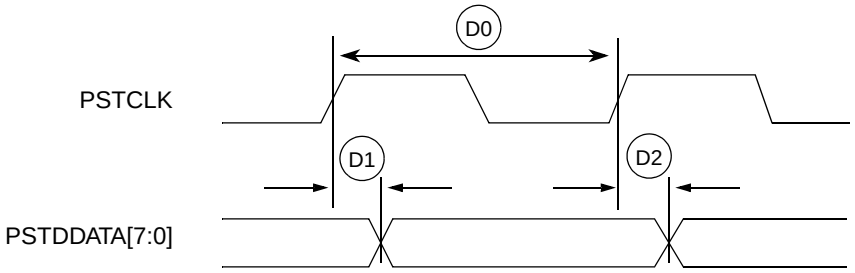


Figure 27. Real-Time Trace AC Timing

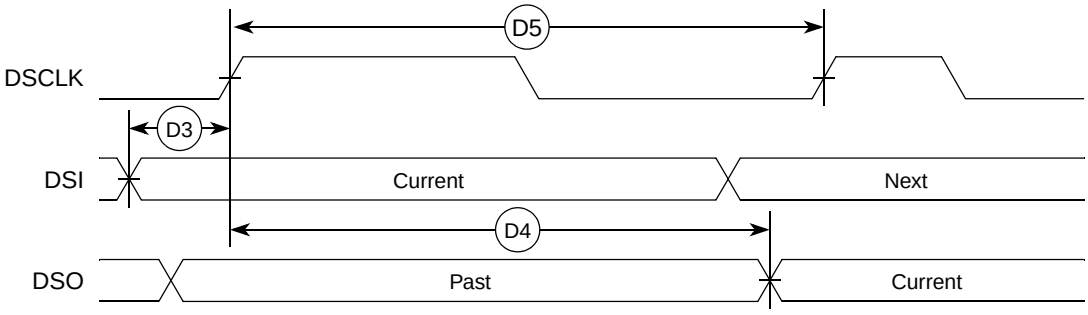


Figure 28. BDM Serial Port AC Timing

6 Current Consumption

All current consumption data is lab data measured on a single device using an evaluation board. Table 26 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

7.1 Package Dimensions—196 MAPBGA

Figure 31 shows the MCF5373LCVM240, MCF5372LCVM240, and MCF53721CVM240 package dimensions.

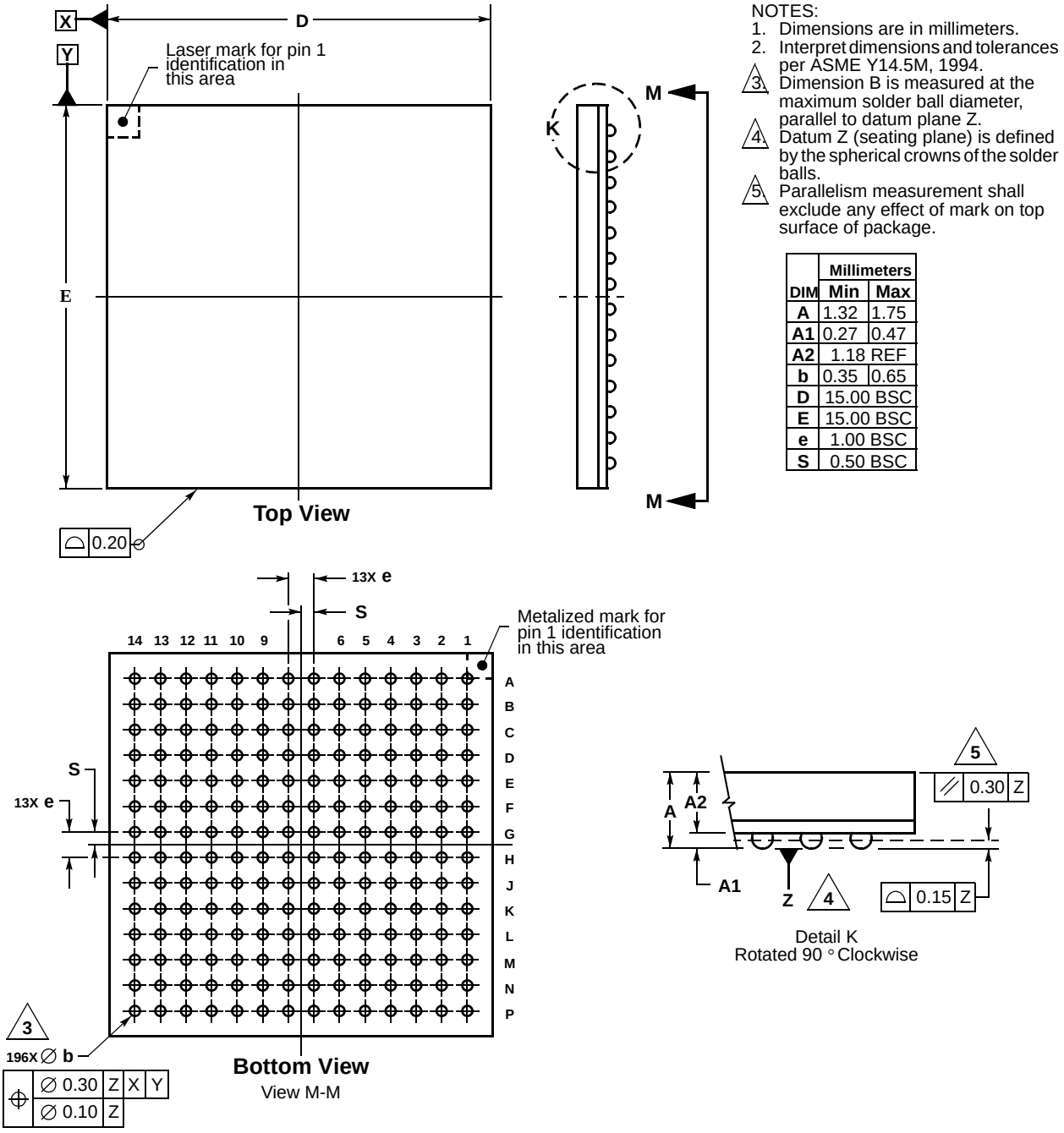
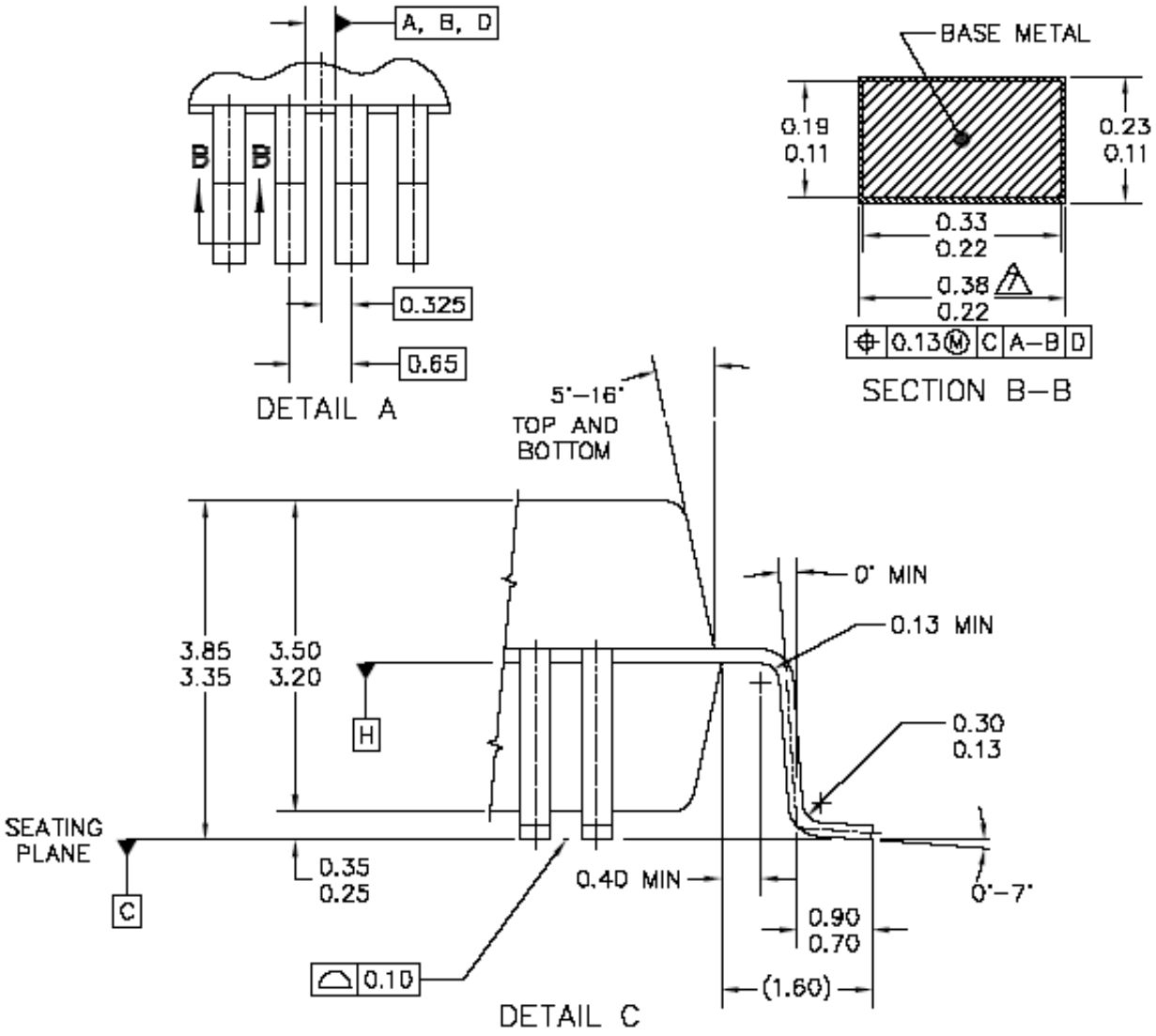


Figure 31. 196 MAPBGA Package Dimensions (Case No. 1128A-01)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

Figure 33. 160QFP Package Dimensions (Sheet 2 of 2)

8 Revision History

Table 28. MCF5373DS Document Revision History

Rev. No.	Substantive Changes	Date of Release
0	• Initial release	11/2005
0.1	• Swapped pin locations PLL_VSS (J11->H11) and DRAMSEL (H11->J11) in Table 1. Figure 4 is correct.	12/2005
0.2	• Added not to Section 7, “Package Information.” • Added “top view” and “bottom view” where appropriate in mechanical drawings and pinout figures. • Figure 6: Corrected “FB_CLK (75MHz)” label to “FB_CLK (80MHz)”	3/2006
0.3	• Changed 160QFP pinouts in Figure 5 and Table 2: Removed IRQ3 pin, shifted pins 89–99 up one pin to 90–100. Pin 89 is now VSS. • Table 2: Rearranged GPIO signal names for FEC pins. • Removed ULPI specifications as the device does not support ULPI.	4/2006
1	• Updated thermal characteristic values in Table 7. • Updated DC electricals values in Table 7. • Updated Section 3.3, “Supply Voltage Sequencing and Separation Cautions” and subsections. • Updated and added Oscillator/PLL characteristics in Table 8. • Table 9: Swapped min/max for FB1; Removed FB8 & FB9. • Updated SDRAM write timing diagram, Figure 9. • Table 11: Added values for frequency of operation and DD1. • Replaced figure & table Section 5.11, “SSI Timing Specifications,” with slave & master mode versions. • Removed second sentence from Section 5.13.2, “MII Transmit Signal Timing,” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 5.13.2, “MII Transmit Signal Timing,” as this feature is not supported on this device. • Updated figure & table Section 5.17, “Debug AC Timing Specifications.” • Renamed & moved previous version’s Section 5.5 “Power Consumption” to Section 6, “Current Consumption.” Added additional real-world data to this section as well.	7/2007
2	• Added MCF53721 device information throughout: features list, family configuration table, ordering information table, signals description table, and relevant package diagram titles • Remove Footnote 1 from Table 11. • Changed document type from Advance Information to Technical Data.	8/2007