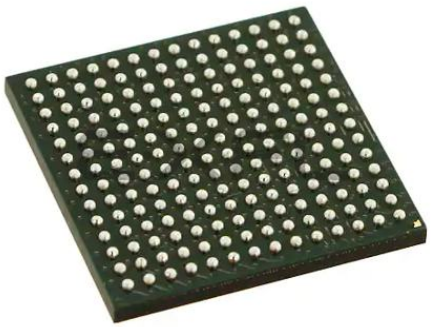

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5373lcvm240j

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Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
Mode Selection							
$\overline{\text{RCON}}$[2]	—	—	—	I	EVDD	72	P8
DRAMSEL	—	—	—	I	EVDD	92	J11
FlexBus							
A[23:22]	—	$\overline{\text{FB\_CS}}$[5:4]	—	O	SDVDD	134, 133	A9, B9
A[21:16]	—	—	—	O	SDVDD	132–127	C9, D9, A10, B10, C10, D10
A[15:14]	—	SD_BA[1:0][3]	—	O	SDVDD	126, 123	A11, B11
A[13:11]	—	SD_A[13:11][3]	—	O	SDVDD	120–118	C11, A12, B12
A10	—	—	—	O	SDVDD	11 7	A13
A[9:0]	—	SD_A[9:0][3]	—	O	SDVDD	116–107	A14, B14, B13, C12, D11, C14, C13, D14–D12
D[31:16]	—	SD_D[31:16][4]	—	I/O	SDVDD	27–34, 46–53	J2, J1, K4–K1, L4, L3, N2, P1, P2, N3, L5, P3, N4, P4
D[15:1]	—	FB_D[31:17][4]	—	I/O	SDVDD	16–23, 57–63	F2, F1, G4–G1, H4, H3, L6, M6, N6, P6, L7, M7, N7
D0[2]	—	FB_D[16][4]	—	I/O	SDVDD	64	P7
$\overline{\text{BE/BWE}}$[3:0]	PBE[3:0]	$\overline{\text{SD\_DQM}}$[3:0][3]	—	O	SDVDD	26, 54, 24, 56	J3, M5, H2, P5
$\overline{\text{OE}}$	PBUSCTL3	—	—	O	SDVDD	66	M8
$\overline{\text{TA}}$[2]	PBUSCTL2	—	—	I	SDVDD	106	E14
R/$\overline{\text{W}}$	PBUSCTL1	—	—	O	SDVDD	65	L8
$\overline{\text{TS}}$	PBUSCTL0	$\overline{\text{DACK0}}$	—	O	SDVDD	12	E2
Chip Selects							
$\overline{\text{FB\_CS}}$[5:4]	PCS[5:4]	—	—	O	SDVDD	—	D8, C8
$\overline{\text{FB\_CS}}$[3:2]	PCS[3:2]	—	—	O	SDVDD	—	B8, A8
$\overline{\text{FB\_CS1}}$	PCS1	—	—	O	SDVDD	135	D7
$\overline{\text{FB\_CS0}}$	—	—	—	O	SDVDD	136	C7
SDRAM Controller							
SD_A10	—	—	—	O	SDVDD	43	M2
SD_CKE	—	—	—	O	SDVDD	14	F4

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
SD_CLK	—	—	—	O	SDVDD	37	L1
$\overline{\text{SD\_CLK}}$	—	—	—	O	SDVDD	38	M1
$\overline{\text{SD\_CS0}}$	—	—	—	O	SDVDD	15	F3
SD_DQS3	—	—	—	O	SDVDD	25	H1
SD_DQS2	—	—	—	O	SDVDD	55	N5
$\overline{\text{SD\_SCAS}}$	—	—	—	O	SDVDD	44	M3
$\overline{\text{SD\_SRAS}}$	—	—	—	O	SDVDD	45	M4
SD_SDR_DQS	—	—	—	O	SDVDD	35	L2
$\overline{\text{SD\_WE}}$	—	—	—	O	SDVDD	13	E1
External Interrupts Port[5]							
$\overline{\text{IRQ7}}$[2]	PIRQ7[2]	—	—	I	EVDD	102	F13
$\overline{\text{IRQ6}}$[2]	PIRQ6[2]	USBHOST_ VBUS_EN	—	I	EVDD	—	F12
$\overline{\text{IRQ5}}$[2]	PIRQ5[2]	USBHOST_ VBUS_OC	—	I	EVDD	—	F11
$\overline{\text{IRQ4}}$[2]	PIRQ4[2]	SSI_MCLK	—	I	EVDD	101	G14
$\overline{\text{IRQ3}}$[2]	PIRQ3[2]	—	—	I	EVDD	—	G13
$\overline{\text{IRQ2}}$[2]	PIRQ2[2]	USB_CLKIN	—	I	EVDD	—	G12
$\overline{\text{IRQ1}}$[2]	PIRQ1[2]	$\overline{\text{DREQ1}}$[2]	SSI_CLKIN	I	EVDD	100	G11
FEC							
FEC_MDC	PFECI2C3	I2C_SCL[2]	—	O	EVDD	4	B1
FEC_MDIO	PFECI2C2	I2C_SDA[2]	—	I/O	EVDD	3	A1
FEC_COL	PFECH7	—	—	I	EVDD	144	B6
FEC_CRS	PFECH6	—	—	I	EVDD	145	A6
FEC_RXCLK	PFECH5	—	—	I	EVDD	146	A5
FEC_RXDV	PFECH4	—	—	I	EVDD	147	B5
FEC_RXD[3:0]	PFECH[3:0]	—	—	I	EVDD	148–151	C5, D5, A4, B4
FEC_RXER	PFECL7	—	—	I	EVDD	152	C4
FEC_TXCLK	PFECL6	—	—	I	EVDD	153	A3
FEC_TXEN	PFECL5	—	—	O	EVDD	154	B3
FEC_TXER	PFECL4	—	—	O	EVDD	155	A2
FEC_TXD[3:0]	PFECL[3:0]	—	—	O	EVDD	157, 158, 1, 2	D4, C3, B2, C2

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
USB Host & USB On-the-Go							
USBOTG_M	—	—	—	I/O	USB VDD	—	H14
USBOTG_P	—	—	—	I/O	USB VDD	—	H13
USBHOST_M	—	—	—	I/O	USB VDD	—	J13
USBHOST_P	—	—	—	I/O	USB VDD	—	J12
FlexCAN (MCF53721 only)							
CANRX and CANTX do not have dedicated bond pads. Please refer to the following pins for muxing: I2C_SDA for CANRX and I2C_SCL for CANTX.							
PWM							
PWM7	PPWM7	—	—	I/O	EVDD	—	E13
PWM5	PPWM5	—	—	I/O	EVDD	—	E12
PWM3	PPWM3	DT3OUT	DT3IN	I/O	EVDD	—	E11
PWM1	PPWM1	DT2OUT	DT2IN	I/O	EVDD	—	F14
SSI							
The SSI signals do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{IRQ4}}$ for SSI_MCLK, $\overline{\text{IRQ1}}$ for SSI_CLKIN, $\overline{\text{U1CTS}}$ for SSI_BCLK, $\overline{\text{U1RTS}}$ for SSI_FS, U1RXD for SSI_RXD, and U1TXD for SSI_TXD							
I²C							
I2C_SCL[2]	PFECI2C1	CANTX[6]	U2TXD	I/O	EVDD	—	E3
I2C_SDA[2]	PFECI2C0	CANRX[6]	U2RXD	I/O	EVDD	—	E4
DMA							
$\overline{\text{DACK}}$[1:0] and $\overline{\text{DREQ}}$[1:0] do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ for $\overline{\text{DACK0}}$, DT0IN for $\overline{\text{DREQ0}}$, DT1IN for $\overline{\text{DACK1}}$, and $\overline{\text{IRQ1}}$ for $\overline{\text{DREQ1}}$.							
QSPI							
QSPI_CS2	PQSPI5	$\overline{\text{U2RTS}}$	—	O	EVDD	78	N12
QSPI_CS1	PQSPI4	PWM7	USBOTG_PU_EN	O	EVDD	—	M12
QSPI_CS0	PQSPI3	PWM5	—	O	EVDD	—	M11
QSPI_CLK	PQSPI2	I2C_SCL[2]	—	O	EVDD	77	P12
QSPI_DIN	PQSPI1	$\overline{\text{U2CTS}}$	—	I	EVDD	75	P11
QSPI_DOUT	PQSPI0	I2C_SDA[2]	—	O	EVDD	76	N11

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
Test							
TEST[8]	—	—	—	I	EVDD	124	E10
Power Supplies							
EVDD	—	—	—	—	—	9, 69, 71, 81, 94, 103, 139, 160	E6, E7, F5–F7, G5, H10, J8, K8–K9
IVDD	—	—	—	—	—	36, 79, 97, 125, 156	E5, J9, K5, K10
PLL_VDD	—	—	—	—	—	99	J10
SD_VDD	—	—	—	—	—	11, 39, 41, 67, 105, 121, 137	E8–E9, F8–F10, J4–J7, H5, K6, K7
USB_VDD	—	—	—	—	—	—	H12
VSS	—	—	—	—	—	10, 42, 68, 82, 89, 104, 122, 138, 159	G6–G9, H6–H9
PLL_VSS	—	—	—	—	—	98	H11
USB_VSS	—	—	—	—	—	—	J14

1 Refers to pin's primary function.

2 Pull-up enabled internally on this signal for this mode.

3 The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.

4 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.

5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

6 MCF53721 only.

7 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

8 Pull-down enabled internally on this signal for this mode.

NOTE

4.2 Pinout—196 MAPBGA

The pinout for the MCF5373LCVM240, MCF5372LCVM240, and MCF53721CVM240 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	FEC_ MDIO	FEC_ TXER	FEC_ TXCLK	FEC_ RXD1	FEC_ RXCLK	FEC_ CRS	U1TXD	FB_CS2	A23	A19	A15	A12	A10	A9	A
B	FEC_ MDC	FEC_ TXD1	FEC_ TXEN	FEC_ RXD0	FEC_ RXDV	FEC_ COL	U1RXD	FB_CS3	A22/	A18	A14	A11	A7	A8	B
C	DT2IN	FEC_ TXD0	FEC_ TXD2	FEC_ RXER	FEC_ RXD3	U1CTS	FB_CS0	FB_CS4	A21	A17	A13	A6	A3	A4	C
D	DT3IN	DT1IN	DT0IN	FEC_ TXD3	FEC_ RXD2	U1RTS	FB_CS1	FB_CS5	A20	A16	A5	A0	A1	A2	D
E	SD_WE	TS	I2C_SCL	I2C_SDA	IVDD	EVDD	EVDD	SD_VDD	SD_VDD	TEST	PWM3	PWM5	PWM7	TA	E
F	D14	D15	SD_CS0	SD_CKE	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	IRQ5	IRQ6	IRQ7	PWM1	F
G	D10	D11	D12	D13	EVDD	VSS	VSS	VSS	VSS	JTAG_ EN	IRQ1	IRQ2	IRQ3	IRQ4	G
H	SD_ DQS3	BE/ BWE1	D8	D9	SD_VDD	VSS	VSS	VSS	VSS	EVDD	PLL_ VSS	USBOTG _VDD	USB OTG_P	USB OTG_M	H
J	D30	D31	BE/ BWE3	SD_VDD	SD_VDD	SD_VDD	SD_VDD	EVDD	IVDD	PLL_ VDD	DRAM SEL	USB HOST_P	USB HOST_M	USBHOST _VSS	J
K	D26	D27	D28	D29	IVDD	SD_VDD	SD_VDD	EVDD	EVDD	IVDD	TRST/ DSCLK	TDI/DSI	RESET	XTAL	K
L	SD_CLK	SD_DR_ DQS	D24	D25	D19	D7	D3	R/W	DDATA3	PST3	TDO/ DSO	RSTOUT	TMS/ BKPT	EXTAL	L
M	SD_CLK	SD_A10	SD_CAS	SD_RAS	BE/ BWE2	D6	D2	OE	DDATA2	PST2	QSPI_ CS0	QSPI_ CS1	U0RTS	U0CTS	M
N	FB_CLK	D23	D20	D17	SD_ DQS2	D5	D1	TCLK/ PSTCLK	DDATA1	PST1	QSPI_ DOUT	QSPI_ CS2	XTAL 32K	U0TXD	N
P	D22	D21	D18	D16	BE/ BWE0	D4	D0	RCON	DDATA0	PST0	QSPI_ DIN	QSPI_ CLK	EXTAL 32K	U0RXD	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 4. MCF5373LCVM240, MCF5372LCVM240, and MCF53721CVM240 Pinout Top View (196 MAPBGA)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5373 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5373.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. However, for production silicon, these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	– 0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	– 0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	– 0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to +85	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

1 Functional operating conditions are given in Section 5.4, “DC Electrical Specifications.” Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

Table 8. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
14	Discrete load capacitance for EXTAL	C_{L_EXTAL}		$2*C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [7]	pF
17	CLKOUT Period Jitter, [3, 4, 7, 8, 9] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 10 TBD	 % $f_{sys/3}$ % $f_{sys/3}$
18	Frequency Modulation Range Limit [3, 10, 11] (f_{sys}Max must not be exceeded)	C_{mod}	0.8	2.2	%$f_{sys/3}$
19	VCO Frequency. $f_{vco} = (f_{ref} * PFD)/4$	f_{vco}	350	540	MHz

1 The maximum allowable input clock frequency when booting with the PLL enabled is 24MHz. For higher input clock frequencies the processor must boot in LIMP mode to avoid violating the maximum allowable CPU frequency.

2 All internal registers retain data at 0 Hz.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 This parameter is guaranteed by design rather than 100% tested.

6 This specification is the PLL lock time only and does not include oscillator start-up time.

7 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

10 Modulation percentage applies over an interval of 10 μs, or equivalently the modulation rate is 100 KHz.

11 Modulation range determined by hardware design.

5.6 External Interface Timing Characteristics

Table 9 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 9 are shown in Figure 7 and Figure 8.

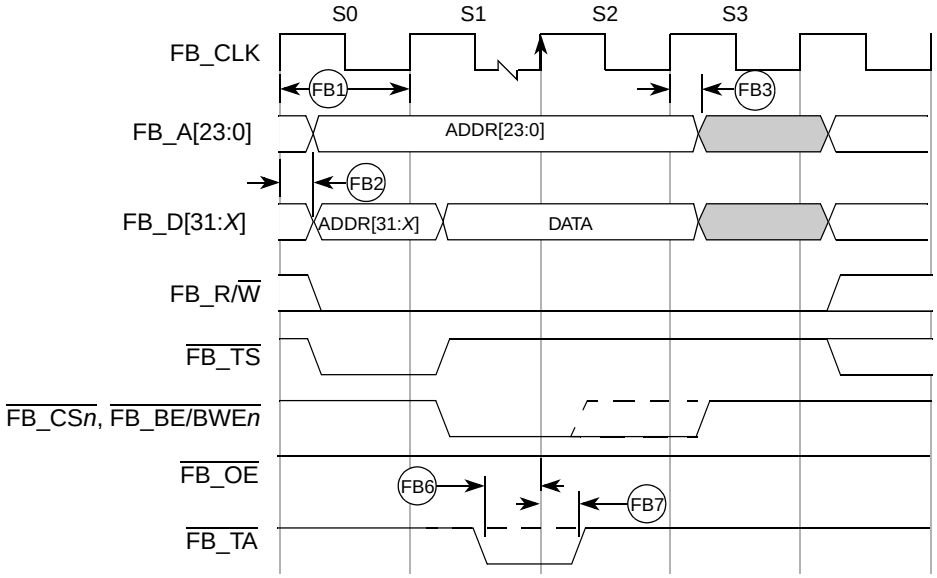


Figure 8. FlexBus Write Timing

5.7 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time.

5.7.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SD_DQS on read cycles. The device's SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must remain supplied to the device for each data beat of an SDR read. The processor accomplishes this by asserting a signal named SD_SDR_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SD_SDR_DQS signal and its usage.

Table 10. SDR Timing Specifications

Symbol	Characteristic	Symbol	Min	Max	Unit
•	Frequency of Operation[1]	•	60	80	MHz
SD1	Clock Period[2]	t_{SDCK}	12.5	16.67	ns
SD3	Pulse Width High[3]	t_{SDCKH}	0.45	0.55	SD_CLK
SD4	Pulse Width Low[4]	t_{SDCKH}	0.45	0.55	SD_CLK
SD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns
SD6	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns
SD7	SD_SDR_DQS Output Valid[5]	t_{DQSOV}	—	Self timed	ns
SD8	SD_DQS[3:0] input setup relative to SD_CLK[6]	$t_{DQVSDCH}$	0.25 × SD_CLK	0.40 × SD_CLK	ns

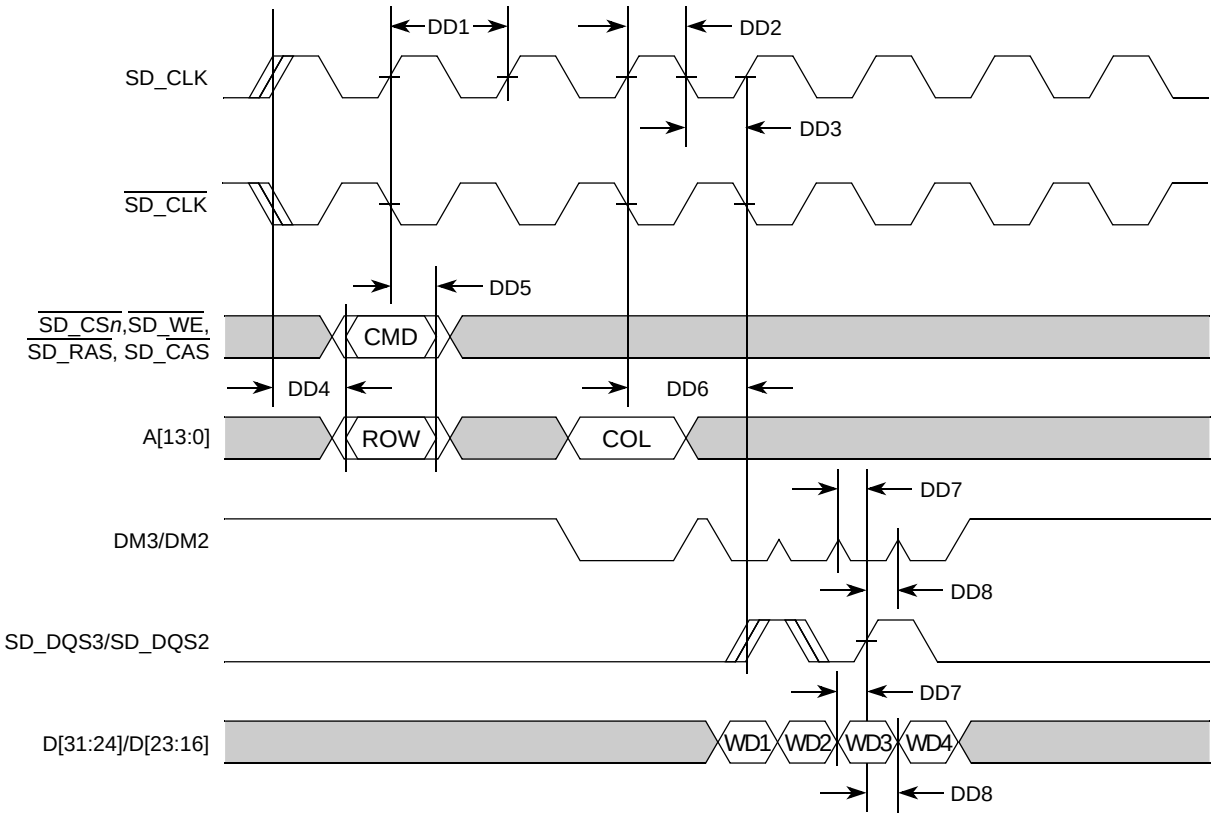


Figure 11. DDR Write Timing

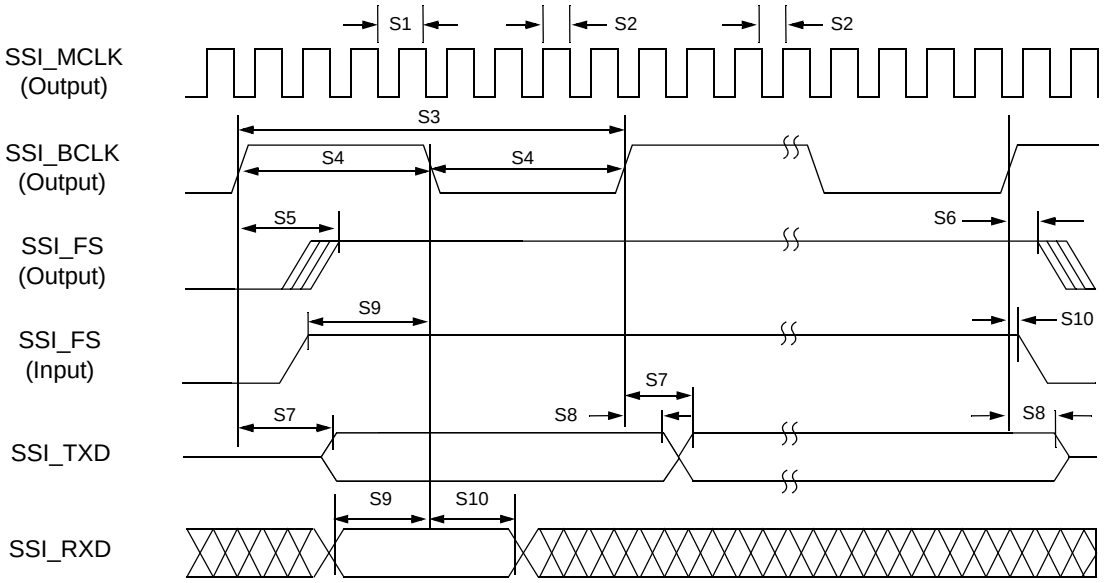


Figure 15. SSI Timing – Master Modes

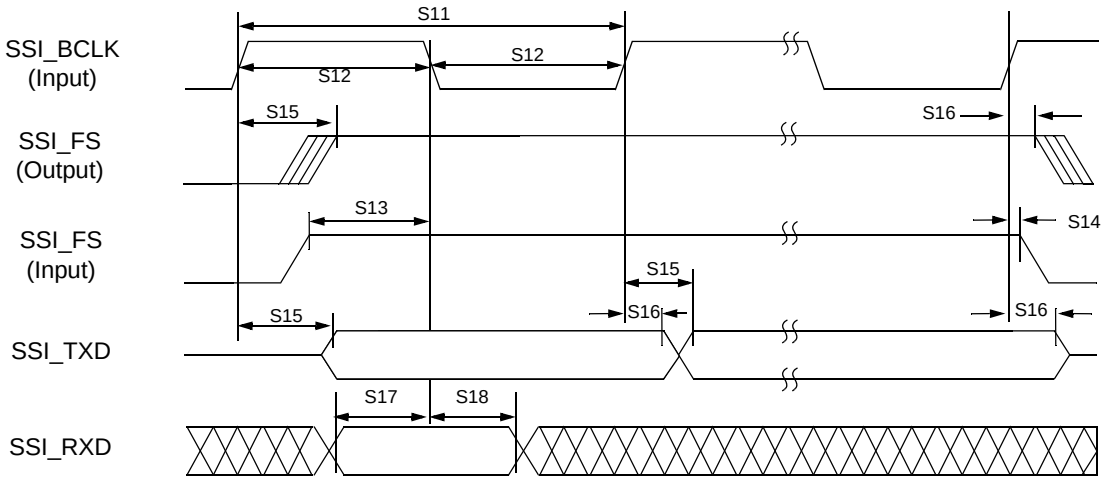


Figure 16. SSI Timing – Slave Modes

5.12 I²C Input/Output Timing Specifications

Table 16 lists specifications for the I²C input timing parameters shown in Figure 17.

Table 16. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

Table 16. I²C Input Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Units
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 17 lists specifications for the I²C output timing parameters shown in Figure 17.

Table 17. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 17. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 17 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 17 shows timing for the values in Table 17 and Table 16.

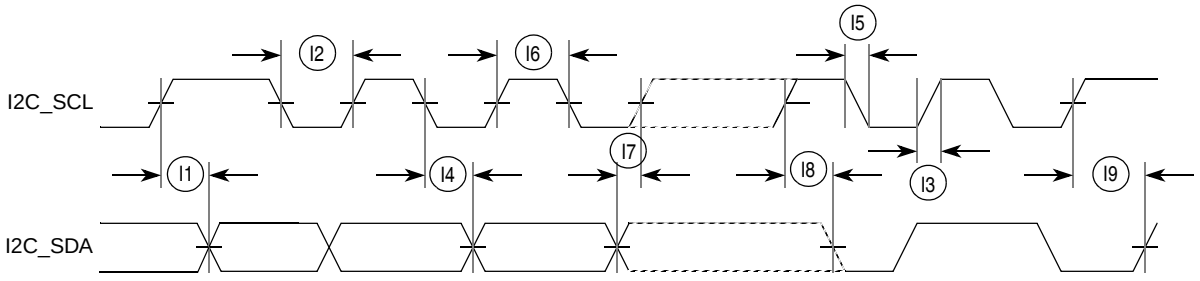


Figure 17. I²C Input/Output Timings

5.13 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at 5.0 V or 3.3 V.

5.13.1 MII Receive Signal Timing

The receiver functions correctly up to a FEC_RXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC_RXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RXDV, FEC_RXER to FEC_RXCLK setup	5	—	ns
M2	FEC_RXCLK to FEC_RXD[3:0], FEC_RXDV, FEC_RXER hold	5	—	ns
M3	FEC_RXCLK pulse width high	35%	65%	FEC_RXCLK period
M4	FEC_RXCLK pulse width low	35%	65%	FEC_RXCLK period

Figure 18 shows MII receive signal timings listed in Table 18.

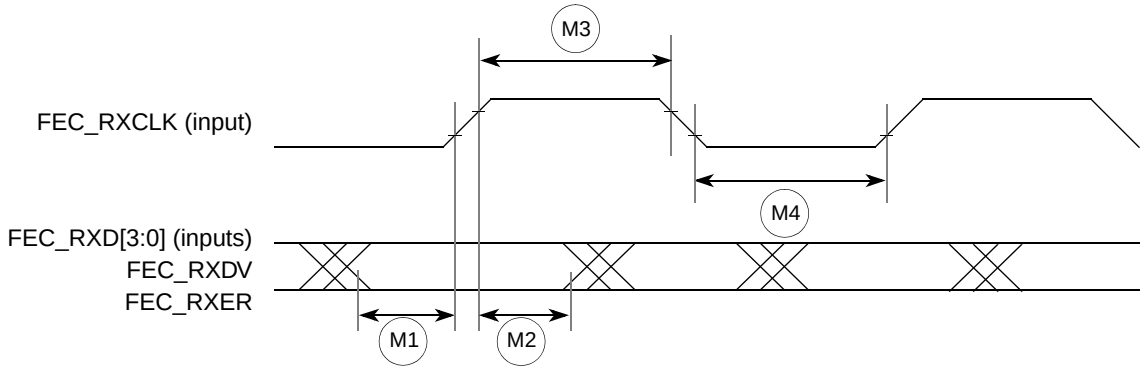


Figure 18. MII Receive Signal Timing Diagram

5.13.2 MII Transmit Signal Timing

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC_TXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC_TXCLK frequency.

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER invalid	5	—	ns
M6	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER valid	—	25	ns
M7	FEC_TXCLK pulse width high	35%	65%	FEC_TXCLK period
M8	FEC_TXCLK pulse width low	35%	65%	FEC_TXCLK period

Figure 19 shows MII transmit signal timings listed in Table 19.

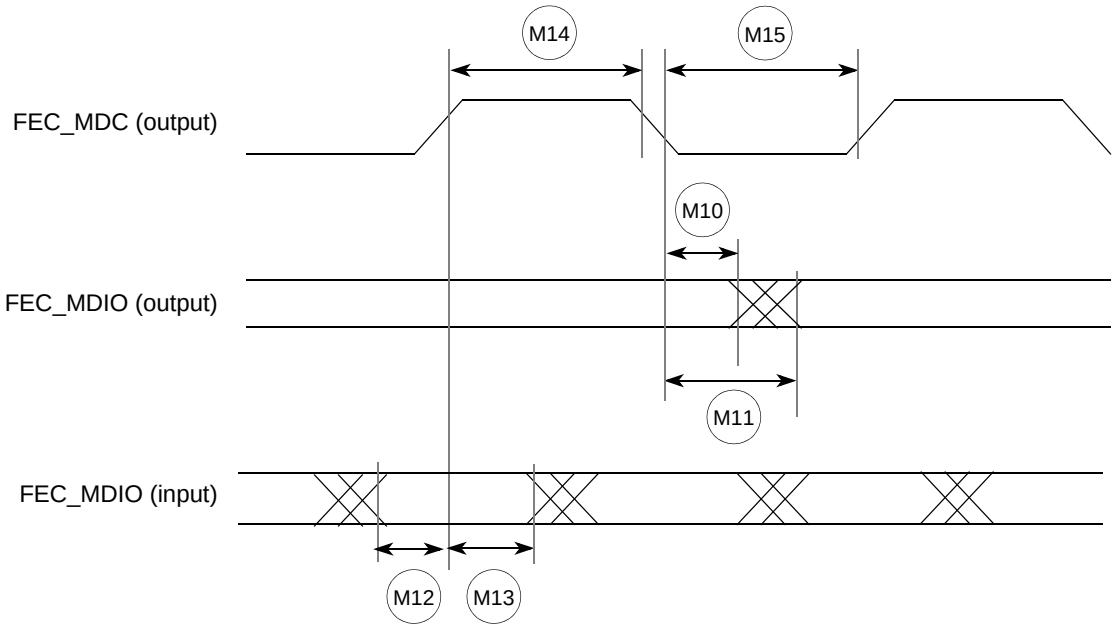


Figure 21. MII Serial Management Channel Timing Diagram

5.14 32-Bit Timer Module Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.15 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

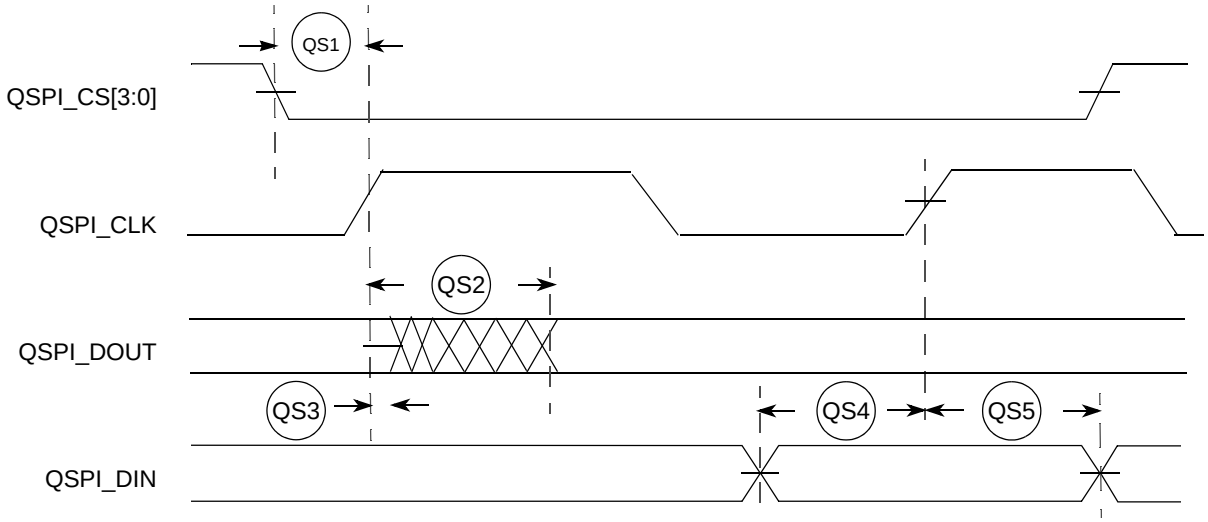


Figure 22. QSPI Timing

5.16 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/3}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

5.17 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 27.

Table 25. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	2	2	$t_{SYS} = 1/f_{SYS}$
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

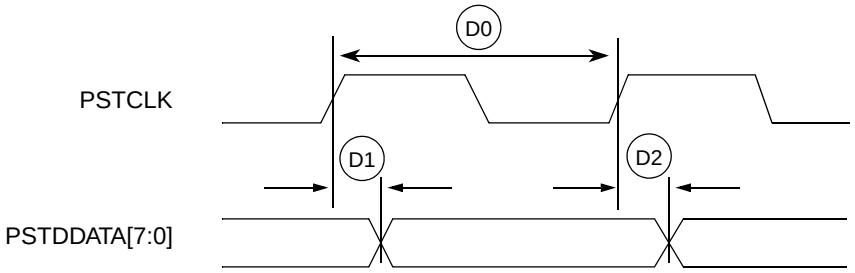


Figure 27. Real-Time Trace AC Timing

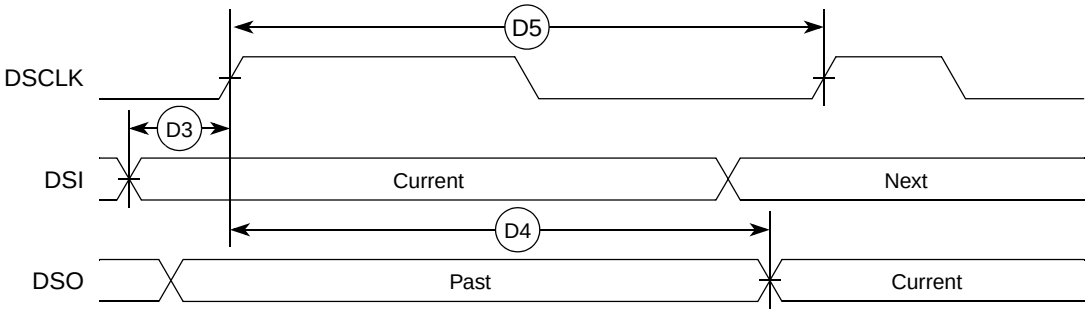


Figure 28. BDM Serial Port AC Timing

6 Current Consumption

All current consumption data is lab data measured on a single device using an evaluation board. Table 26 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

Table 26. Current Consumption in Low-Power Modes[1,2]

Mode	Voltage	58 MHz (Typ)[3]	64 MHz (Typ)[3]	72 MHz (Typ)[3]	80 MHz (Typ)[3]	80 MHz (Peak)[4]	Units
Stop Mode 3 (Stop 11)[5]	3.3 V	3.9	3.92	4.0	4.0	4.0	mA
	1.5 V	1.04	1.04	1.04	1.04	1.08	
Stop Mode 2 (Stop 10)[4]	3.3 V	4.69	4.72	4.8	4.8	4.8	
	1.5 V	2.69	2.69	2.70	2.70	2.75	
Stop Mode 1(Stop 01)[4]	3.3 V	4.72	4.73	4.81	4.81	4.81	
	1.5 V	15.28	16.44	17.85	19.91	20.42	
Stop Mode 0 (Stop 00)[4]	3.3 V	21.65	21.68	24.33	26.13	26.16	
	1.5 V	15.47	16.63	18.06	20.12	20.67	
Wait/Doze	3.3 V	22.49	22.52	25.21	27.03	39.8	
	1.5 V	26.79	28.85	30.81	34.47	97.4	
Run	3.3 V	33.61	33.61	42.3	50.5	62.6	
	1.5 V	56.3	60.7	65.4	73.4	132.3	

1 All values are measured with a 3.30V EV_{DD}, 3.30V SDV_{DD} and 1.5V IV_{DD} power supplies. Tests performed at room temperature with pins configured for high drive strength.

2 Refer to the Power Management chapter in the *MCF537x Reference Manual* for more information on low-power modes.

3 All peripheral clocks except UART0, FlexBus, INTC0, reset controller, PLL, and edge port off before entering low power mode. All code executed from flash.

4 All peripheral clocks on before entering low power mode. All code is executed from flash.

5 See the description of the low-power control register (LCPR) in the *MCF537x Reference Manual* for more information on stop modes 0–3.

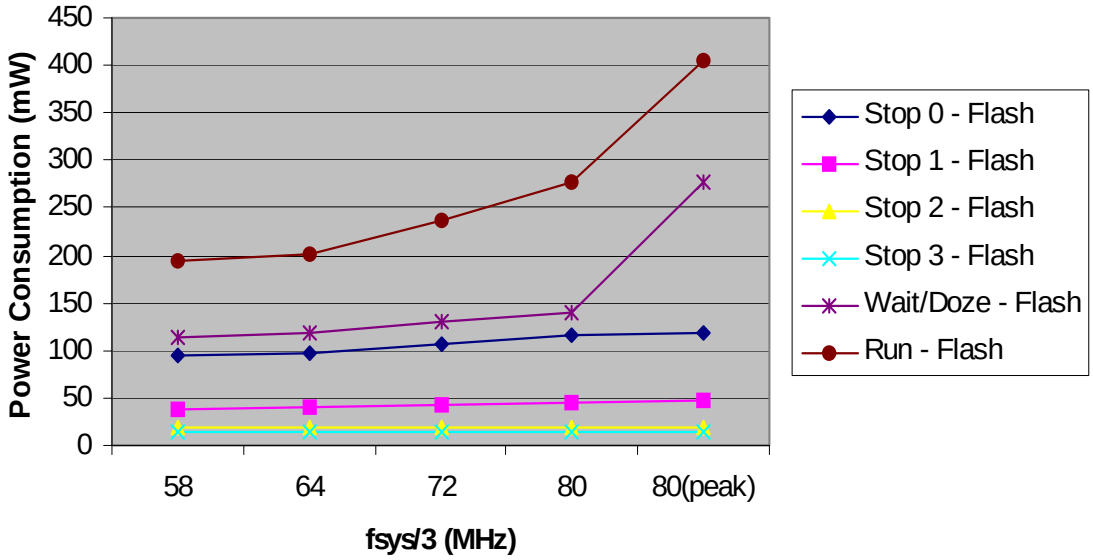
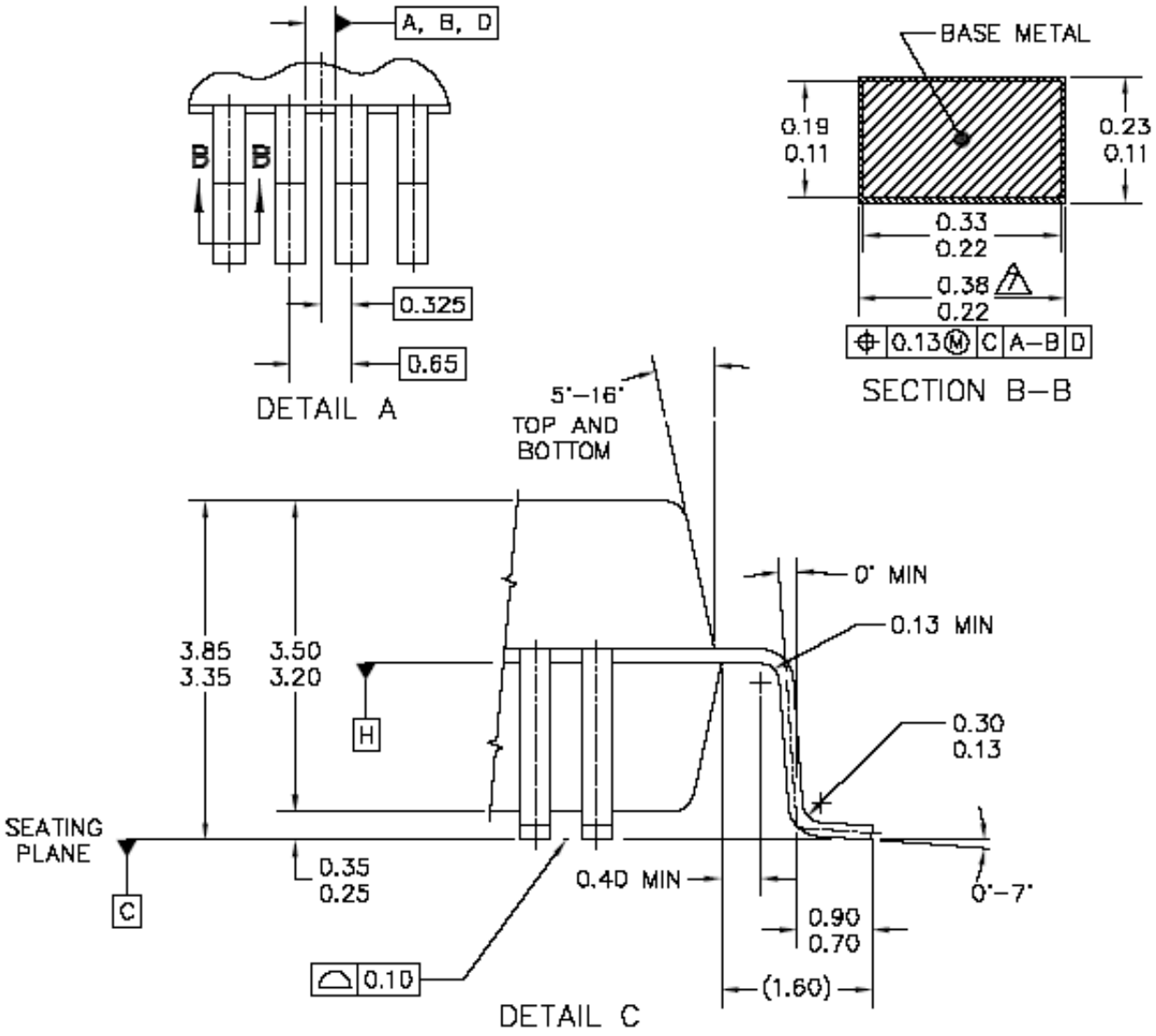


Figure 29. Current Consumption in Low-Power Modes



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

Figure 33. 160QFP Package Dimensions (Sheet 2 of 2)

8 Revision History

Table 28. MCF5373DS Document Revision History

Rev. No.	Substantive Changes	Date of Release
0	• Initial release	11/2005
0.1	• Swapped pin locations PLL_VSS (J11->H11) and DRAMSEL (H11->J11) in Table 1. Figure 4 is correct.	12/2005
0.2	• Added not to Section 7, “Package Information.” • Added “top view” and “bottom view” where appropriate in mechanical drawings and pinout figures. • Figure 6: Corrected “FB_CLK (75MHz)” label to “FB_CLK (80MHz)”	3/2006
0.3	• Changed 160QFP pinouts in Figure 5 and Table 2: Removed IRQ3 pin, shifted pins 89–99 up one pin to 90–100. Pin 89 is now VSS. • Table 2: Rearranged GPIO signal names for FEC pins. • Removed ULPI specifications as the device does not support ULPI.	4/2006
1	• Updated thermal characteristic values in Table 7. • Updated DC electricals values in Table 7. • Updated Section 3.3, “Supply Voltage Sequencing and Separation Cautions” and subsections. • Updated and added Oscillator/PLL characteristics in Table 8. • Table 9: Swapped min/max for FB1; Removed FB8 & FB9. • Updated SDRAM write timing diagram, Figure 9. • Table 11: Added values for frequency of operation and DD1. • Replaced figure & table Section 5.11, “SSI Timing Specifications,” with slave & master mode versions. • Removed second sentence from Section 5.13.2, “MII Transmit Signal Timing,” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 5.13.2, “MII Transmit Signal Timing,” as this feature is not supported on this device. • Updated figure & table Section 5.17, “Debug AC Timing Specifications.” • Renamed & moved previous version’s Section 5.5 “Power Consumption” to Section 6, “Current Consumption.” Added additional real-world data to this section as well.	7/2007
2	• Added MCF53721 device information throughout: features list, family configuration table, ordering information table, signals description table, and relevant package diagram titles • Remove Footnote 1 from Table 11. • Changed document type from Advance Information to Technical Data.	8/2007