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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	600
Number of I/O	36
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7032aetc44-7n

Table 1. MAX 7000A Device Features

Feature	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
t_{PD} (ns)	4.5	4.5	5.0	5.5	7.5
t_{SU} (ns)	2.9	2.8	3.3	3.9	5.6
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3.0
t_{CO1} (ns)	3.0	3.1	3.4	3.5	4.7
f_{CNT} (MHz)	227.3	222.2	192.3	172.4	116.3

...and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt™ I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins

MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000A devices contain from 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms, providing up to 32 product terms per macrocell.

MAX 7000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5-V, 3.3-V, and 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems.

MAX 7000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. [Figure 1](#) shows the architecture of MAX 7000A devices.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000A devices. As shown in [Figure 1](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figure 2](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in a MAX 7000AE device may be set to either a high or low state. This power-up state is specified at design entry. Upon power-up, each register in EPM7128A and EPM7256A devices are set to a low state.

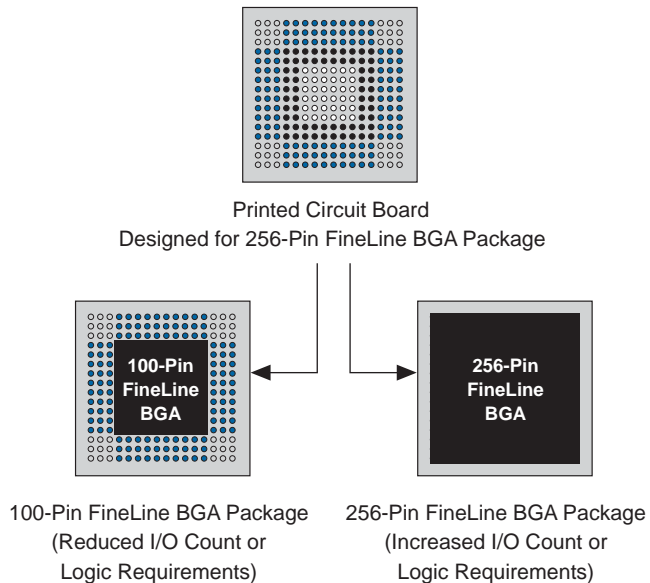
All MAX 7000A I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (as low as 2.5 ns) input setup time.

SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 7](#)).

Figure 7. SameFrame Pin-Out Example





For more information on using the Jam STAPL language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)*.

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000A Device

The time required to program a single MAX 7000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
 t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
 $Cycle_{PTCK}$ = Number of TCK cycles to program a device
 f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
 t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
 $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Programmable Speed/Power Control

MAX 7000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000A device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power operation (i.e., with the Turbo Bit option turned off). As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters.

Output Configuration

MAX 7000A device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000A devices to connect to systems with differing supply voltages. MAX 7000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with VCCIO levels lower than 3.0 V incur a slightly greater timing delay of t_{OD2} instead of t_{OD1} . Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 12 describes the MAX 7000A MultiVolt I/O support.

Table 12. MAX 7000A MultiVolt I/O Support						
V _{CCIO} Voltage	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓		✓	✓

Table 14. MAX 7000A Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (13)	3.0	3.6	V
V _{CCIO}	Supply voltage for output drivers, 3.3-V operation	(3)	3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation	(3)	2.3	2.7	V
V _{CCISP}	Supply voltage during in-system programming		3.0	3.6	V
V _I	Input voltage	(4)	−0.5	5.75	V
V _O	Output voltage		0	V _{CCIO}	V
T _A	Ambient temperature	Commercial range	0	70	°C
		Industrial range (5)	−40	85	°C
T _J	Junction temperature	Commercial range	0	90	°C
		Industrial range (5)	−40	105	°C
		Extended range (5)	−40	130	°C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) For EPM7128A and EPM7256A devices only, V_{CC} must rise monotonically.
- (4) In MAX 7000AE devices, all pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (5) These devices support in-system programming for -40° to 100° C. For in-system programming support between -40° and 0° C, contact Altera Applications.
- (6) These values are specified under the recommended operating conditions shown in [Table 14 on page 28](#).
- (7) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (8) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.
- (9) This value is specified for normal device operation. For MAX 7000AE devices, the maximum leakage current during power-up is ± 300 μ A. For EPM7128A and EPM7256A devices, leakage current during power-up is not specified.
- (10) For EPM7128A and EPM7256A devices, this pull-up exists while a device is programmed in-system.
- (11) For MAX 7000AE devices, this pull-up exists while devices are programmed in-system and in unprogrammed devices during power-up.
- (12) Capacitance is measured at 25° C and is sample-tested only. The $\odot E1$ pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
- (13) The POR time for MAX 7000AE devices (except MAX 7128A and MAX 7256A devices) does not exceed 100 μ s. The sufficient V_{CCINT} voltage level for POR is 3.0 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.

Figure 12. MAX 7000A Switching Waveforms

t_R & $t_F < 2$ ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

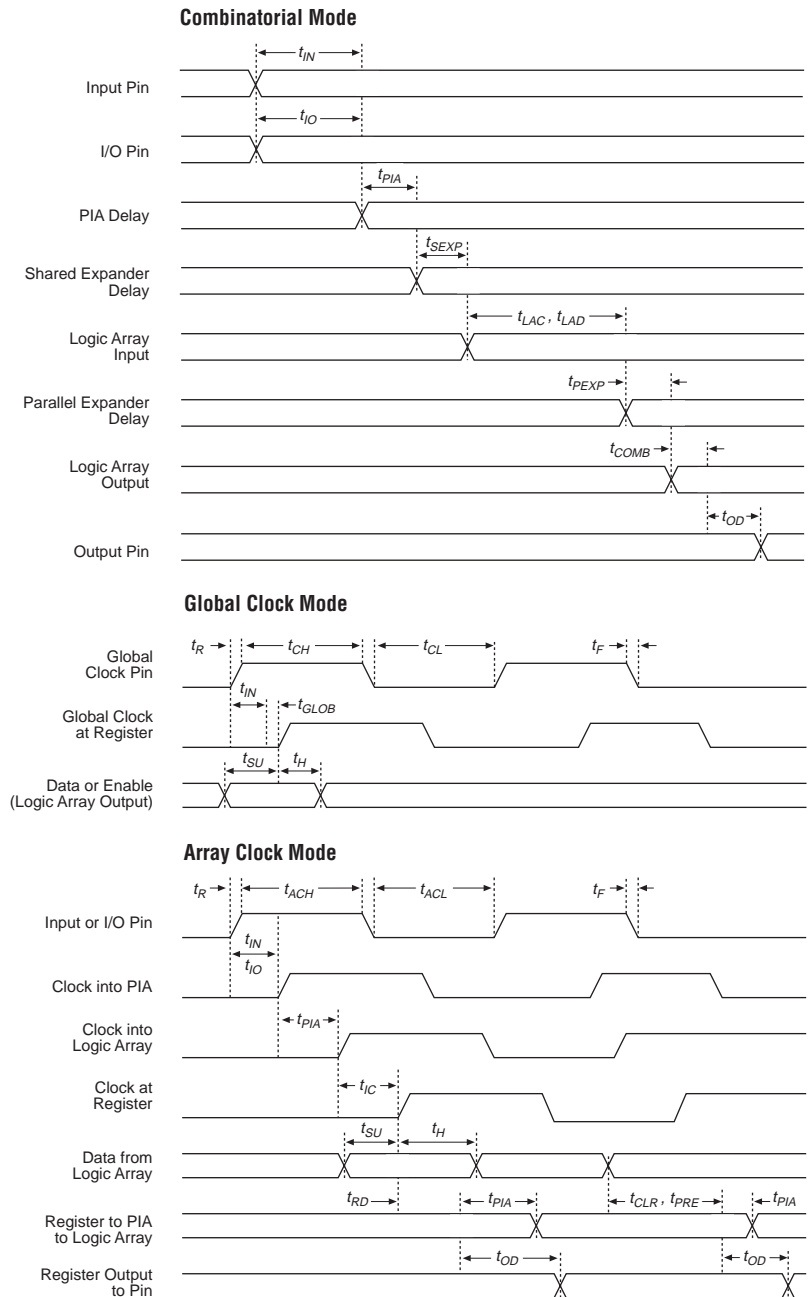


Table 22. EPM7128AE Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		1.0		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.7		1.0		1.4	ns
t_{FIN}	Fast input delay			2.5		3.0		3.4	ns
t_{SEXP}	Shared expander delay			2.0		2.9		3.8	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.6		2.4		3.1	ns
t_{LAC}	Logic control array delay			0.7		1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.3		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.8		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.4		2.1		2.9		ns
t_H	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		1.1		1.6		1.6		ns
t_{FH}	Register hold time of fast input		1.4		1.4		1.4		ns
t_{RD}	Register delay			0.8		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.5		0.9		1.3	ns
t_{IC}	Array clock delay			1.2		1.7		2.2	ns

Table 24. EPM7256AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IC}	Array clock delay			1.2		1.6		2.1	ns
t_{EN}	Register enable time			0.8		1.0		1.3	ns
t_{GLOB}	Global control delay			1.0		1.5		2.0	ns
t_{PRE}	Register preset time			1.6		2.3		3.0	ns
t_{CLR}	Register clear time			1.6		2.3		3.0	ns
t_{PIA}	PIA delay	(2)		1.7		2.4		3.2	ns
t_{LPA}	Low-power adder	(6)		4.0		4.0		5.0	ns

Table 26. EPM7512AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

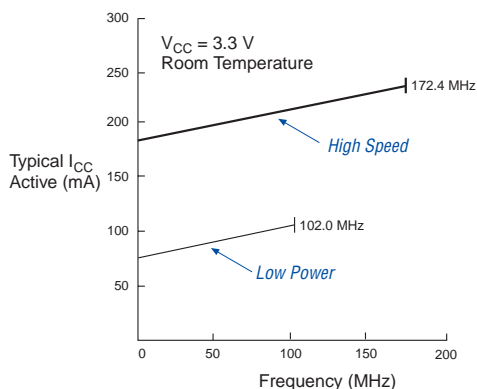
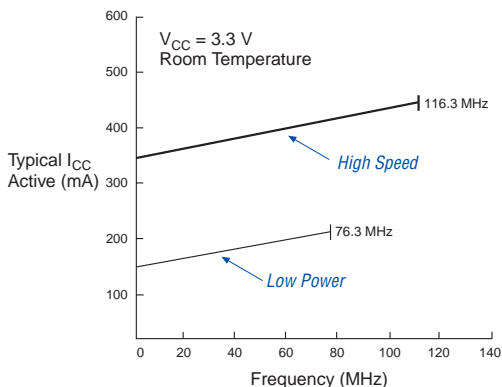
Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{IC}	Array clock delay			1.8		2.3		2.9	ns
t_{EN}	Register enable time			1.0		1.3		1.7	ns
t_{GLOB}	Global control delay			1.7		2.2		2.7	ns
t_{PRE}	Register preset time			1.0		1.4		1.7	ns
t_{CLR}	Register clear time			1.0		1.4		1.7	ns
t_{PIA}	PIA delay	(2)		3.0		4.0		4.8	ns
t_{LPA}	Low-power adder	(6)		4.5		5.0		5.0	ns

Table 28. EPM7128A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		0.7		0.9		1.1	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.7		0.9		1.1	ns
t_{FIN}	Fast input delay			2.7		3.1		3.6		3.9	ns
t_{SEXP}	Shared expander delay			2.5		3.2		4.3		5.1	ns
t_{PEXP}	Parallel expander delay			0.7		0.8		1.1		1.3	ns
t_{LAD}	Logic array delay			2.4		3.0		4.1		4.9	ns
t_{LAC}	Logic control array delay			2.4		3.0		4.1		4.9	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.4		0.6		0.7		0.9	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		0.9		1.1		1.2		1.4	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.4		5.6		5.7		5.9	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0		5.0	ns
t_{SU}	Register setup time		1.9		2.4		3.1		3.8		ns
t_H	Register hold time		1.5		2.2		3.3		4.3		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.7		1.9		1.9		1.9		ns

Table 28. EPM7128A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{RD}	Register delay			1.7		2.1		2.8		3.3	ns
t_{COMB}	Combinatorial delay			1.7		2.1		2.8		3.3	ns
t_{IC}	Array clock delay			2.4		3.0		4.1		4.9	ns
t_{EN}	Register enable time			2.4		3.0		4.1		4.9	ns
t_{GLOB}	Global control delay			1.0		1.2		1.7		2.0	ns
t_{PRE}	Register preset time			3.1		3.9		5.2		6.2	ns
t_{CLR}	Register clear time			3.1		3.9		5.2		6.2	ns
t_{PIA}	PIA delay	(2)		0.9		1.1		1.5		1.8	ns
t_{LPA}	Low-power adder	(6)		11.0		10.0		10.0		10.0	ns

Figure 13. I_{CC} vs. Frequency for MAX 7000A Devices (Part 2 of 2)**EPM7256A & EPM7256AE****EPM7512AE**

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figures 14 through 23 show the package pin-out diagrams for MAX 7000A devices.

Figure 14. 44-Pin PLCC/TQFP Package Pin-Out Diagram

Package outlines not drawn to scale.

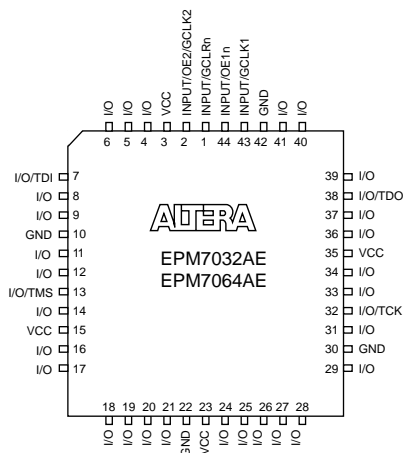
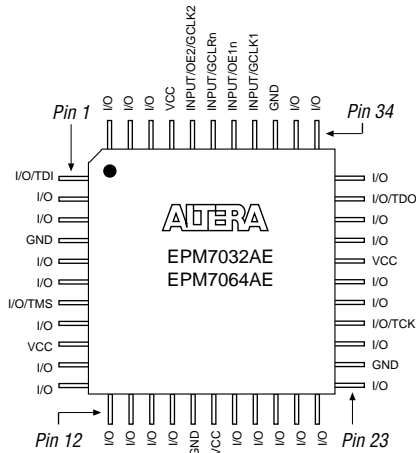
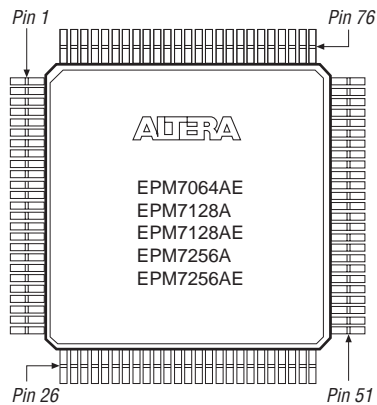
**44-Pin PLCC****44-Pin TQFP**

Figure 17. 100-Pin TQFP Package Pin-Out Diagram*Package outline not drawn to scale.***Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram***Package outline not drawn to scale.*

Version 4.3

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.3:

- Added extended temperature devices to document
- Updated [Table 14](#).

Version 4.2

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.2:

- Removed *Note (1)* from [Table 2](#).
- Removed *Note (4)* from [Tables 3](#) and [4](#).

Version 4.1

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.1:

- Updated leakage current information in [Table 15](#).
- Updated [Note \(9\)](#) of [Table 15](#).
- Updated [Note \(1\)](#) of [Tables 17](#) through [30](#).



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