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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

| Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	36
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7064aeli44-7

■ Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

■ Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest

■ Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, ByteBlasterMV™ parallel port download cable, and BitBlaster™ serial download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File- (**.svf**) capable in-circuit tester

General Description

MAX 7000A (including MAX 7000AE) devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 7000A devices in the -4, -5, -6, -7, and some -10 speed grades are compatible with the timing requirements for 33 MHz operation of the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See Table 2.

Table 2. MAX 7000A Speed Grades						
Device	**Speed Grade**					
	-4	**-5**	**-6**	**-7**	**-10**	**-12**
EPM7032AE	✓			✓	✓	
EPM7064AE	✓			✓	✓	
EPM7128A			✓	✓	✓	✓
EPM7128AE		✓		✓	✓	
EPM7256A			✓	✓	✓	✓
EPM7256AE		✓		✓	✓	
EPM7512AE				✓	✓	✓

Figure 1. MAX 7000A Device Block Diagram
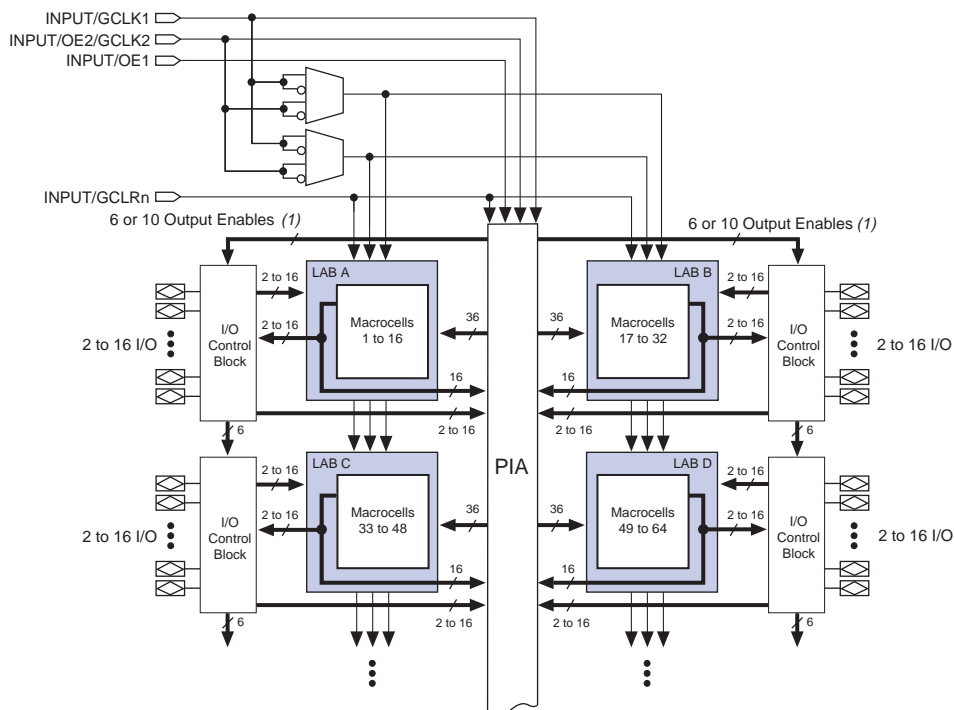
Note:
(1)   EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables.
      EPM7512AE devices have 10 output enables.

Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

■   36 signals from the PIA that are used for general logic inputs
■   Global controls that are used for secondary register functions
■   Direct input paths from I/O pins to the registers that are used for fast setup times

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders, and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 5. MAX 7000A PIA Routing

PIA Signals
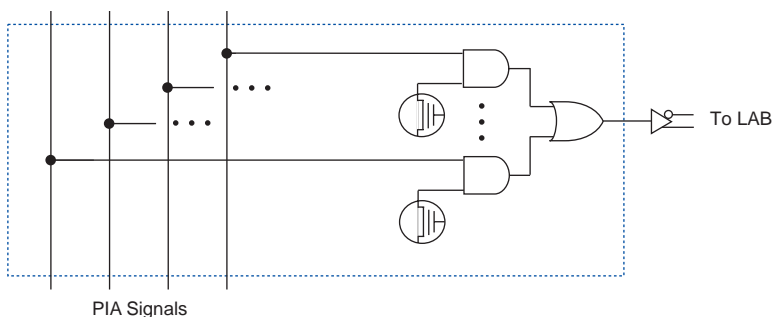
While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 7000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 6. I/O Control Block of MAX 7000A Devices
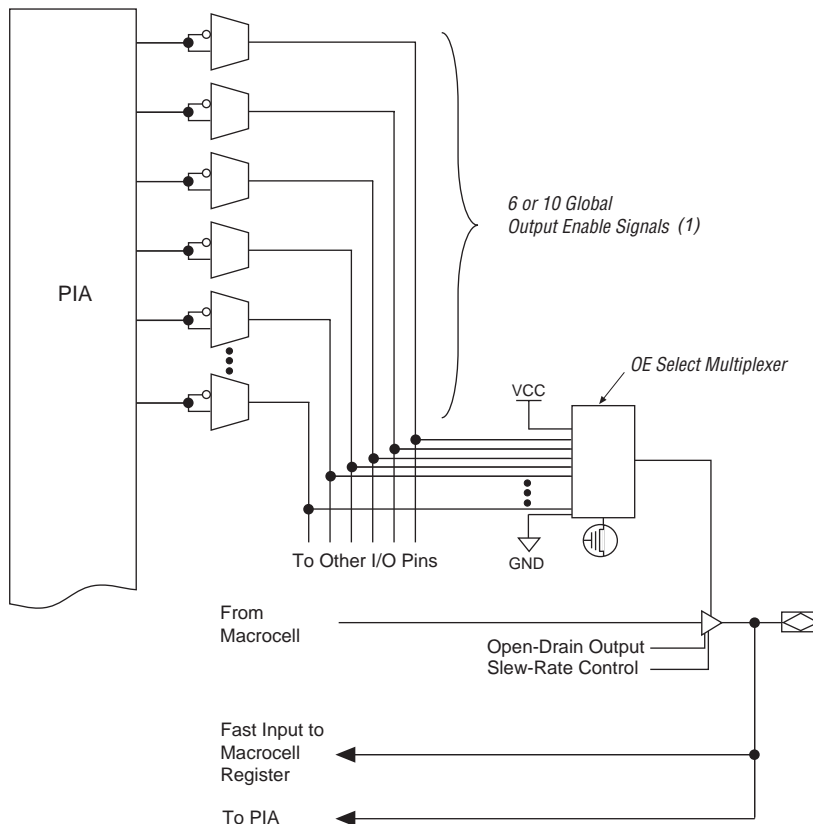
Note:

(1)   EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enable signals. EPM7512AE devices have 10 output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The MAX 7000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Table 7. MAX 7000A Stand-Alone Verification Times for Different Test Clock Frequencies									
Device	f_{TCK}								**Units**
	10 MHz	**5 MHz**	**2 MHz**	**1 MHz**	**500 kHz**	**200 kHz**	**100 kHz**	**50 kHz**	
EPM7032AE	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	s
EPM7064AE	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	s
EPM7128AE	0.01	0.02	0.04	0.07	0.14	0.34	0.68	1.36	s
EPM7256AE	0.02	0.03	0.08	0.15	0.30	0.75	1.49	2.98	s
EPM7512AE	0.03	0.06	0.15	0.30	0.60	1.49	2.97	5.94	s
EPM7128A *(1)*	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	s
EPM7256A *(1)*	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	s

Note to tables:

(1)   EPM7128A and EPM7256A devices can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

Programming with External Hardware

MAX 7000A devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checks to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices.

For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1. Table 8 describes the JTAG instructions supported by MAX 7000A devices. The pin-out tables, available from the Altera web site (**http://www.altera.com**), show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

The instruction register length of MAX 7000A devices is 10 bits. The user electronic signature (UES) register length in MAX 7000A devices is 16 bits. The MAX 7000AE USERCODE register length is 32 bits. Tables 9 and 10 show the boundary-scan register length and device IDCODE information for MAX 7000A devices.

Table 9. MAX 7000A Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032AE	96
EPM7064AE	192
EPM7128A	288
EPM7128AE	288
EPM7256A	480
EPM7256AE	480
EPM7512AE	624

Table 10. 32-Bit MAX 7000A Device IDCODE   Note (1)

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM7032AE	0001	0111 0000 0011 0010	00001101110	1
EPM7064AE	0001	0111 0000 0110 0100	00001101110	1
EPM7128A	0000	0111 0001 0010 1000	00001101110	1
EPM7128AE	0001	0111 0001 0010 1000	00001101110	1
EPM7256A	0000	0111 0010 0101 0110	00001101110	1
EPM7256AE	0001	0111 0010 0101 0110	00001101110	1
EPM7512AE	0001	0111 0101 0001 0010	00001101110	1

Notes:

(1)   The most significant bit (MSB) is on the left.

(2)   The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST.

Programmable Speed/Power Control

MAX 7000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000A device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power operation (i.e., with the Turbo Bit option turned off). As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, t_{ACL}, and t_{CPPW} parameters.

Output Configuration

MAX 7000A device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000A devices to connect to systems with differing supply voltages. MAX 7000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 3.0 V incur a slightly greater timing delay of t_{OD2} instead of t_{OD1}. Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 12 describes the MAX 7000A MultiVolt I/O support.

Table 12. MAX 7000A MultiVolt I/O Support						
V_{CCIO} Voltage	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓		✓	✓

Power Sequencing & Hot-Socketing	Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000AE devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.

MAX 7000AE device I/O pins will not source or sink more than 300 μA of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the OE1 and GLCRn pins. The OE1 and GLCRn pins can be driven up to 3.6 V during hot-socketing. After V_{CCINT} and V_{CCIO} reach the recommended operating conditions, these two pins are 5.0-V tolerant.

EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.

Design Security

All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9. Test patterns can be used and then erased during early stages of the production flow.

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet.*

(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) For EPM7128A and EPM7256A devices only, V_{CC} must rise monotonically.

(4) In MAX 7000AE devices, all pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(5) These devices support in-system programming for –40° to 100° C. For in-system programming support between –40° and 0° C, contact Altera Applications.

(6) These values are specified under the recommended operating conditions shown in Table 14 on page 28.

(7) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.

(8) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.

(9) This value is specified for normal device operation. For MAX 7000AE devices, the maximum leakage current during power-up is ±300 μA. For EPM7128A and EPM7256A devices, leakage current during power-up is not specified.

(10) For EPM7128A and EPM7256A devices, this pull-up exists while a device is programmed in-system.

(11) For MAX 7000AE devices, this pull-up exists while devices are programmed in-system and in unprogrammed devices during power-up.

(12) Capacitance is measured at 25 °C and is sample-tested only. The OE1 pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

(13) The POR time for MAX 7000AE devices (except MAX 7128A and MAX 7256A devices) does not exceed 100 μs. The sufficient V_{CCINT} voltage level for POR is 3.0 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.

Figure 11. MAX 7000A Timing Model
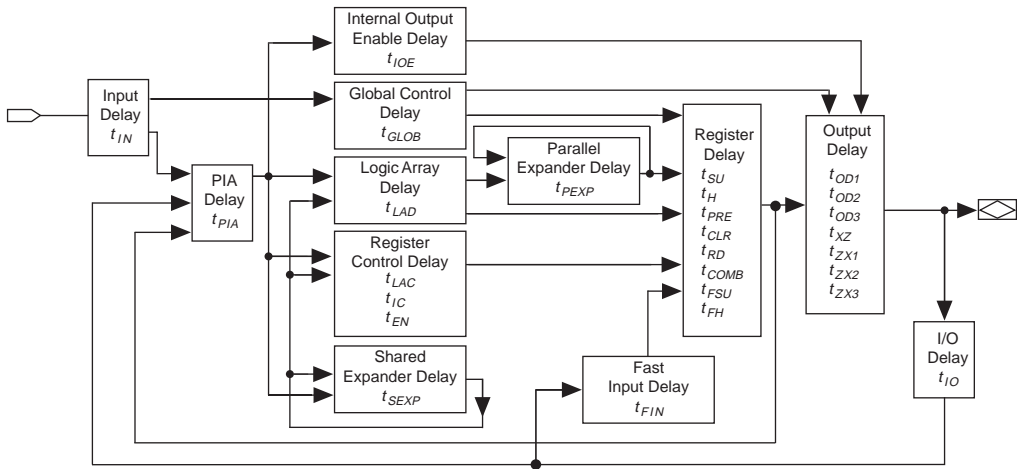
The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 12 shows the timing relationship between internal and external delay parameters.

See *Application Note 94 (Understanding MAX 7000 Timing)* for more information.

Table 18. EPM7032AE Internal Timing Parameters (Part 2 of 2)   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IC}	Array clock delay			1.2		2.0		2.5	ns
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			0.8		1.3		1.9	ns
t_{PRE}	Register preset time			1.2		1.9		2.6	ns
t_{CLR}	Register clear time			1.2		1.9		2.6	ns
t_{PIA}	PIA delay	*(2)*		0.9		1.5		2.1	ns
t_{LPA}	Low-power adder	*(6)*		2.5		4.0		5.0	ns

Table 19. EPM7064AE External Timing Parameters   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		4.5		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		4.5		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	2.8		4.7		6.2		ns
t_H	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.1	1.0	5.1	1.0	7.0	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.6		2.6		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.3		0.4		0.6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.3	1.0	7.2	1.0	9.6	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		4.5		7.4		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*(2), (4)*	222.2		135.1		100.0		MHz
t_{ACNT}	Minimum array clock period	*(2)*		4.5		7.4		10.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(2), (4)*	222.2		135.1		100.0		MHz

Table 24. EPM7256AE Internal Timing Parameters (Part 1 of 2) Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		0.9		1.2	ns
t_{IO}	I/O input pad and buffer delay			0.7		0.9		1.2	ns
t_{FIN}	Fast input delay			2.4		2.9		3.4	ns
t_{SEXP}	Shared expander delay			2.1		2.8		3.7	ns
t_{PEXP}	Parallel expander delay			0.3		0.5		0.6	ns
t_{LAD}	Logic array delay			1.7		2.2		2.8	ns
t_{LAC}	Logic control array delay			0.8		1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF (5)		1.4		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF (5)		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.5		2.1		2.9		ns
t_{H}	Register hold time		0.7		0.9		1.2		ns
t_{FSU}	Register setup time of fast input		1.1		1.6		1.6		ns
t_{FH}	Register hold time of fast input		1.4		1.4		1.4		ns
t_{RD}	Register delay			0.9		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.5		0.8		1.2	ns

Table 26. EPM7512AE Internal Timing Parameters (Part 2 of 2)   Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{IC}	Array clock delay			1.8		2.3		2.9	ns
t_{EN}	Register enable time			1.0		1.3		1.7	ns
t_{GLOB}	Global control delay			1.7		2.2		2.7	ns
t_{PRE}	Register preset time			1.0		1.4		1.7	ns
t_{CLR}	Register clear time			1.0		1.4		1.7	ns
t_{PIA}	PIA delay	(2)		3.0		4.0		4.8	ns
t_{LPA}	Low-power adder	(6)		4.5		5.0		5.0	ns

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Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{RD}	Register delay			1.7		2.1		2.8		3.3	ns
t_{COMB}	Combinatorial delay			1.7		2.1		2.8		3.3	ns
t_{IC}	Array clock delay			2.4		3.0		4.1		4.9	ns
t_{EN}	Register enable time			2.4		3.0		4.1		4.9	ns
t_{GLOB}	Global control delay			1.0		1.2		1.7		2.0	ns
t_{PRE}	Register preset time			3.1		3.9		5.2		6.2	ns
t_{CLR}	Register clear time			3.1		3.9		5.2		6.2	ns
t_{PIA}	PIA delay	(2)		0.9		1.1		1.5		1.8	ns
t_{LPA}	Low-power adder	(6)		11.0		10.0		10.0		10.0	ns

Table 28. EPM7128A Internal Timing Parameters (Part 2 of 2)   *Note (1)*

Table 30. EPM7256A Internal Timing Parameters (Part 2 of 2)   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{COMB}	Combinatorial delay			1.6		2.0		2.7		3.2	ns
t_{IC}	Array clock delay			2.7		3.4		4.5		5.4	ns
t_{EN}	Register enable time			2.5		3.1		4.2		5.0	ns
t_{GLOB}	Global control delay			1.1		1.4		1.8		2.2	ns
t_{PRE}	Register preset time			2.3		2.9		3.8		4.6	ns
t_{CLR}	Register clear time			2.3		2.9		3.8		4.6	ns
t_{PIA}	PIA delay	*(2)*		1.3		1.6		2.1		2.6	ns
t_{LPA}	Low-power adder	*(6)*		11.0		10.0		10.0		10.0	ns

Notes to tables:

(1)   These values are specified under the recommended operating conditions shown in Table 14 on page 28. See Figure 12 for more information on switching waveforms.

(2)   These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3)   This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(4)   This parameter is measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5)   Operating conditions: V_{CCIO} = 2.5 ± 0.2 V for commercial and industrial use.

(6)   The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, **t_{ACL}**, and **t_{CPPW}** parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency (f_{MAX}, in MHz) for MAX 7000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times tog_{LC})$$

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The parameters in this equation are:

MC_{TON}	=	Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV}	=	Number of macrocells in the device
MC_{USED}	=	Total number of macrocells in the design, as reported in the Report File
f_{MAX}	=	Highest clock frequency to the device
tog_{LC}	=	Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C	=	Constants, shown in Table 31

Table 31. MAX 7000A I_{CC} Equation Constants

Device	A	B	C
EPM7032AE	0.71	0.30	0.014
EPM7064AE	0.71	0.30	0.014
EPM7128A	0.71	0.30	0.014
EPM7128AE	0.71	0.30	0.014
EPM7256A	0.71	0.30	0.014
EPM7256AE	0.71	0.30	0.014
EPM7512AE	0.71	0.30	0.014

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.
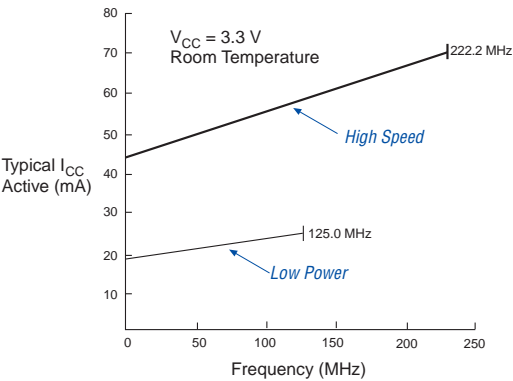
Figure 13 shows the typical supply current versus frequency for MAX 7000A devices.

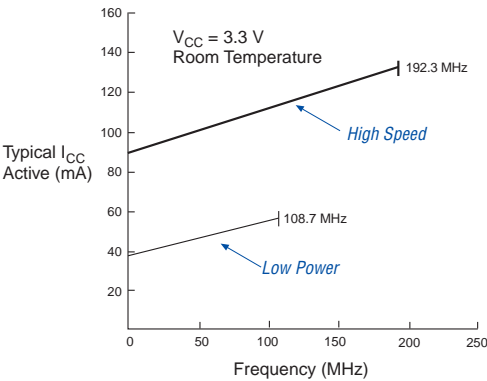*Figure 13. I_{CC} vs. Frequency for MAX 7000A Devices (Part 1 of 2)*
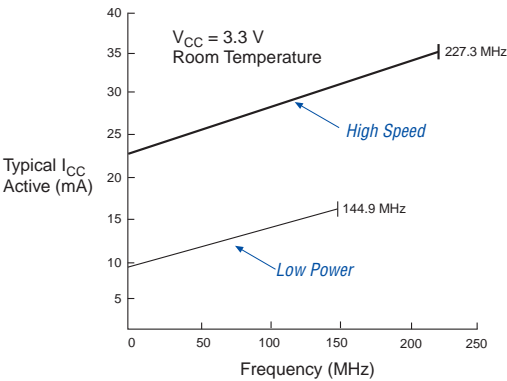
Figure 19. 144-Pin TQFP Package Pin-Out Diagram
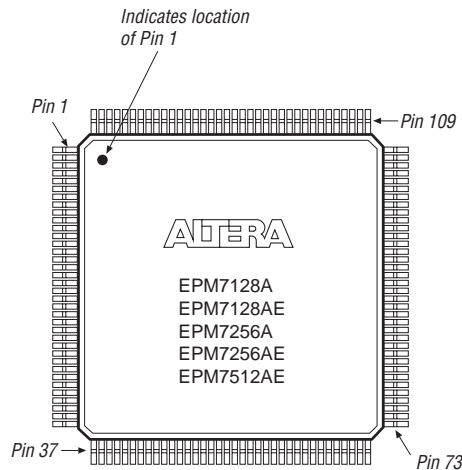
Package outline not drawn to scale.

Figure 20. 169-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.