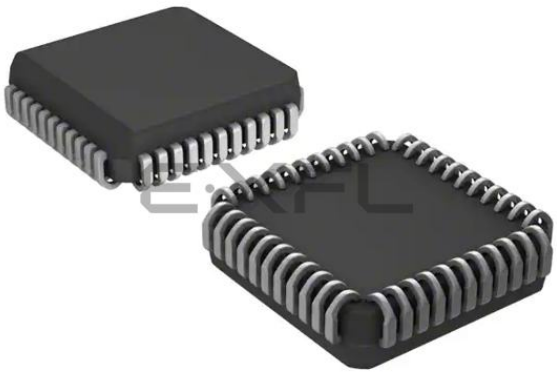

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	36
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7064aeli44-7n

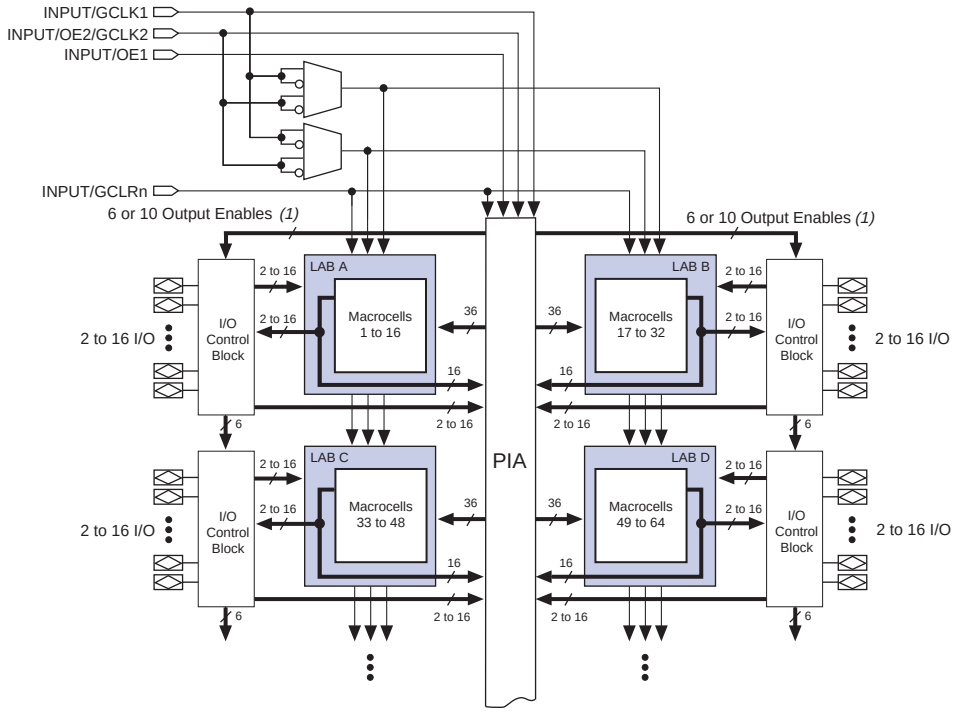
Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000A devices.

Figure 1. MAX 7000A Device Block Diagram



Note:

(1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables. EPM7512AE devices have 10 output enables.

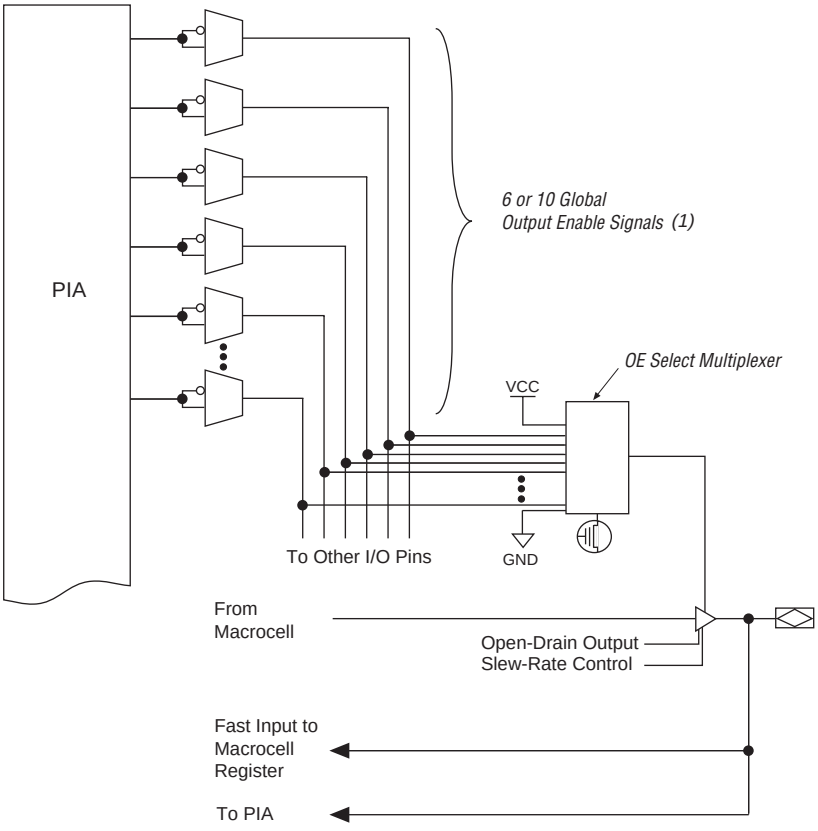
Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Figure 6. I/O Control Block of MAX 7000A Devices



Note:

(1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enable signals. EPM7512AE devices have 10 output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The MAX 7000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Table 8. MAX 7000A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO. The USERCODE instruction is available for MAX 7000AE devices only
UESCODE	These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be shifted out of TDO. UESCODE instructions are available for EPM7128A and EPM7256A devices only.
ISP Instructions	These instructions are used when programming MAX 7000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam STAPL File, JBC File, or SVF File via an embedded processor or test equipment.

The instruction register length of MAX 7000A devices is 10 bits. The user electronic signature (UES) register length in MAX 7000A devices is 16 bits. The MAX 7000AE USERCODE register length is 32 bits. Tables 9 and 10 show the boundary-scan register length and device IDCODE information for MAX 7000A devices.

Table 9. MAX 7000A Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032AE	96
EPM7064AE	192
EPM7128A	288
EPM7128AE	288
EPM7256A	480
EPM7256AE	480
EPM7512AE	624

Table 10. 32-Bit MAX 7000A Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPM7032AE	0001	0111 0000 0011 0010	00001101110	1
EPM7064AE	0001	0111 0000 0110 0100	00001101110	1
EPM7128A	0000	0111 0001 0010 1000	00001101110	1
EPM7128AE	0001	0111 0001 0010 1000	00001101110	1
EPM7256A	0000	0111 0010 0101 0110	00001101110	1
EPM7256AE	0001	0111 0010 0101 0110	00001101110	1
EPM7512AE	0001	0111 0101 0001 0010	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST.

Figure 8 shows timing information for the JTAG signals.

Figure 8. MAX 7000A JTAG Waveforms

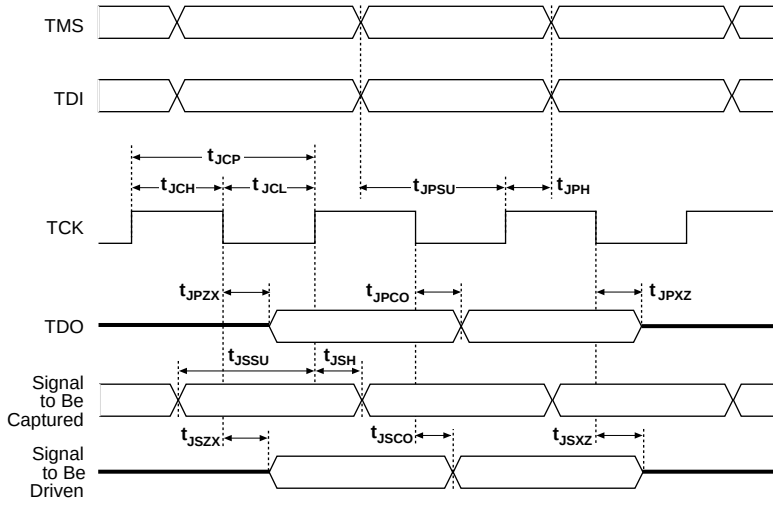


Table 11 shows the JTAG timing parameters and values for MAX 7000A devices.

Table 11. JTAG Timing Parameters & Values for MAX 7000A Devices Note (1)

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

Note:
(1) Timing parameters shown in this table apply for all specified VCCIO levels.

Figure 12. MAX 7000A Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

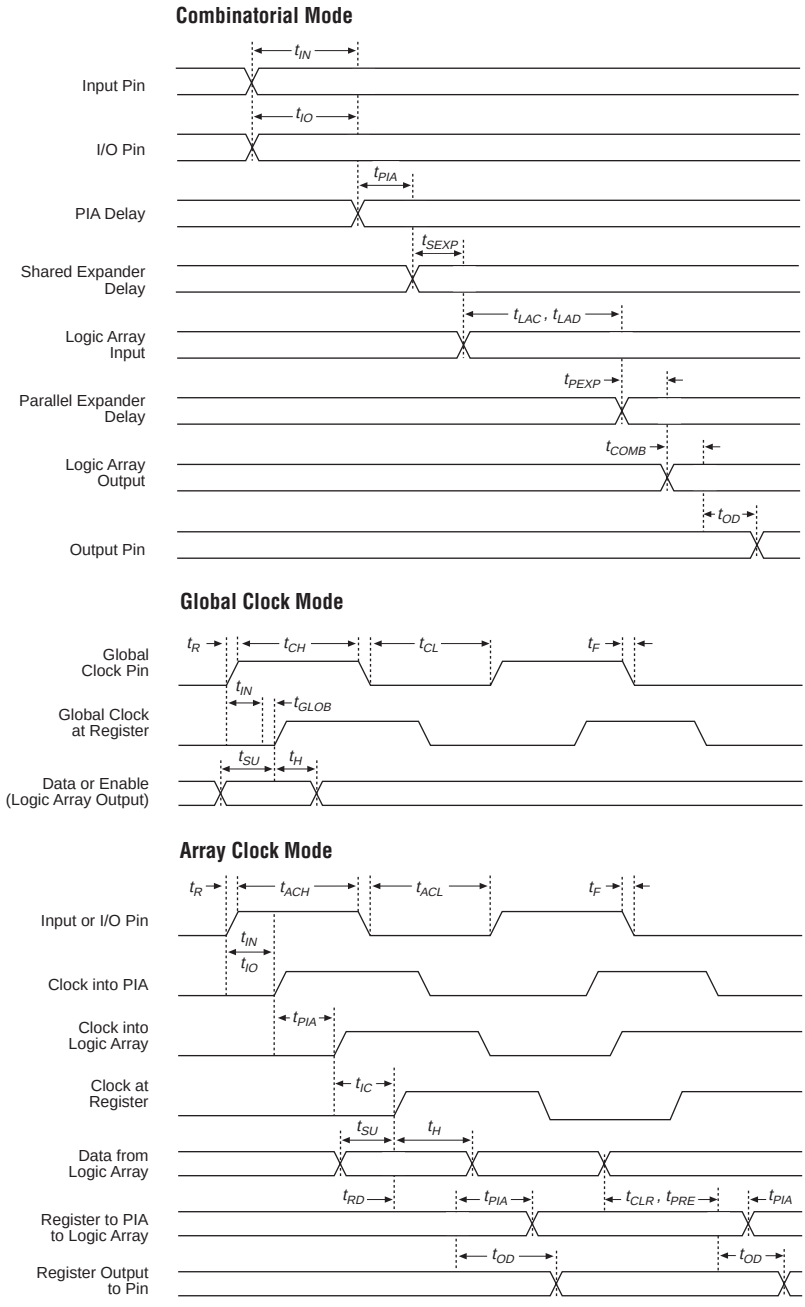


Table 20. EPM7064AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			1.0		1.5		2.2	ns
t_{PRE}	Register preset time			1.3		2.1		2.9	ns
t_{CLR}	Register clear time			1.3		2.1		2.9	ns
t_{PIA}	PIA delay	*(2)*		1.0		1.7		2.3	ns
t_{LPA}	Low-power adder	*(6)*		3.5		4.0		5.0	ns

Table 21. EPM7128AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		5.0		7.5		10	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		5.0		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	3.3		4.9		6.6		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.4	1.0	5.0	1.0	6.6	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.8		2.8		3.8		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.9	1.0	7.1	1.0	9.4	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		5.2		7.7		10.2	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	192.3		129.9		98.0		MHz
t_{ACNT}	Minimum array clock period	*(2)*		5.2		7.7		10.2	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	192.3		129.9		98.0		MHz

Table 22. EPM7128AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{EN}	Register enable time			0.7		1.0		1.3	ns
t_{GLOB}	Global control delay			1.1		1.6		2.0	ns
t_{PRE}	Register preset time			1.4		2.0		2.7	ns
t_{CLR}	Register clear time			1.4		2.0		2.7	ns
t_{PIA}	PIA delay	*(2)*		1.4		2.0		2.6	ns
t_{LPA}	Low-power adder	*(6)*		4.0		4.0		5.0	ns

Table 25. EPM7512AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		7.5		10.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		7.5		10.0		12.0	ns
t_{SU}	Global clock setup time	*(2)*	5.6		7.6		9.1		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	4.7	1.0	6.3	1.0	7.5	ns
t_{CH}	Global clock high time		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time	*(2)*	2.5		3.5		4.1		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	7.8	1.0	10.4	1.0	12.5	ns
t_{ACH}	Array clock high time		3.0		4.0		5.0		ns
t_{ACL}	Array clock low time		3.0		4.0		5.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		4.0		5.0		ns
t_{CNT}	Minimum global clock period	*(2)*		8.6		11.5		13.9	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	116.3		87.0		71.9		MHz
t_{ACNT}	Minimum array clock period	*(2)*		8.6		11.5		13.9	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	116.3		87.0		71.9		MHz

Table 26. EPM7512AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{IC}	Array clock delay			1.8		2.3		2.9	ns
t_{EN}	Register enable time			1.0		1.3		1.7	ns
t_{GLOB}	Global control delay			1.7		2.2		2.7	ns
t_{PRE}	Register preset time			1.0		1.4		1.7	ns
t_{CLR}	Register clear time			1.0		1.4		1.7	ns
t_{PIA}	PIA delay	*(2)*		3.0		4.0		4.8	ns
t_{LPA}	Low-power adder	*(6)*		4.5		5.0		5.0	ns

Table 27. EPM7128A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		6.0		7.5		10.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		6.0		7.5		10.0		12.0	ns
t_{SU}	Global clock setup time	*(2)*	4.2		5.3		7.0		8.5		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.7	1.0	4.6	1.0	6.1	1.0	7.3	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.9		2.4		3.1		3.8		ns
t_{AH}	Array clock hold time	*(2)*	1.5		2.2		3.3		4.3		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	6.0	1.0	7.5	1.0	10.0	1.0	12.0	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		5.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		5.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		3.0		4.0		5.0		ns
t_{CNT}	Minimum global clock period	*(2)*		6.9		8.6		11.5		13.8	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	144.9		116.3		87.0		72.5		MHz
t_{ACNT}	Minimum array clock period	*(2)*		6.9		8.6		11.5		13.8	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	144.9		116.3		87		72.5		MHz

Table 29. EPM7256A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		6.0		7.5		10.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		6.0		7.5		10.0		12.0	ns
t_{SU}	Global clock setup time	*(2)*	3.7		4.6		6.2		7.4		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	4.2	1.0	5.5	1.0	6.6	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		4.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	0.8		1.0		1.4		1.6		ns
t_{AH}	Array clock hold time	*(2)*	1.9		2.7		4.0		5.1		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	6.2	1.0	7.8	1.0	10.3	1.0	12.4	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		4.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		3.0		4.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		6.4		8.0		10.7		12.8	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	156.3		125.0		93.5		78.1		MHz
t_{ACNT}	Minimum array clock period	*(2)*		6.4		8.0		10.7		12.8	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	156.3		125.0		93.5		78.1		MHz

Table 30. EPM7256A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.4		0.5		0.6	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.4		0.5		0.6	ns
t_{FIN}	Fast input delay			2.4		3.0		3.4		3.8	ns
t_{SEXP}	Shared expander delay			2.8		3.5		4.7		5.6	ns
t_{PEXP}	Parallel expander delay			0.5		0.6		0.8		1.0	ns
t_{LAD}	Logic array delay			2.5		3.1		4.2		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.1		4.2		5.0	ns
t_{IOE}	Internal output enable delay			0.2		0.3		0.4		0.5	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.3		0.4		0.5		0.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		0.8		0.9		1.0		1.1	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.3		5.4		5.5		5.6	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		4.5		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		5.0	ns
t_{SU}	Register setup time		1.0		1.3		1.7		2.0		ns
t_{H}	Register hold time		1.7		2.4		3.7		4.7		ns
t_{FSU}	Register setup time of fast input		1.2		1.4		1.4		1.4		ns
t_{FH}	Register hold time of fast input		1.3		1.6		1.6		1.6		ns
t_{RD}	Register delay			1.6		2.0		2.7		3.2	ns

The parameters in this equation are:

MC_{TON} = Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Total number of macrocells in the design, as reported in the Report File
$\mathbf{f_{MAX}}$ = Highest clock frequency to the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 31

Table 31. MAX 7000A I_{CC} Equation Constants

Device	A	B	C
EPM7032AE	0.71	0.30	0.014
EPM7064AE	0.71	0.30	0.014
EPM7128A	0.71	0.30	0.014
EPM7128AE	0.71	0.30	0.014
EPM7256A	0.71	0.30	0.014
EPM7256AE	0.71	0.30	0.014
EPM7512AE	0.71	0.30	0.014

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 17. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

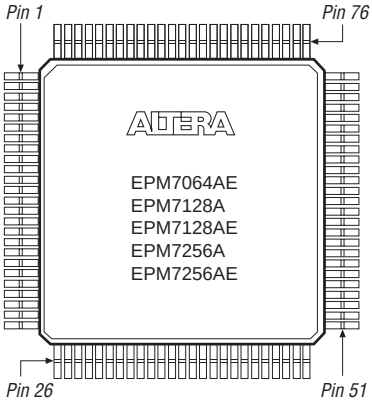


Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

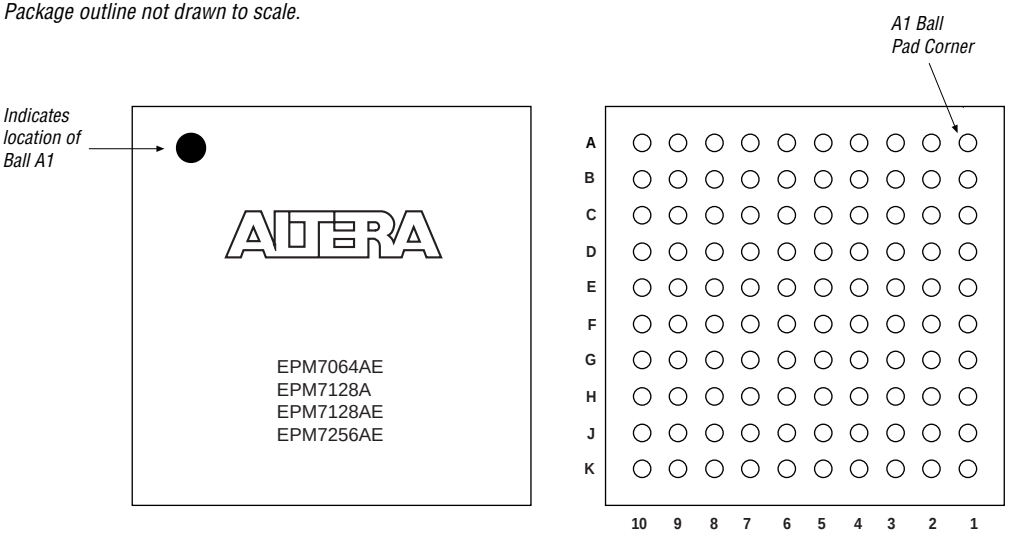


Figure 21. 208-Pin PQFP Package Pin-Out Diagram

Package outline not drawn to scale.

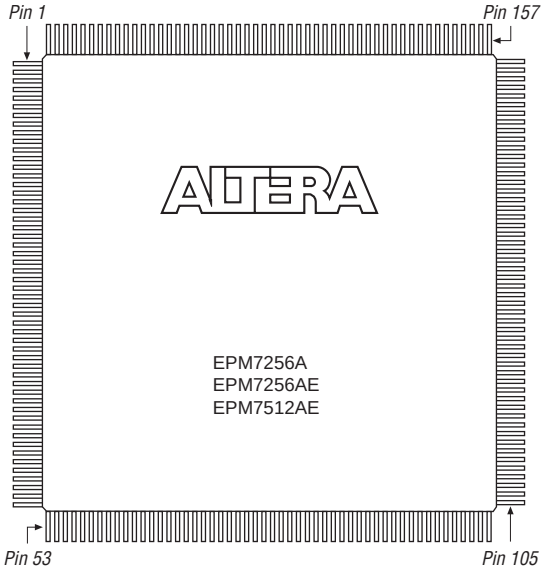
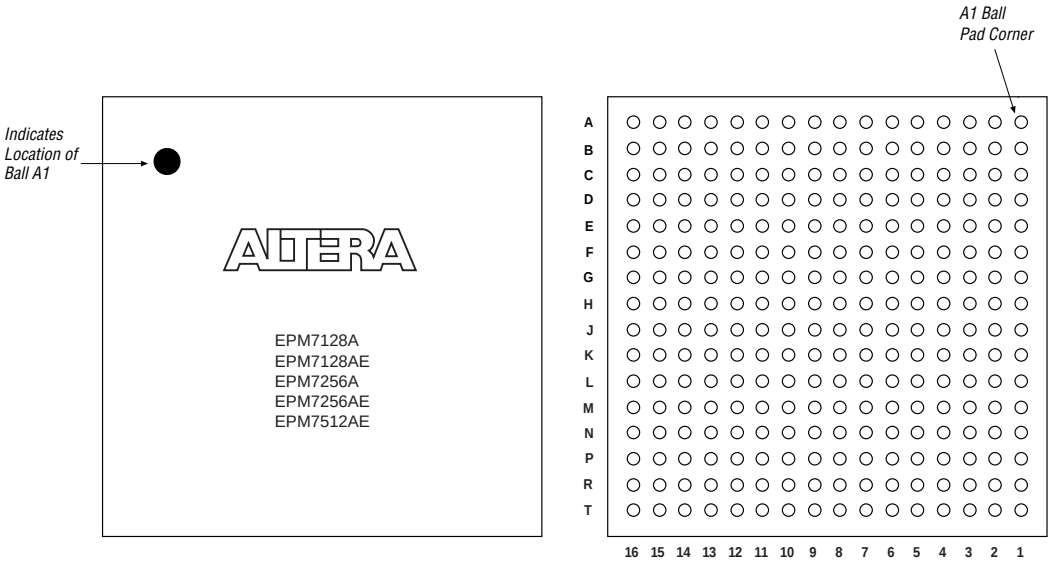


Figure 23. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5 supersedes information published in previous versions.

Version 4.5

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5:

- Updated text in the "Power Sequencing & Hot-Socketing" section.

Version 4.4

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.4:

- Added Tables 5 through 7.
- Added "Programming Sequence" on page 17 and "Programming Times" on page 18.

Version 4.3

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.3:

- Added extended temperature devices to document
- Updated Table 14.

Version 4.2

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.2:

- Removed *Note (1)* from Table 2.
- Removed *Note (4)* from Tables 3 and 4.

Version 4.1

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.1:

- Updated leakage current information in Table 15.
- Updated *Note (9)* of Table 15.
- Updated *Note (1)* of Tables 17 through 30.

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