# E·XFL

# Intel - EPM7064AETC100-10N Datasheet



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### Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

#### Applications of Embedded - CPLDs

## Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7064aetc100-10n

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- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster<sup>TM</sup> serial/universal serial bus (USB) communications cable, ByteBlasterMV<sup>TM</sup> parallel port download cable, and BitBlaster<sup>TM</sup> serial download cable, as well as programming hardware from third-party manufacturers and any Jam<sup>TM</sup> STAPL File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File- (.svf) capable in-circuit tester

# General Description

MAX 7000A (including MAX 7000AE) devices are high-density, highperformance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROMbased MAX 7000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 7000A devices in the -4, -5, -6, -7, and some -10 speed grades are compatible with the timing requirements for 33 MHz operation of the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See Table 2.

Table 2. MAX 7000A Speed Grades								
Device			Speed	Grade				
	-4	-5	-6	-7	-10	-12		
EPM7032AE	~			~	~			
EPM7064AE	$\checkmark$			$\checkmark$	~			
EPM7128A			<ul> <li>Image: A set of the set of the</li></ul>	~	~	~		
EPM7128AE		~		~	~			
EPM7256A			$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$		
EPM7256AE		$\checkmark$		$\checkmark$	$\checkmark$			
EPM7512AE				$\checkmark$	$\checkmark$	<ul> <li>Image: A set of the set of the</li></ul>		

The MAX 7000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices including PALs, GALs, and 22V10s devices. MAX 7000A devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, Ultra FineLine BGA, PQFP, and TQFP packages. See Table 3 and Table 4.

Table 3. MAX 700	OA Maximum U	lser I/O Pins	Note (1)			
Device	44-Pin PLCC	44-Pin TQFP	49-Pin Ultra FineLine BGA (2)	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine BGA (3)
EPM7032AE	36	36				
EPM7064AE	36	36	41		68	68
EPM7128A				68	84	84
EPM7128AE				68	84	84
EPM7256A					84	
EPM7256AE					84	84
EPM7512AE						

Table 4. MAX 7000A Maximum User I/O Pins     Note (1)									
Device	144-Pin TQFP	169-Pin Ultra FineLine BGA <i>(2)</i>	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA (3)				
EPM7032AE									
EPM7064AE									
EPM7128A	100				100				
EPM7128AE	100	100			100				
EPM7256A	120		164		164				
EPM7256AE	120		164		164				
EPM7512AE	120		176	212	212				

#### Notes to tables:

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.
- (2) All Ultra FineLine BGA packages are footprint-compatible via the SameFrame<sup>TM</sup> feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.
- (3) All FineLine BGA packages are footprint-compatible via the SameFrame feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.

MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000A devices contain from 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and highspeed parallel expander product terms, providing up to 32 product terms per macrocell.

MAX 7000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5-V, 3.3-V, and 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems.

MAX 7000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

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For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*. For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000A devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in a MAX 7000AE device may be set to either a high or low state. This power-up state is specified at design entry. Upon power-up, each register in EPM7128A and EPM7256A devices are set to a low state.

All MAX 7000A I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (as low as 2.5 ns) input setup time.

## **Expander Product Terms**

Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000A architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ( $t_{SEXP}$ ) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.



Shareable expanders can be shared by any or all macrocells in an LAB.



Figure 5. MAX 7000A PIA Routing



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

## I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or  $V_{CC}$ . Figure 6 shows the I/O control block for MAX 7000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

# SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ballcount packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 7).





Printed Circuit Board Designed for 256-Pin FineLine BGA Package



 

 100-Pin FineLine BGA Package (Reduced I/O Count or Logic Requirements)
 256-Pin FineLine BGA Package (Increased I/O Count or Logic Requirements)



For more information on using the Jam STAPL language, see *Application Note 88* (Using the Jam Language for ISP & ICR via an Embedded Processor) and *Application Note 122* (Using Jam STAPL for ISP & ICR via an Embedded *Processor*).

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

# **Programming Sequence**

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

- 1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
- 2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
- 3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
- 4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
- 5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
- 6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

# Programmable Speed/Power Control

MAX 7000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000A device for either high-speed (i.e., with the Turbo Bit<sup>TM</sup> option turned on) or low-power operation (i.e., with the Turbo Bit option turned off). As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ( $t_{LPA}$ ) for the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $\mathbf{t}_{ACL}$ , and  $\mathbf{t_{CPPW}}$  parameters.

# Output Configuration

MAX 7000A device outputs can be programmed to meet a variety of system-level requirements.

# MultiVolt I/O Interface

The MAX 7000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000A devices to connect to systems with differing supply voltages. MAX 7000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V<sub>CCIO</sub> levels lower than 3.0 V incur a slightly greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ . Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 12 describes the MAX 7000A MultiVolt I/O support.

Table 12. MAX 7000A MultiVolt I/O Support									
V <sub>CCIO</sub> Voltage	Inp	ut Signal	(V)	Out	put Signa	I (V)			
	2.5	3.3	5.0	2.5	3.3	5.0			
2.5	~	~	~	$\checkmark$					
3.3	$\checkmark$	$\checkmark$	$\checkmark$		$\checkmark$	$\checkmark$			

Power Sequencing & Hot-Socketing	Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The $\rm V_{CCIO}$ and $\rm V_{CCINT}$ power planes can be powered in any order.
	Signals can be driven into MAX 7000AE devices before and during power- up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.
	MAX 7000AE device I/O pins will not source or sink more than 300 $\mu A$ of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the OE1 and GLCRn pins. The OE1 and GLCRn pins can be driven up to 3.6 V during hot-socketing. After V <sub>CCINT</sub> and V <sub>CCIO</sub> reach the recommended operating conditions, these two pins are 5.0-V tolerant.
	EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.
Design Security	All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.
Generic Testing	MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9. Test patterns can be used and then erased during early stages of the production flow.

Table 1	4. MAX 7000A Device Recomm	ended Operating Conditions			
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCINT</sub>	Supply voltage for internal logic and input buffers	(3), (13)	3.0	3.6	V
V <sub>CCIO</sub>	Supply voltage for output drivers, 3.3-V operation	(3)	3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation	(3)	2.3	2.7	V
V <sub>CCISP</sub>	Supply voltage during in- system programming		3.0	3.6	V
VI	Input voltage	(4)	-0.5	5.75	V
Vo	Output voltage		0	V <sub>CCIO</sub>	V
T <sub>A</sub>	Ambient temperature	Commercial range	0	70	°C
		Industrial range (5)	-40	85	°C
Τ <sub>J</sub>	Junction temperature	Commercial range	0	90	°C
		Industrial range (5)	-40	105	°C
		Extended range (5)	-40	130	°C
t <sub>R</sub>	Input rise time			40	ns
t <sub>F</sub>	Input fall time			40	ns

Figure 11. MAX 7000A Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 12 shows the timing relationship between internal and external delay parameters.



See *Application Note 94 (Understanding MAX 7000 Timing)* for more information.

## Figure 12. MAX 7000A Switching Waveforms



Tables 17 through 30 show EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, EPM7512AE, EPM7128A, and EPM7256A timing information.

Table 1	7. EPM7032AE External Timi	ng Parameters	Note (	(1)					
Symbol	Parameter	Conditions			Speed	Grade			Unit
			-	4	-	7	-10		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t <sub>SU</sub>	Global clock setup time	(2)	2.9		4.7		6.3		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t <sub>CH</sub>	Global clock high time		2.0		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.6		2.5		3.6		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.3		0.5		0.5		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.4	ns
t <sub>ACH</sub>	Array clock high time		2.0		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.0		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		4.4		7.2		9.7	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	227.3		138.9		103.1		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		4.4		7.2		9.7	ns
facnt	Maximum internal array clock frequency	(2), (4)	227.3		138.9		103.1		MHz

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Table 1	Table 18. EPM7032AE Internal Timing Parameters (Part 2 of 2)       Note (1)									
Symbol	Parameter	Conditions			Speed	Grade			Unit	
			-	-4		-7		10		
			Min	Max	Min	Max	Min	Max		
t <sub>IC</sub>	Array clock delay			1.2		2.0		2.5	ns	
t <sub>EN</sub>	Register enable time			0.6		1.0		1.2	ns	
t <sub>GLOB</sub>	Global control delay			0.8		1.3		1.9	ns	
t <sub>PRE</sub>	Register preset time			1.2		1.9		2.6	ns	
t <sub>CLR</sub>	Register clear time			1.2		1.9		2.6	ns	
t <sub>PIA</sub>	PIA delay	(2)		0.9		1.5		2.1	ns	
t <sub>LPA</sub>	Low-power adder	(6)		2.5		4.0		5.0	ns	

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Table 22	Table 22. EPM7128AE Internal Timing Parameters (Part 2 of 2)       Note (1)									
Symbol	Parameter	Conditions			Speed	Grade			Unit	
				-5		-7		-10		
			Min	Max	Min	Max	Min	Max		
t <sub>EN</sub>	Register enable time			0.7		1.0		1.3	ns	
t <sub>GLOB</sub>	Global control delay			1.1		1.6		2.0	ns	
t <sub>PRE</sub>	Register preset time			1.4		2.0		2.7	ns	
t <sub>CLR</sub>	Register clear time			1.4		2.0		2.7	ns	
t <sub>PIA</sub>	PIA delay	(2)		1.4		2.0		2.6	ns	
t <sub>LPA</sub>	Low-power adder	(6)		4.0		4.0		5.0	ns	

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Symbol	Parameter	Conditions			Speed	Grade			Unit
-			-	5	-	7	-	10	
			Min	Max	Min	Max	Min	Max	
t <sub>IN</sub>	Input pad and buffer delay			0.7		0.9		1.2	ns
t <sub>IO</sub>	I/O input pad and buffer delay			0.7		0.9		1.2	ns
t <sub>FIN</sub>	Fast input delay			2.4		2.9		3.4	ns
t <sub>SEXP</sub>	Shared expander delay			2.1		2.8		3.7	ns
t <sub>PEXP</sub>	Parallel expander delay			0.3		0.5		0.6	ns
t <sub>LAD</sub>	Logic array delay			1.7		2.2		2.8	ns
t <sub>LAC</sub>	Logic control array delay			0.8		1.0		1.3	ns
t <sub>IOE</sub>	Internal output enable delay			0.0		0.0		0.0	ns
t <sub>OD1</sub>	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		0.9		1.2		1.6	ns
t <sub>OD2</sub>	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		1.4		1.7		2.1	ns
t <sub>OD3</sub>	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		5.9		6.2		6.6	ns
t <sub>ZX1</sub>	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		4.0		5.0	ns
t <sub>ZX2</sub>	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		4.5		5.5	ns
t <sub>ZX3</sub>	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3 V$	C1 = 35 pF		9.0		9.0		10.0	ns
t <sub>XZ</sub>	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t <sub>SU</sub>	Register setup time		1.5		2.1		2.9		ns
t <sub>H</sub>	Register hold time		0.7		0.9		1.2		ns
t <sub>FSU</sub>	Register setup time of fast input		1.1		1.6		1.6		ns
t <sub>FH</sub>	Register hold time of fast input		1.4		1.4		1.4		ns
t <sub>RD</sub>	Register delay			0.9		1.2		1.6	ns
t <sub>COMB</sub>	Combinatorial delay			0.5		0.8		1.2	ns

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Symbol	Parameter	Conditions			Speed	Grade			Unit
			-	7	-'	10		12	
			Min	Max	Min	Max	Min	Max	1
t <sub>IN</sub>	Input pad and buffer delay			0.7		0.9		1.0	ns
t <sub>IO</sub>	I/O input pad and buffer delay			0.7		0.9		1.0	ns
t <sub>FIN</sub>	Fast input delay			3.1		3.6		4.1	ns
t <sub>SEXP</sub>	Shared expander delay			2.7		3.5		4.4	ns
t <sub>PEXP</sub>	Parallel expander delay			0.4		0.5		0.6	ns
t <sub>LAD</sub>	Logic array delay			2.2		2.8		3.5	ns
t <sub>LAC</sub>	Logic control array delay			1.0		1.3		1.7	ns
t <sub>IOE</sub>	Internal output enable delay			0.0		0.0		0.0	ns
t <sub>OD1</sub>	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		1.0		1.5		1.7	ns
t <sub>OD2</sub>	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		1.5		2.0		2.2	ns
t <sub>OD3</sub>	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		6.0		6.5		6.7	ns
t <sub>ZX1</sub>	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		5.0		5.0	ns
t <sub>ZX2</sub>	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		5.5		5.5	ns
t <sub>ZX3</sub>	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3 V$	C1 = 35 pF		9.0		10.0		10.0	ns
t <sub>XZ</sub>	Output buffer disable delay	C1 = 5 pF		4.0		5.0		5.0	ns
t <sub>SU</sub>	Register setup time		2.1		3.0		3.5		ns
t <sub>H</sub>	Register hold time		0.6		0.8		1.0		ns
t <sub>FSU</sub>	Register setup time of fast input		1.6		1.6		1.6		ns
t <sub>FH</sub>	Register hold time of fast input		1.4		1.4		1.4		ns
t <sub>RD</sub>	Register delay			1.3		1.7		2.1	ns
t <sub>COMB</sub>	Combinatorial delay			0.6		0.8		1.0	ns

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		1
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		6.0		7.5		10.0		12.0	ns
t <sub>PD2</sub>	I/O input to non- registered output	C1 = 35 pF (2)		6.0		7.5		10.0		12.0	ns
t <sub>SU</sub>	Global clock setup time	(2)	4.2		5.3		7.0		8.5		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.7	1.0	4.6	1.0	6.1	1.0	7.3	ns
t <sub>CH</sub>	Global clock high time		3.0		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.9		2.4		3.1		3.8		ns
t <sub>AH</sub>	Array clock hold time	(2)	1.5		2.2		3.3		4.3		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	6.0	1.0	7.5	1.0	10.0	1.0	12.0	ns
t <sub>ACH</sub>	Array clock high time		3.0		3.0		4.0		5.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		3.0		4.0		5.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	3.0		3.0		4.0		5.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		6.9		8.6		11.5		13.8	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	144.9		116.3		87.0		72.5		MHz
t <sub>acnt</sub>	Minimum array clock period	(2)		6.9		8.6		11.5		13.8	ns
f <sub>acnt</sub>	Maximum internal array clock frequency	(2), (4)	144.9		116.3		87		72.5		MHz

#### Figure 22. 256-Pin BGA Package Pin-Out Diagram

Package outline not drawn to scale.

