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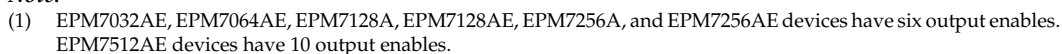
Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7064aetc100-4



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For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000A devices. As shown in [Figure 1](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figure 2](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in a MAX 7000AE device may be set to either a high or low state. This power-up state is specified at design entry. Upon power-up, each register in EPM7128A and EPM7256A devices are set to a low state.

All MAX 7000A I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (as low as 2.5 ns) input setup time.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

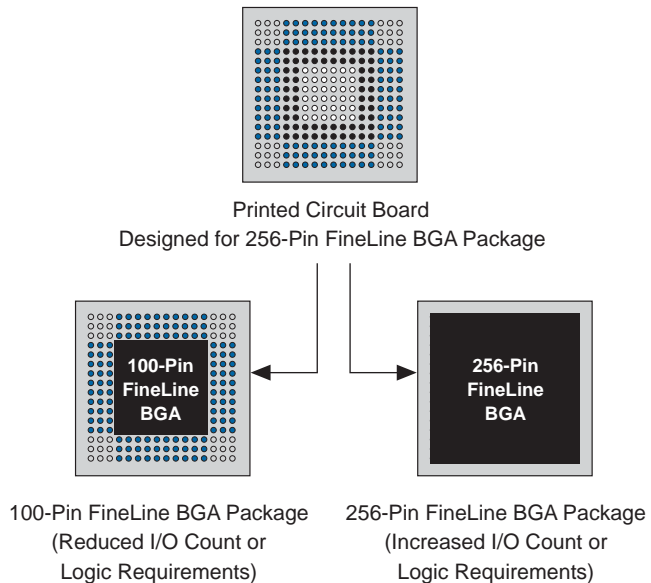
Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders, and the highest-numbered macrocell can only borrow them. [Figure 4](#) shows how parallel expanders can be borrowed from a neighboring macrocell.

SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 7](#)).

Figure 7. SameFrame Pin-Out Example



Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000A Device

The time required to program a single MAX 7000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
 t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
 $Cycle_{PTCK}$ = Number of TCK cycles to program a device
 f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
 t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
 $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

The programming times described in [Tables 5 through 7](#) are associated with the worst-case method using the enhanced ISP algorithm.

Table 5. MAX 7000A t_{PULSE} & $Cycle_{TCK}$ Values

Device	Programming		Stand-Alone Verification	
	t_{PPULSE} (s)	$Cycle_{PTCK}$	t_{VPULSE} (s)	$Cycle_{VTCK}$
EPM7032AE	2.00	55,000	0.002	18,000
EPM7064AE	2.00	105,000	0.002	35,000
EPM7128AE	2.00	205,000	0.002	68,000
EPM7256AE	2.00	447,000	0.002	149,000
EPM7512AE	2.00	890,000	0.002	297,000
EPM7128A (1)	5.11	832,000	0.03	528,000
EPM7256A (1)	6.43	1,603,000	0.03	1,024,000

[Tables 6 and 7](#) show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 6. MAX 7000A In-System Programming Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032AE	2.01	2.01	2.03	2.06	2.11	2.28	2.55	3.10	s
EPM7064AE	2.01	2.02	2.05	2.11	2.21	2.53	3.05	4.10	s
EPM7128AE	2.02	2.04	2.10	2.21	2.41	3.03	4.05	6.10	s
EPM7256AE	2.05	2.09	2.23	2.45	2.90	4.24	6.47	10.94	s
EPM7512AE	2.09	2.18	2.45	2.89	3.78	6.45	10.90	19.80	s
EPM7128A (1)	5.19	5.27	5.52	5.94	6.77	9.27	13.43	21.75	s
EPM7256A (1)	6.59	6.75	7.23	8.03	9.64	14.45	22.46	38.49	s

The instruction register length of MAX 7000A devices is 10 bits. The user electronic signature (UES) register length in MAX 7000A devices is 16 bits. The MAX 7000AE USERCODE register length is 32 bits. [Tables 9 and 10](#) show the boundary-scan register length and device IDCODE information for MAX 7000A devices.

Table 9. MAX 7000A Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032AE	96
EPM7064AE	192
EPM7128A	288
EPM7128AE	288
EPM7256A	480
EPM7256AE	480
EPM7512AE	624

Table 10. 32-Bit MAX 7000A Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) <i>(2)</i>
EPM7032AE	0001	0111 0000 0011 0010	00001101110	1
EPM7064AE	0001	0111 0000 0110 0100	00001101110	1
EPM7128A	0000	0111 0001 0010 1000	00001101110	1
EPM7128AE	0001	0111 0001 0010 1000	00001101110	1
EPM7256A	0000	0111 0010 0101 0110	00001101110	1
EPM7256AE	0001	0111 0010 0101 0110	00001101110	1
EPM7512AE	0001	0111 0101 0001 0010	00001101110	1

Notes:

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information on JTAG BST.

Power Sequencing & Hot-Socketing

Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000AE devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.

MAX 7000AE device I/O pins will not source or sink more than 300 μ A of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the OE1 and GLCRn pins. The OE1 and GLCRn pins can be driven up to 3.6 V during hot-socketing. After V_{CCINT} and V_{CCIO} reach the recommended operating conditions, these two pins are 5.0-V tolerant.

EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.

Design Security

All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 9](#). Test patterns can be used and then erased during early stages of the production flow.

Table 15. MAX 7000A Device DC Operating Conditions *Note (6)*

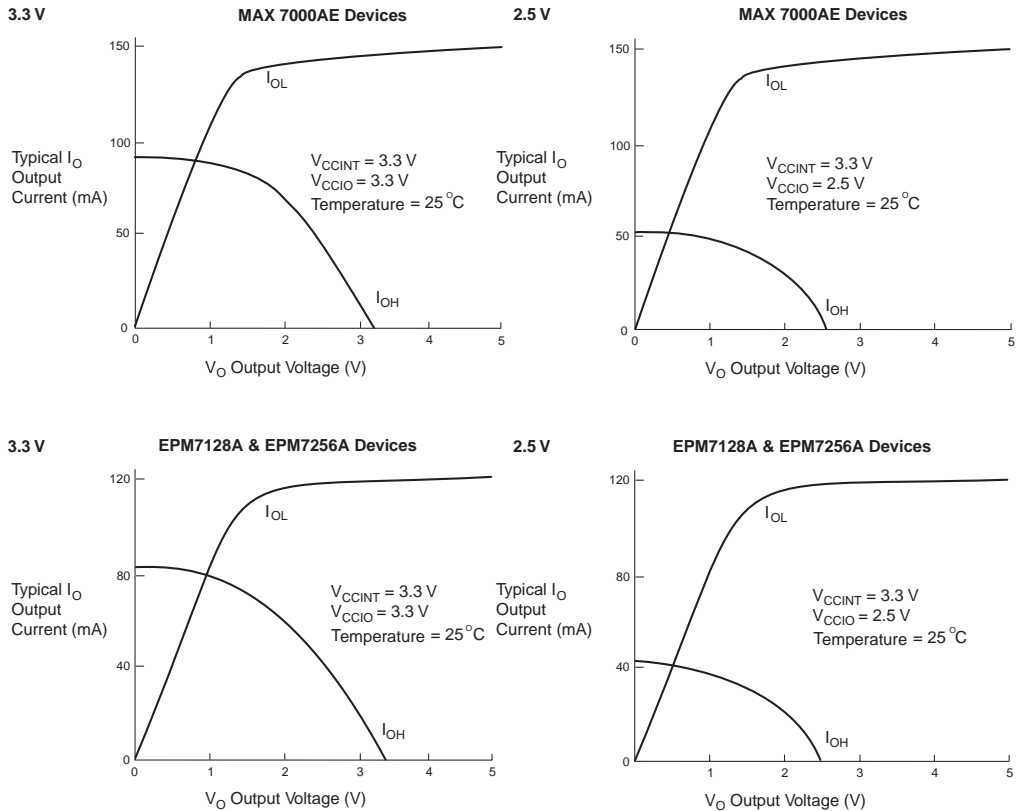
Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		1.7	5.75	V
V_{IL}	Low-level input voltage		-0.5	0.8	V
V_{OH}	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (7)	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (7)	$V_{CCIO} - 0.2$		V
	2.5-V high-level output voltage	$I_{OH} = -100$ μ A DC, $V_{CCIO} = 2.30$ V (7)	2.1		V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (7)	2.0		V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (7)	1.7		V
V_{OL}	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 3.00$ V (8)		0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)		0.2	V
	2.5-V low-level output voltage	$I_{OL} = 100$ μ A DC, $V_{CCIO} = 2.30$ V (8)		0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (8)		0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (8)		0.7	V
I_I	Input leakage current	$V_I = -0.5$ to 5.5 V (9)	-10	10	μ A
I_{OZ}	Tri-state output off-state current	$V_I = -0.5$ to 5.5 V (9)	-10	10	μ A
R_{ISP}	Value of I/O pin pull-up resistor during in-system programming or during power-up	$V_{CCIO} = 3.0$ to 3.6 V (10)	20	50	k Ω
		$V_{CCIO} = 2.3$ to 2.7 V (10)	30	80	k Ω
		$V_{CCIO} = 2.3$ to 3.6 V (11)	20	74	k Ω

Table 16. MAX 7000A Device Capacitance *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		8	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		8	pF

Figure 10 shows the typical output drive characteristics of MAX 7000A devices.

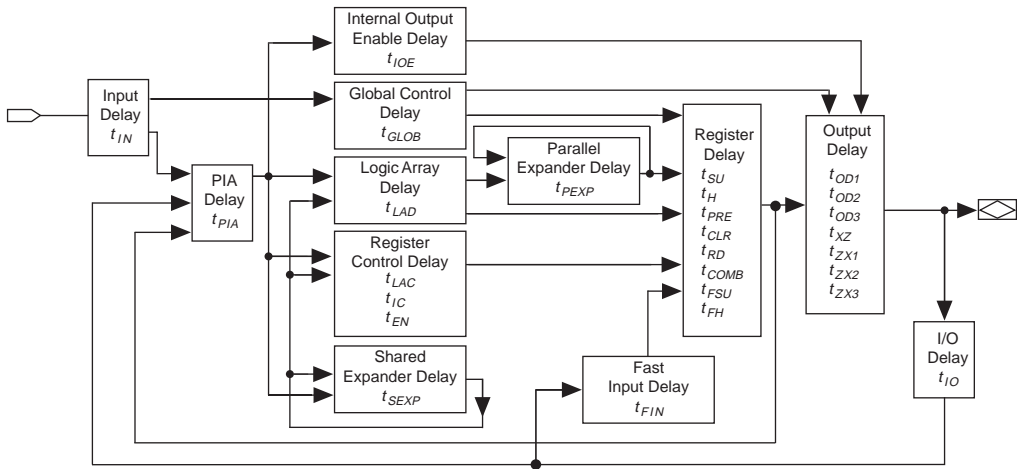
Figure 10. Output Drive Characteristics of MAX 7000A Devices



Timing Model

MAX 7000A device timing can be analyzed with the Altera software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 11. MAX 7000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 11. MAX 7000A Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 12 shows the timing relationship between internal and external delay parameters.



See [Application Note 94 \(Understanding MAX 7000 Timing\)](#) for more information.

Tables 17 through 30 show EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, EPM7512AE, EPM7128A, and EPM7256A timing information.

Table 17. EPM7032AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t _{SU}	Global clock setup time	(2)	2.9		4.7		6.3		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.6		2.5		3.6		ns
t _{AH}	Array clock hold time	(2)	0.3		0.5		0.5		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.4	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		4.4		7.2		9.7	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	227.3		138.9		103.1		MHz
t _{ACNT}	Minimum array clock period	(2)		4.4		7.2		9.7	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (4)	227.3		138.9		103.1		MHz

Table 18. EPM7032AE Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		1.2		1.5	ns
t_{IO}	I/O input pad and buffer delay			0.7		1.2		1.5	ns
t_{FIN}	Fast input delay			2.3		2.8		3.4	ns
t_{SEXP}	Shared expander delay			1.9		3.1		4.0	ns
t_{PEXP}	Parallel expander delay			0.5		0.8		1.0	ns
t_{LAD}	Logic array delay			1.5		2.5		3.3	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.8		ns
t_H	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.7		1.2		1.5	ns
t_{COMB}	Combinatorial delay			0.6		1.0		1.3	ns

Table 18. EPM7032AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IC}	Array clock delay			1.2		2.0		2.5	ns
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			0.8		1.3		1.9	ns
t_{PRE}	Register preset time			1.2		1.9		2.6	ns
t_{CLR}	Register clear time			1.2		1.9		2.6	ns
t_{PIA}	PIA delay	(2)		0.9		1.5		2.1	ns
t_{LPA}	Low-power adder	(6)		2.5		4.0		5.0	ns

Table 20. EPM7064AE Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		1.1		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.6		1.1		1.4	ns
t_{FIN}	Fast input delay			2.5		3.0		3.7	ns
t_{SEXP}	Shared expander delay			1.8		3.0		3.9	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.5		2.5		3.2	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.9		ns
t_H	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.7		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.6		0.9		1.3	ns
t_{IC}	Array clock delay			1.2		1.9		2.5	ns

Table 20. EPM7064AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			1.0		1.5		2.2	ns
t_{PRE}	Register preset time			1.3		2.1		2.9	ns
t_{CLR}	Register clear time			1.3		2.1		2.9	ns
t_{PIA}	PIA delay	(2)		1.0		1.7		2.3	ns
t_{LPA}	Low-power adder	(6)		3.5		4.0		5.0	ns

Table 21. EPM7128AE External Timing Parameters *Note (1)*

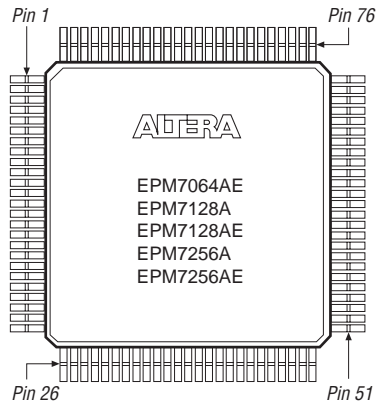
Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10	ns
t _{SU}	Global clock setup time	(2)	3.3		4.9		6.6		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.4	1.0	5.0	1.0	6.6	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.8		2.8		3.8		ns
t _{AH}	Array clock hold time	(2)	0.2		0.3		0.4		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.9	1.0	7.1	1.0	9.4	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		5.2		7.7		10.2	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	192.3		129.9		98.0		MHz
t _{ACNT}	Minimum array clock period	(2)		5.2		7.7		10.2	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (4)	192.3		129.9		98.0		MHz

Table 22. EPM7128AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{EN}	Register enable time			0.7		1.0		1.3	ns
t_{GLOB}	Global control delay			1.1		1.6		2.0	ns
t_{PRE}	Register preset time			1.4		2.0		2.7	ns
t_{CLR}	Register clear time			1.4		2.0		2.7	ns
t_{PIA}	PIA delay	(2)		1.4		2.0		2.6	ns
t_{LPA}	Low-power adder	(6)		4.0		4.0		5.0	ns

Table 24. EPM7256AE Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		0.9		1.2	ns
t_{IO}	I/O input pad and buffer delay			0.7		0.9		1.2	ns
t_{FIN}	Fast input delay			2.4		2.9		3.4	ns
t_{SEXP}	Shared expander delay			2.1		2.8		3.7	ns
t_{PEXP}	Parallel expander delay			0.3		0.5		0.6	ns
t_{LAD}	Logic array delay			1.7		2.2		2.8	ns
t_{LAC}	Logic control array delay			0.8		1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.4		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.9		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.5		2.1		2.9		ns
t_H	Register hold time		0.7		0.9		1.2		ns
t_{FSU}	Register setup time of fast input		1.1		1.6		1.6		ns
t_{FH}	Register hold time of fast input		1.4		1.4		1.4		ns
t_{RD}	Register delay			0.9		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.5		0.8		1.2	ns

Figure 17. 100-Pin TQFP Package Pin-Out Diagram*Package outline not drawn to scale.***Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram***Package outline not drawn to scale.*