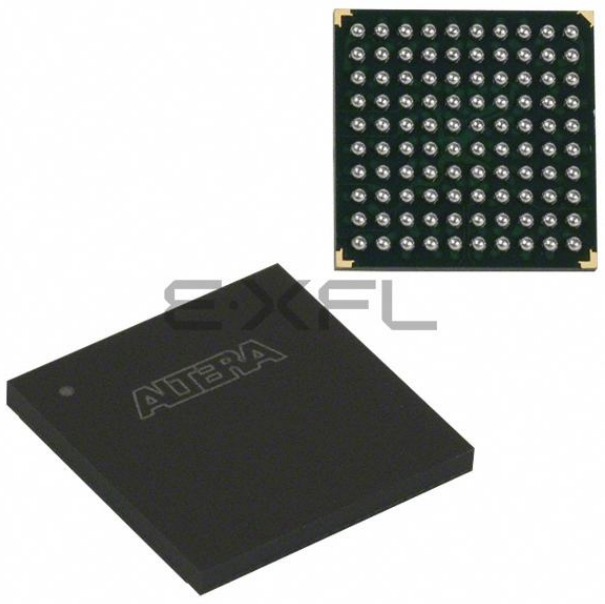


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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 10 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | 8 |
| Number of Macrocells | 128 |
| Number of Gates | 2500 |
| Number of I/O | 84 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LBGA |
| Supplier Device Package | 100-FBGA (11x11) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7128aefc100-10 |

MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000A devices contain from 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms, providing up to 32 product terms per macrocell.

MAX 7000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5-V, 3.3-V, and 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems.

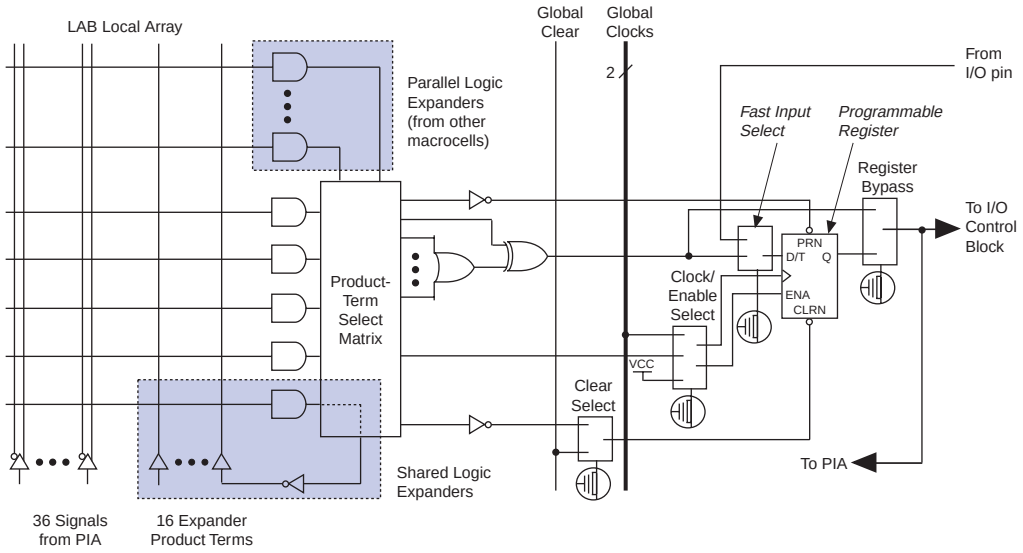
MAX 7000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

## Macrocells

MAX 7000A macrocells can be individually configured for either sequential or combinatorial logic operation. The macrocells consist of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows a MAX 7000A macrocell.

***Figure 2. MAX 7000A Macrocell***




Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

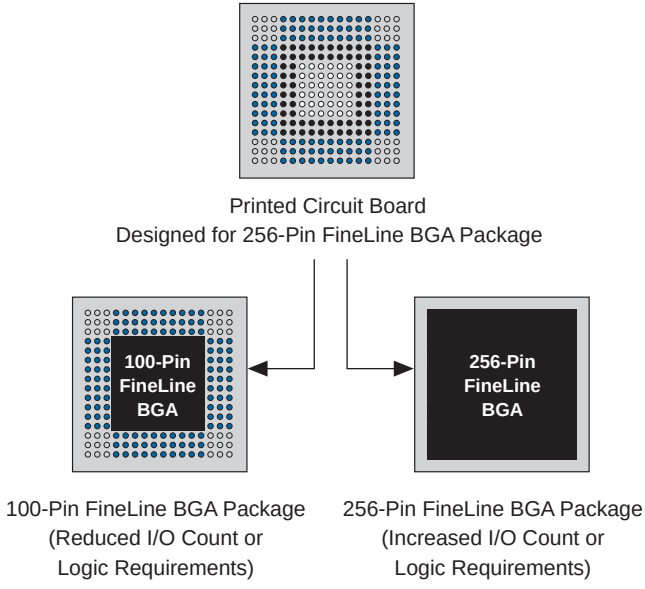
The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

## SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 7).

*Figure 7. SameFrame Pin-Out Example*



## In-System Programmability

MAX 7000A devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 kΩ.

MAX 7000AE devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is only available in EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, and EPM7512AE devices.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster serial/USB communications cable, ByteBlasterMV parallel port download cable, and BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000AE devices can be programmed with either an adaptive or constant (non-adaptive) algorithm. EPM7128A and EPM7256A device can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD 71, can be used to program MAX 7000A devices with in-circuit testers, PCs, or embedded processors.

For more information on using the Jam STAPL language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)*.

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Figure 8 shows timing information for the JTAG signals.

*Figure 8. MAX 7000A JTAG Waveforms*

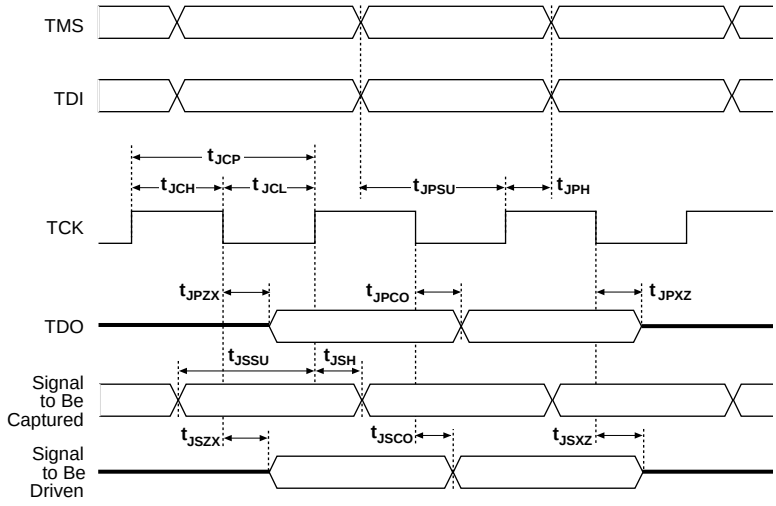



Table 11 shows the JTAG timing parameters and values for MAX 7000A devices.

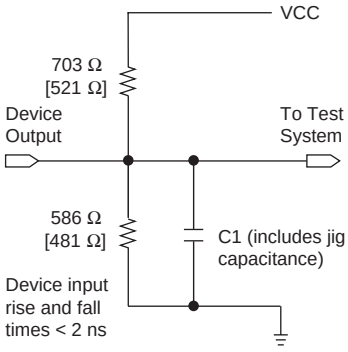
*Table 11. JTAG Timing Parameters & Values for MAX 7000A Devices* Note (1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 25 | ns |

*Note:*
(1) Timing parameters shown in this table apply for all specified VCCIO levels.

*Figure 9. MAX 7000A AC Test Conditions*

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs.*




## Operating Conditions

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000A devices.

*Table 13. MAX 7000A Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_A$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | BGA, FineLine BGA, PQFP, and TQFP packages, under bias | | 135 | ° C |

*Table 15. MAX 7000A Device DC Operating Conditions* *Note (6)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7 | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | 0.8 | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(7)* | 2.4 | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(7)* | $V_{CCIO}$ – 0.2 | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –100 µA DC, $V_{CCIO}$ = 2.30 V *(7)* | 2.1 | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(7)* | 2.0 | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(7)* | 1.7 | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 8 mA DC, $V_{CCIO}$ = 3.00 V *(8)* | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(8)* | | 0.2 | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 100 µA DC, $V_{CCIO}$ = 2.30 V *(8)* | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(8)* | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(8)* | | 0.7 | V |
| $I_I$ | Input leakage current | $V_I$ = –0.5 to 5.5 V *(9)* | –10 | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_I$ = –0.5 to 5.5 V *(9)* | –10 | 10 | µA |
| $R_{ISP}$ | Value of I/O pin pull-up resistor during in-system programming or during power-up | $V_{CCIO}$ = 3.0 to 3.6 V *(10)* | 20 | 50 | kΩ |
| | | $V_{CCIO}$ = 2.3 to 2.7 V *(10)* | 30 | 80 | kΩ |
| | | $V_{CCIO}$ = 2.3 to 3.6 V *(11)* | 20 | 74 | kΩ |

*Table 16. MAX 7000A Device Capacitance* *Note (12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

*Notes to tables:*

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) For EPM7128A and EPM7256A devices only, $V_{CC}$ must rise monotonically.
(4) In MAX 7000AE devices, all pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(5) These devices support in-system programming for –40° to 100° C. For in-system programming support between –40° and 0° C, contact Altera Applications.
(6) These values are specified under the recommended operating conditions shown in Table 14 on page 28.
(7) The parameter is measured with 50% of the outputs each sourcing the specified current. The $I_{OH}$ parameter refers to high-level TTL or CMOS output current.
(8) The parameter is measured with 50% of the outputs each sinking the specified current. The $I_{OL}$ parameter refers to low-level TTL or CMOS output current.
(9) This value is specified for normal device operation. For MAX 7000AE devices, the maximum leakage current during power-up is ±300 µA. For EPM7128A and EPM7256A devices, leakage current during power-up is not specified.
(10) For EPM7128A and EPM7256A devices, this pull-up exists while a device is programmed in-system.
(11) For MAX 7000AE devices, this pull-up exists while devices are programmed in-system and in unprogrammed devices during power-up.
(12) Capacitance is measured at 25 °C and is sample-tested only. The `OE1` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(13) The POR time for MAX 7000AE devices (except MAX 7128A and MAX 7256A devices) does not exceed 100 µs. The sufficient $V_{CCINT}$ voltage level for POR is 3.0 V. The device is fully initialized within the POR time after $V_{CCINT}$ reaches the sufficient POR voltage level.

Tables 17 through 30 show EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, EPM7512AE, EPM7128A, and EPM7256A timing information.

*Table 17. EPM7032AE External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -4 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 4.5 | | 7.5 | | 10 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 4.5 | | 7.5 | | 10 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 2.9 | | 4.7 | | 6.3 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 2.5 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 3.0 | 1.0 | 5.0 | 1.0 | 6.7 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 1.6 | | 2.5 | | 3.6 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.3 | | 0.5 | | 0.5 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 4.3 | 1.0 | 7.2 | 1.0 | 9.4 | ns |
| $t_{ACH}$ | Array clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 4.4 | | 7.2 | | 9.7 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(4)* | 227.3 | | 138.9 | | 103.1 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 4.4 | | 7.2 | | 9.7 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(4)* | 227.3 | | 138.9 | | 103.1 | | MHz |

*Table 22. EPM7128AE Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.7 | | 1.0 | | 1.4 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.7 | | 1.0 | | 1.4 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.5 | | 3.0 | | 3.4 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 2.0 | | 2.9 | | 3.8 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.7 | | 0.9 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.6 | | 2.4 | | 3.1 | ns |
| $t_{LAC}$ | Logic control array delay | | | 0.7 | | 1.0 | | 1.3 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.8 | | 1.2 | | 1.6 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 1.3 | | 1.7 | | 2.1 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.8 | | 6.2 | | 6.6 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 1.4 | | 2.1 | | 2.9 | | ns |
| $t_{H}$ | Register hold time | | 0.6 | | 1.0 | | 1.3 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.1 | | 1.6 | | 1.6 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.4 | | 1.4 | | 1.4 | | ns |
| $t_{RD}$ | Register delay | | | 0.8 | | 1.2 | | 1.6 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.5 | | 0.9 | | 1.3 | ns |
| $t_{IC}$ | Array clock delay | | | 1.2 | | 1.7 | | 2.2 | ns |

*Table 22. EPM7128AE Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{EN}$ | Register enable time | | | 0.7 | | 1.0 | | 1.3 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.1 | | 1.6 | | 2.0 | ns |
| $t_{PRE}$ | Register preset time | | | 1.4 | | 2.0 | | 2.7 | ns |
| $t_{CLR}$ | Register clear time | | | 1.4 | | 2.0 | | 2.7 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 1.4 | | 2.0 | | 2.6 | ns |
| $t_{LPA}$ | Low-power adder | *(6)* | | 4.0 | | 4.0 | | 5.0 | ns |

*Table 23. EPM7256AE External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 5.5 | | 7.5 | | 10 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 5.5 | | 7.5 | | 10 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 3.9 | | 5.2 | | 6.9 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 2.5 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 3.5 | 1.0 | 4.8 | 1.0 | 6.4 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 2.0 | | 2.7 | | 3.6 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.3 | | 0.5 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 5.4 | 1.0 | 7.3 | 1.0 | 9.7 | ns |
| $t_{ACH}$ | Array clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 5.8 | | 7.9 | | 10.5 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(4)* | 172.4 | | 126.6 | | 95.2 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 5.8 | | 7.9 | | 10.5 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(4)* | 172.4 | | 126.6 | | 95.2 | | MHz |

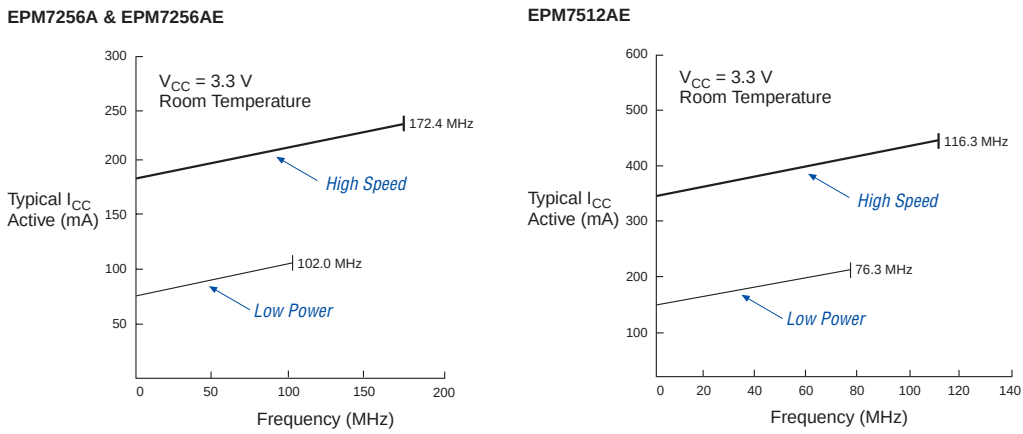
*Table 28. EPM7128A Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -12 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.6 | | 0.7 | | 0.9 | | 1.1 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.6 | | 0.7 | | 0.9 | | 1.1 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.7 | | 3.1 | | 3.6 | | 3.9 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 2.5 | | 3.2 | | 4.3 | | 5.1 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.7 | | 0.8 | | 1.1 | | 1.3 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.4 | | 3.0 | | 4.1 | | 4.9 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.4 | | 3.0 | | 4.1 | | 4.9 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.4 | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 0.9 | | 1.1 | | 1.2 | | 1.4 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.4 | | 5.6 | | 5.7 | | 5.9 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 4.5 | | 4.5 | | 5.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 1.9 | | 2.4 | | 3.1 | | 3.8 | | ns |
| $t_{H}$ | Register hold time | | 1.5 | | 2.2 | | 3.3 | | 4.3 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 0.8 | | 1.1 | | 1.1 | | 1.1 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.7 | | 1.9 | | 1.9 | | 1.9 | | ns |

*Table 30. EPM7256A Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -12 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.4 | | 3.0 | | 3.4 | | 3.8 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 2.8 | | 3.5 | | 4.7 | | 5.6 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.5 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.5 | | 3.1 | | 4.2 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.5 | | 3.1 | | 4.2 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.2 | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 0.8 | | 0.9 | | 1.0 | | 1.1 | ns |
| $t_{OD3}$ | Output buffer and pad delay slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.3 | | 5.4 | | 5.5 | | 5.6 | ns |
| $t_{ZX1}$ | Output buffer enable delay slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 4.5 | | 4.5 | | 5.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 1.3 | | 1.7 | | 2.0 | | ns |
| $t_{H}$ | Register hold time | | 1.7 | | 2.4 | | 3.7 | | 4.7 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.2 | | 1.4 | | 1.4 | | 1.4 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.3 | | 1.6 | | 1.6 | | 1.6 | | ns |
| $t_{RD}$ | Register delay | | | 1.6 | | 2.0 | | 2.7 | | 3.2 | ns |

*Figure 13. $I_{CC}$ vs. Frequency for MAX 7000A Devices (Part 2 of 2)*



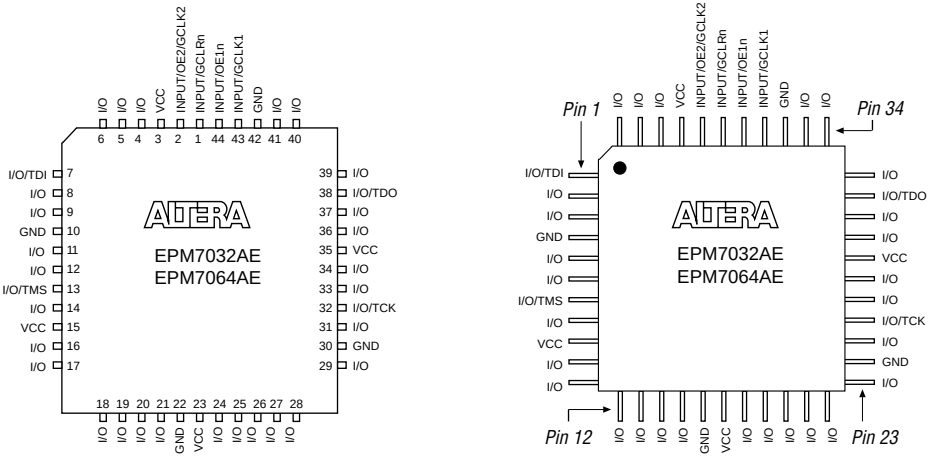

## Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information.

Figures 14 through 23 show the package pin-out diagrams for MAX 7000A devices.

*Figure 14. 44-Pin PLCC/TQFP Package Pin-Out Diagram*

*Package outlines not drawn to scale.*




44-Pin PLCC

44-Pin TQFP

*Figure 17. 100-Pin TQFP Package Pin-Out Diagram*

*Package outline not drawn to scale.*

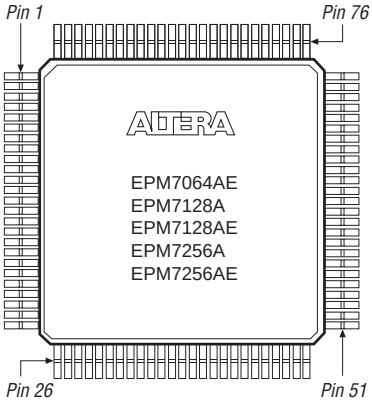



*Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram*

*Package outline not drawn to scale.*

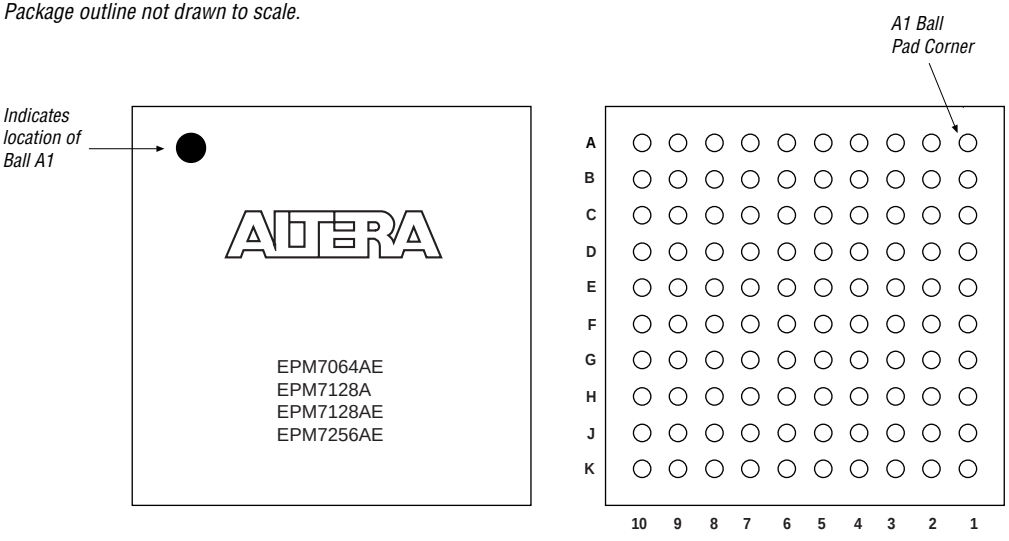


*Figure 21. 208-Pin PQFP Package Pin-Out Diagram*

*Package outline not drawn to scale.*

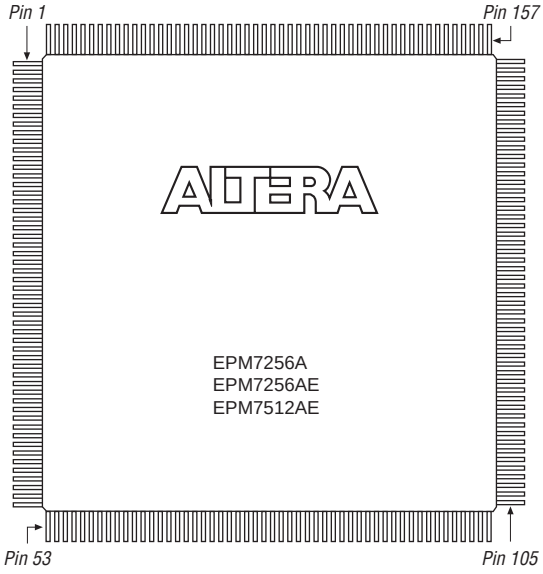
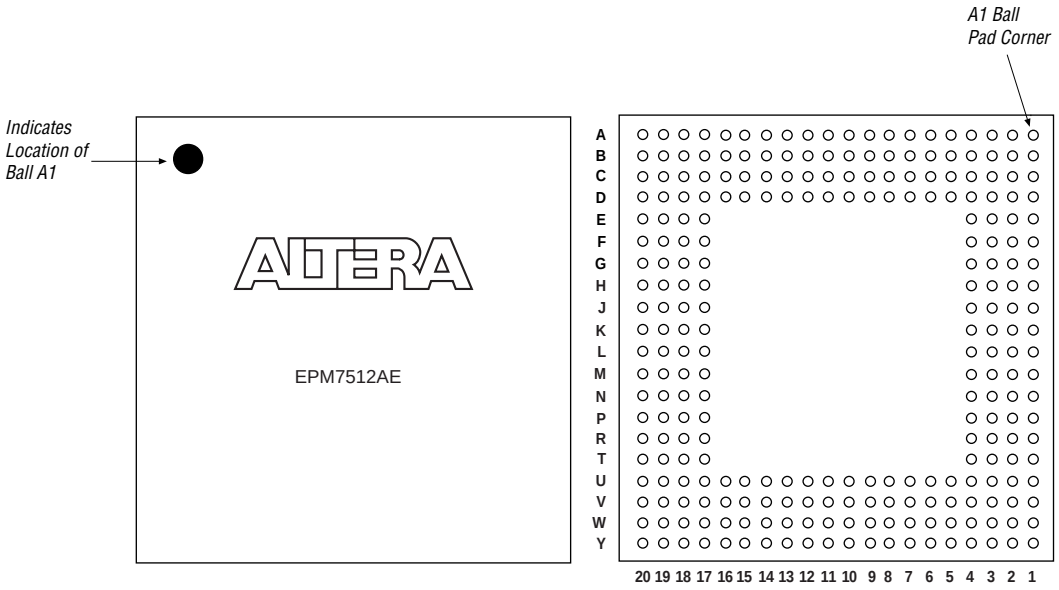


*Figure 22. 256-Pin BGA Package Pin-Out Diagram*

*Package outline not drawn to scale.*



## Version 4.3

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.3:

- Added extended temperature devices to document
- Updated Table 14.

## Version 4.2

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.2:

- Removed *Note (1)* from Table 2.
- Removed *Note (4)* from Tables 3 and 4.

## Version 4.1

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.1:

- Updated leakage current information in Table 15.
- Updated *Note (9)* of Table 15.
- Updated *Note (1)* of Tables 17 through 30.

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