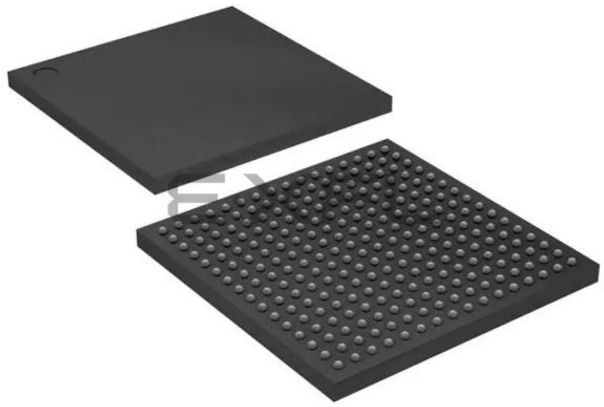
Intel - EPM7128AEFC256-5 Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	100
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128aefc256-5

Table 1. MAX 7000A Device Features

Feature	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
t_{PD} (ns)	4.5	4.5	5.0	5.5	7.5
t_{SU} (ns)	2.9	2.8	3.3	3.9	5.6
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3.0
t_{CO1} (ns)	3.0	3.1	3.4	3.5	4.7
f_{CNT} (MHz)	227.3	222.2	192.3	172.4	116.3

...and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt™ I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins

The MAX 7000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices including PALs, GALs, and 22V10s devices. MAX 7000A devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, Ultra FineLine BGA, PQFP, and TQFP packages. See Table 3 and Table 4.

Table 3. MAX 7000A Maximum User I/O Pins Note (1)

Device	44-Pin PLCC	44-Pin TQFP	49-Pin Ultra FineLine BGA (2)	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine BGA (3)
EPM7032AE	36	36				
EPM7064AE	36	36	41		68	68
EPM7128A				68	84	84
EPM7128AE				68	84	84
EPM7256A					84	
EPM7256AE					84	84
EPM7512AE						

Table 4. MAX 7000A Maximum User I/O Pins Note (1)

Device	144-Pin TQFP	169-Pin Ultra FineLine BGA (2)	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA (3)
EPM7032AE					
EPM7064AE					
EPM7128A	100				100
EPM7128AE	100	100			100
EPM7256A	120		164		164
EPM7256AE	120		164		164
EPM7512AE	120		176	212	212

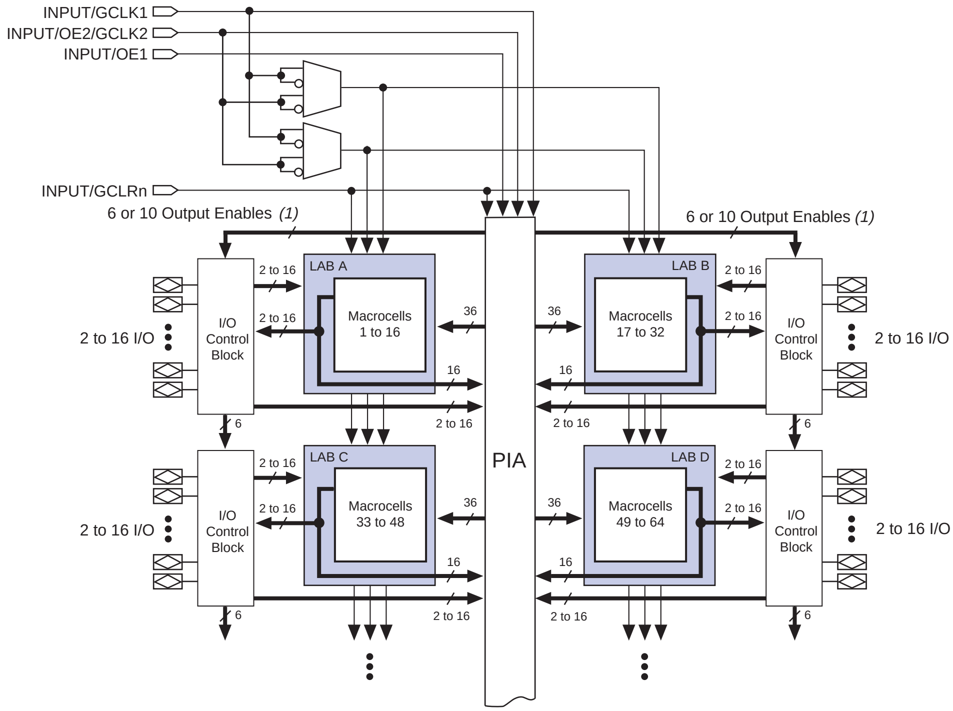
Notes to tables:

(1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

(2) All Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.

(3) All FineLine BGA packages are footprint-compatible via the SameFrame feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.

Figure 1. MAX 7000A Device Block Diagram



Note:

(1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables. EPM7512AE devices have 10 output enables.

Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

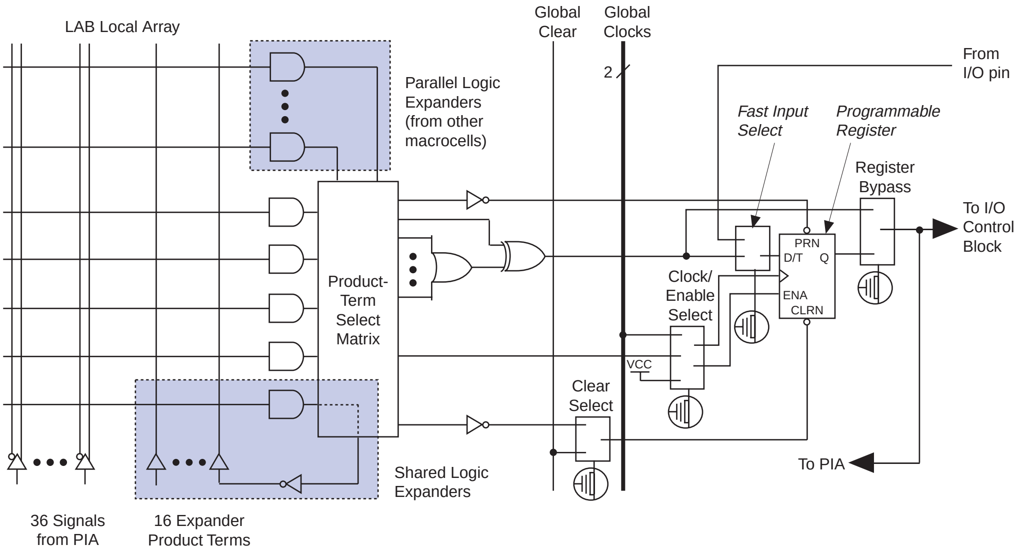
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Macrocells

MAX 7000A macrocells can be individually configured for either sequential or combinatorial logic operation. The macrocells consist of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows a MAX 7000A macrocell.

Figure 2. MAX 7000A Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the `OR` and `XOR` gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

Expander Product Terms

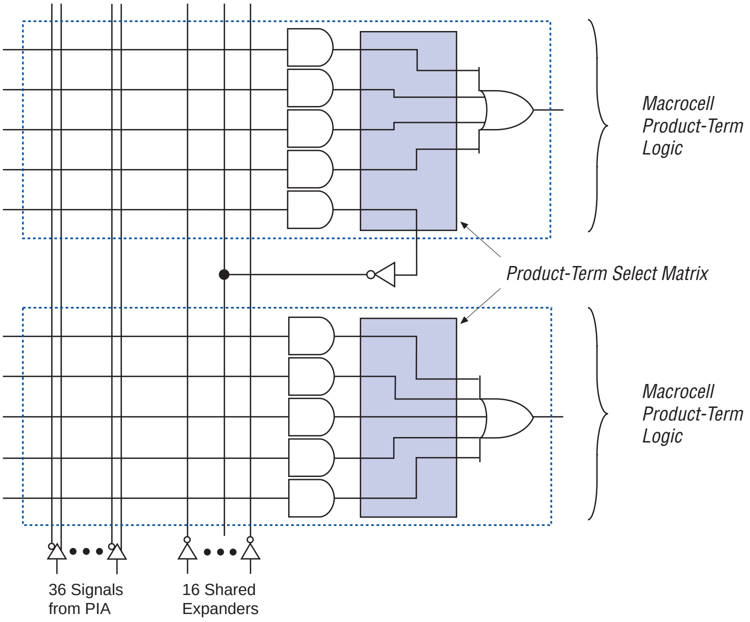
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000A architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 7000A Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



In-System Programmability

MAX 7000A devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 kΩ.

MAX 7000AE devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is only available in EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, and EPM7512AE devices.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster serial/USB communications cable, ByteBlasterMV parallel port download cable, and BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000AE devices can be programmed with either an adaptive or constant (non-adaptive) algorithm. EPM7128A and EPM7256A device can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD 71, can be used to program MAX 7000A devices with in-circuit testers, PCs, or embedded processors.

For more information on using the Jam STAPL language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)*.

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (`TCK`) frequency and the number of `TCK` cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the `TCK` frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000A Device

The time required to program a single MAX 7000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of `TCK` cycles to program a device
f_{TCK} = `TCK` frequency

The ISP times for a stand-alone verification of a single MAX 7000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of `TCK` cycles to verify a device

Table 8. MAX 7000A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the `TDI` and `TDO` pins, allowing the IDCODE to be serially shifted out of `TDO`
USERCODE	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE value to be shifted out of `TDO`. The USERCODE instruction is available for MAX 7000AE devices only
UESCODE	These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be shifted out of `TDO`. UESCODE instructions are available for EPM7128A and EPM7256A devices only.
ISP Instructions	These instructions are used when programming MAX 7000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam STAPL File, JBC File, or SVF File via an embedded processor or test equipment.

Power Sequencing & Hot-Socketing

Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000AE devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.

MAX 7000AE device I/O pins will not source or sink more than 300 µA of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the `OE1` and `GLCRn` pins. The `OE1` and `GLCRn` pins can be driven up to 3.6 V during hot-socketing. After V_{CCINT} and V_{CCIO} reach the recommended operating conditions, these two pins are 5.0-V tolerant.

EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.

Design Security

All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9. Test patterns can be used and then erased during early stages of the production flow.

Table 14. MAX 7000A Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(13)*	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation	*(3)*	3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation	*(3)*	2.3	2.7	V
V_{CCISP}	Supply voltage during in-system programming		3.0	3.6	V
V_I	Input voltage	*(4)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	Commercial range	0	70	° C
		Industrial range *(5)*	–40	85	° C
T_J	Junction temperature	Commercial range	0	90	° C
		Industrial range *(5)*	–40	105	° C
		Extended range *(5)*	–40	130	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 19. EPM7064AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		4.5		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		4.5		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	2.8		4.7		6.2		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.1	1.0	5.1	1.0	7.0	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.6		2.6		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.3		0.4		0.6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.3	1.0	7.2	1.0	9.6	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		4.5		7.4		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	222.2		135.1		100.0		MHz
t_{ACNT}	Minimum array clock period	*(2)*		4.5		7.4		10.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	222.2		135.1		100.0		MHz

Table 23. EPM7256AE External Timing Parameters *Note (1)*									
Symbol	**Parameter**	**Conditions**	**Speed Grade**						**Unit**
			-5		**-7**		**-10**		
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		5.5		7.5		10	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		5.5		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	3.9		5.2		6.9		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.5	1.0	4.8	1.0	6.4	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	2.0		2.7		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	5.4	1.0	7.3	1.0	9.7	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		5.8		7.9		10.5	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	172.4		126.6		95.2		MHz
t_{ACNT}	Minimum array clock period	*(2)*		5.8		7.9		10.5	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	172.4		126.6		95.2		MHz

Table 24. EPM7256AE Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		0.9		1.2	ns
t_{IO}	I/O input pad and buffer delay			0.7		0.9		1.2	ns
t_{FIN}	Fast input delay			2.4		2.9		3.4	ns
t_{SEXP}	Shared expander delay			2.1		2.8		3.7	ns
t_{PEXP}	Parallel expander delay			0.3		0.5		0.6	ns
t_{LAD}	Logic array delay			1.7		2.2		2.8	ns
t_{LAC}	Logic control array delay			0.8		1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		1.4		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.5		2.1		2.9		ns
t_H	Register hold time		0.7		0.9		1.2		ns
t_{FSU}	Register setup time of fast input		1.1		1.6		1.6		ns
t_{FH}	Register hold time of fast input		1.4		1.4		1.4		ns
t_{RD}	Register delay			0.9		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.5		0.8		1.2	ns

Table 25. EPM7512AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		7.5		10.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		7.5		10.0		12.0	ns
t_{SU}	Global clock setup time	*(2)*	5.6		7.6		9.1		ns
t_H	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	4.7	1.0	6.3	1.0	7.5	ns
t_{CH}	Global clock high time		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time	*(2)*	2.5		3.5		4.1		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	7.8	1.0	10.4	1.0	12.5	ns
t_{ACH}	Array clock high time		3.0		4.0		5.0		ns
t_{ACL}	Array clock low time		3.0		4.0		5.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		4.0		5.0		ns
t_{CNT}	Minimum global clock period	*(2)*		8.6		11.5		13.9	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	116.3		87.0		71.9		MHz
t_{ACNT}	Minimum array clock period	*(2)*		8.6		11.5		13.9	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	116.3		87.0		71.9		MHz

Table 30. EPM7256A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{COMB}	Combinatorial delay			1.6		2.0		2.7		3.2	ns
t_{IC}	Array clock delay			2.7		3.4		4.5		5.4	ns
t_{EN}	Register enable time			2.5		3.1		4.2		5.0	ns
t_{GLOB}	Global control delay			1.1		1.4		1.8		2.2	ns
t_{PRE}	Register preset time			2.3		2.9		3.8		4.6	ns
t_{CLR}	Register clear time			2.3		2.9		3.8		4.6	ns
t_{PIA}	PIA delay	*(2)*		1.3		1.6		2.1		2.6	ns
t_{LPA}	Low-power adder	*(6)*		11.0		10.0		10.0		10.0	ns

Notes to tables:

(1) These values are specified under the recommended operating conditions shown in Table 14 on page 28. See Figure 12 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(4) This parameter is measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) Operating conditions: $V_{CCIO} = 2.5 \pm 0.2$ V for commercial and industrial use.

(6) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

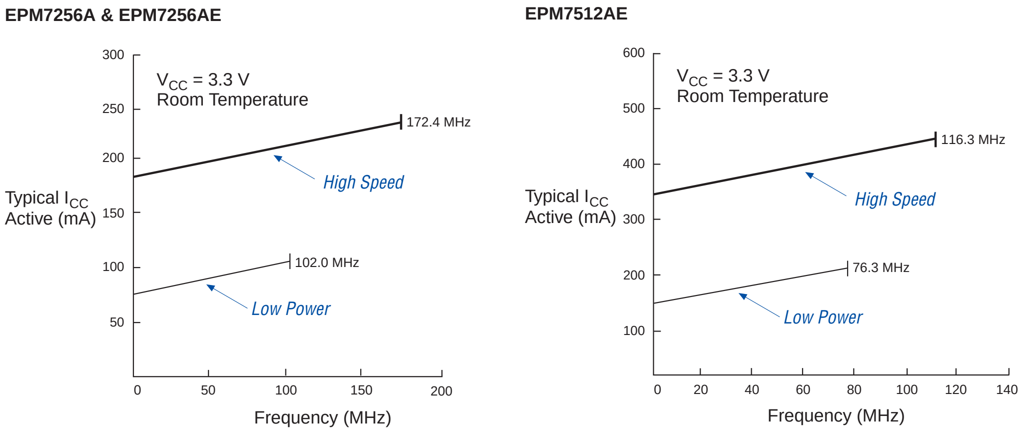
The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

Figure 13. I_{CC} vs. Frequency for MAX 7000A Devices (Part 2 of 2)



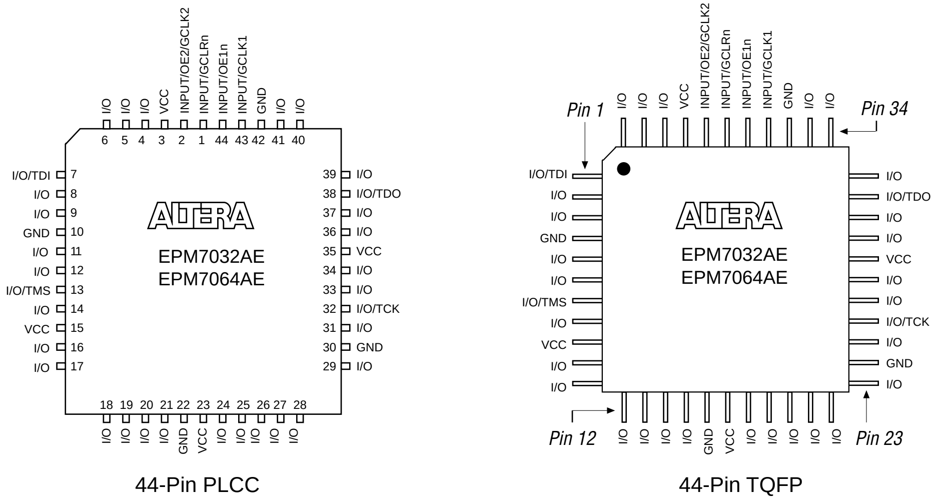
Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information.

Figures 14 through 23 show the package pin-out diagrams for MAX 7000A devices.

Figure 14. 44-Pin PLCC/TQFP Package Pin-Out Diagram

Package outlines not drawn to scale.



44-Pin PLCC

44-Pin TQFP

Figure 15. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outlines not drawn to scale.

Figure 16. 84-Pin PLCC Package Pin-Out Diagram

Package outline not drawn to scale.

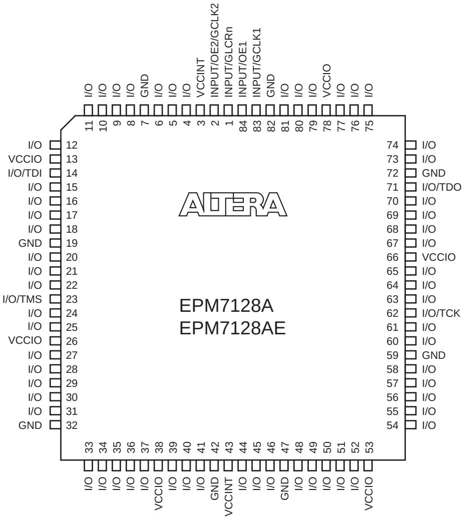


Figure 23. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

Revision History

The information contained in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5 supersedes information published in previous versions.

Version 4.5

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5:

- Updated text in the "Power Sequencing & Hot-Socketing" section.

Version 4.4

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.4:

- Added Tables 5 through 7.
- Added "Programming Sequence" on page 17 and "Programming Times" on page 18.

Version 4.3

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.3:

- Added extended temperature devices to document
- Updated Table 14.

Version 4.2

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.2:

- Removed *Note (1)* from Table 2.
- Removed *Note (4)* from Tables 3 and 4.

Version 4.1

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.1:

- Updated leakage current information in Table 15.
- Updated *Note (9)* of Table 15.
- Updated *Note (1)* of Tables 17 through 30.

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