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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7128aelc84-5">https://www.e-xfl.com/product-detail/intel/epm7128aelc84-5</a>

**Table 1. MAX 7000A Device Features**

Feature	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
$t_{PD}$ (ns)	4.5	4.5	5.0	5.5	7.5
$t_{SU}$ (ns)	2.9	2.8	3.3	3.9	5.6
$t_{FSU}$ (ns)	2.5	2.5	2.5	2.5	3.0
$t_{CO1}$ (ns)	3.0	3.1	3.4	3.5	4.7
$f_{CNT}$ (MHz)	227.3	222.2	192.3	172.4	116.3

## ...and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt™ I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins

- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, ByteBlasterMV™ parallel port download cable, and BitBlaster™ serial download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File- (.svf) capable in-circuit tester

## General Description

MAX 7000A (including MAX 7000AE) devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 7000A devices in the -4, -5, -6, -7, and some -10 speed grades are compatible with the timing requirements for 33 MHz operation of the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See [Table 2](#).

**Table 2. MAX 7000A Speed Grades**

Device	Speed Grade					
	-4	-5	-6	-7	-10	-12
EPM7032AE	✓			✓	✓	
EPM7064AE	✓			✓	✓	
EPM7128A			✓	✓	✓	✓
EPM7128AE		✓		✓	✓	
EPM7256A			✓	✓	✓	✓
EPM7256AE		✓		✓	✓	
EPM7512AE				✓	✓	✓

The MAX 7000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices including PALs, GALs, and 22V10s devices. MAX 7000A devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, Ultra FineLine BGA, PQFP, and TQFP packages. See [Table 3](#) and [Table 4](#).

**Table 3. MAX 7000A Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	49-Pin Ultra FineLine BGA (2)	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine BGA (3)
EPM7032AE	36	36				
EPM7064AE	36	36	41		68	68
EPM7128A				68	84	84
EPM7128AE				68	84	84
EPM7256A					84	
EPM7256AE					84	84
EPM7512AE						

**Table 4. MAX 7000A Maximum User I/O Pins** *Note (1)*

Device	144-Pin TQFP	169-Pin Ultra FineLine BGA (2)	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA (3)
EPM7032AE					
EPM7064AE					
EPM7128A	100				100
EPM7128AE	100	100			100
EPM7256A	120		164		164
EPM7256AE	120		164		164
EPM7512AE	120		176	212	212

**Notes to tables:**

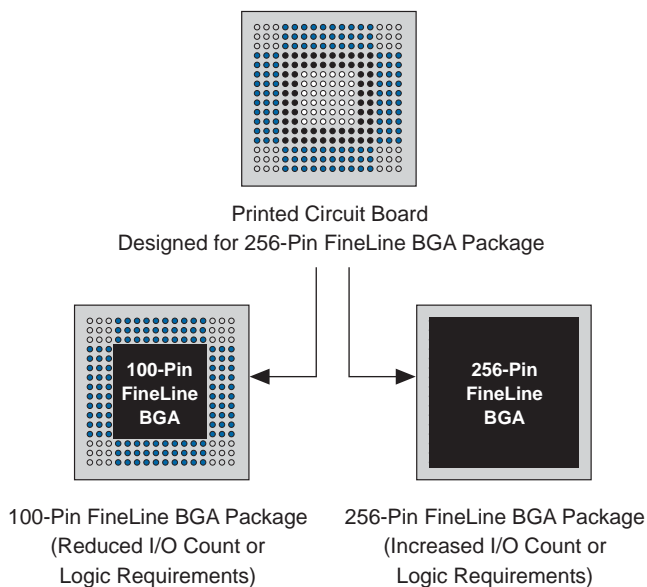
- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.
- (2) All Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 15](#) for more details.
- (3) All FineLine BGA packages are footprint-compatible via the SameFrame feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See [“SameFrame Pin-Outs” on page 15](#) for more details.

## SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 7](#)).

**Figure 7. SameFrame Pin-Out Example**





For more information on using the Jam STAPL language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)*.

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

The programming times described in [Tables 5 through 7](#) are associated with the worst-case method using the enhanced ISP algorithm.

**Table 5. MAX 7000A  $t_{PULSE}$  &  $Cycle_{TCK}$  Values**

Device	Programming		Stand-Alone Verification	
	$t_{PPULSE}$ (s)	$Cycle_{PTCK}$	$t_{VPULSE}$ (s)	$Cycle_{VTCK}$
EPM7032AE	2.00	55,000	0.002	18,000
EPM7064AE	2.00	105,000	0.002	35,000
EPM7128AE	2.00	205,000	0.002	68,000
EPM7256AE	2.00	447,000	0.002	149,000
EPM7512AE	2.00	890,000	0.002	297,000
EPM7128A (1)	5.11	832,000	0.03	528,000
EPM7256A (1)	6.43	1,603,000	0.03	1,024,000

[Tables 6 and 7](#) show the in-system programming and stand alone verification times for several common test clock frequencies.

**Table 6. MAX 7000A In-System Programming Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032AE	2.01	2.01	2.03	2.06	2.11	2.28	2.55	3.10	s
EPM7064AE	2.01	2.02	2.05	2.11	2.21	2.53	3.05	4.10	s
EPM7128AE	2.02	2.04	2.10	2.21	2.41	3.03	4.05	6.10	s
EPM7256AE	2.05	2.09	2.23	2.45	2.90	4.24	6.47	10.94	s
EPM7512AE	2.09	2.18	2.45	2.89	3.78	6.45	10.90	19.80	s
EPM7128A (1)	5.19	5.27	5.52	5.94	6.77	9.27	13.43	21.75	s
EPM7256A (1)	6.59	6.75	7.23	8.03	9.64	14.45	22.46	38.49	s

**Table 8. MAX 7000A JTAG Instructions**

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO. The USERCODE instruction is available for MAX 7000AE devices only
UESCODE	These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be shifted out of TDO. UESCODE instructions are available for EPM7128A and EPM7256A devices only.
ISP Instructions	These instructions are used when programming MAX 7000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam STAPL File, JBC File, or SVF File via an embedded processor or test equipment.



## Power Sequencing & Hot-Socketing

Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

Signals can be driven into MAX 7000AE devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.

MAX 7000AE device I/O pins will not source or sink more than 300  $\mu$ A of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the  $OE1$  and  $GLCRn$  pins. The  $OE1$  and  $GLCRn$  pins can be driven up to 3.6 V during hot-socketing. After  $V_{CCINT}$  and  $V_{CCIO}$  reach the recommended operating conditions, these two pins are 5.0-V tolerant.

EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.

## Design Security

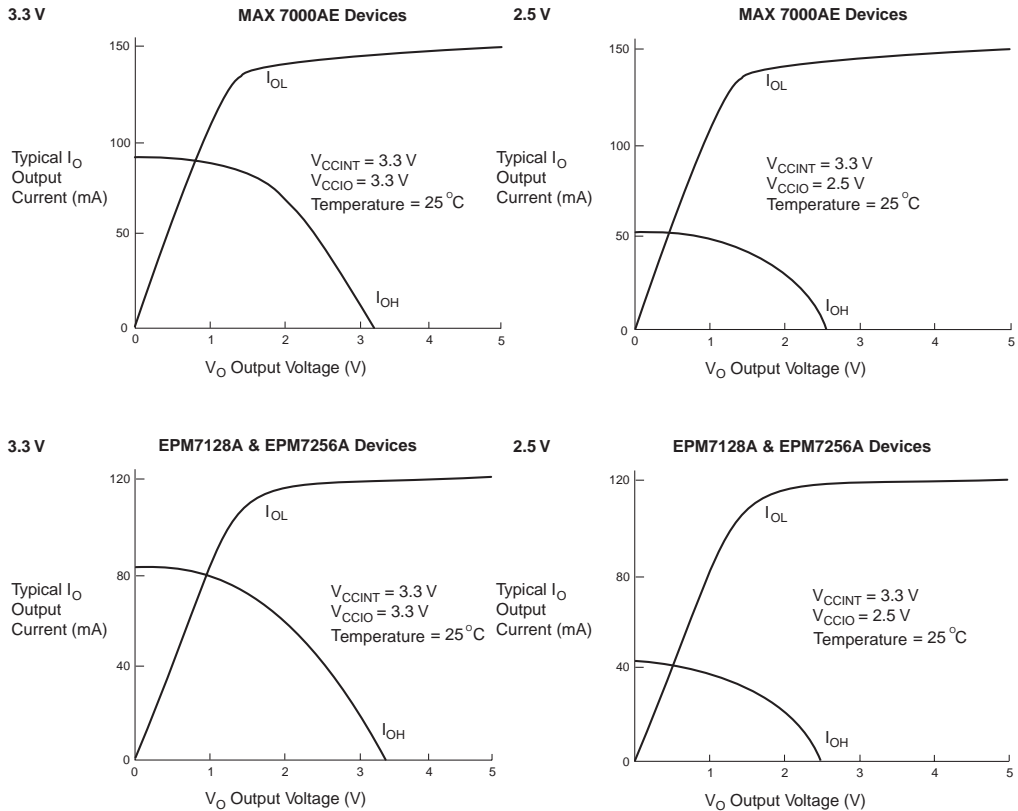
All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 9](#). Test patterns can be used and then erased during early stages of the production flow.

Figure 10 shows the typical output drive characteristics of MAX 7000A devices.

**Figure 10. Output Drive Characteristics of MAX 7000A Devices**



## Timing Model

MAX 7000A device timing can be analyzed with the Altera software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 11. MAX 7000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

**Table 18. EPM7032AE Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		1.2		1.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		1.2		1.5	ns
$t_{FIN}$	Fast input delay			2.3		2.8		3.4	ns
$t_{SEXP}$	Shared expander delay			1.9		3.1		4.0	ns
$t_{PEXP}$	Parallel expander delay			0.5		0.8		1.0	ns
$t_{LAD}$	Logic array delay			1.5		2.5		3.3	ns
$t_{LAC}$	Logic control array delay			0.6		1.0		1.2	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.3		1.8	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.3		1.8		2.3	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.8		6.3		6.8	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		1.3		2.0		2.8		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{FSU}$	Register setup time of fast input		1.0		1.5		1.5		ns
$t_{FH}$	Register hold time of fast input		1.5		1.5		1.5		ns
$t_{RD}$	Register delay			0.7		1.2		1.5	ns
$t_{COMB}$	Combinatorial delay			0.6		1.0		1.3	ns

**Table 18. EPM7032AE Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IC}$	Array clock delay			1.2		2.0		2.5	ns
$t_{EN}$	Register enable time			0.6		1.0		1.2	ns
$t_{GLOB}$	Global control delay			0.8		1.3		1.9	ns
$t_{PRE}$	Register preset time			1.2		1.9		2.6	ns
$t_{CLR}$	Register clear time			1.2		1.9		2.6	ns
$t_{PIA}$	PIA delay	(2)		0.9		1.5		2.1	ns
$t_{LPA}$	Low-power adder	(6)		2.5		4.0		5.0	ns

**Table 20. EPM7064AE Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.6		1.1		1.4	ns
$t_{IO}$	I/O input pad and buffer delay			0.6		1.1		1.4	ns
$t_{FIN}$	Fast input delay			2.5		3.0		3.7	ns
$t_{SEXP}$	Shared expander delay			1.8		3.0		3.9	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.7		0.9	ns
$t_{LAD}$	Logic array delay			1.5		2.5		3.2	ns
$t_{LAC}$	Logic control array delay			0.6		1.0		1.2	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.3		1.8	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.3		1.8		2.3	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.8		6.3		6.8	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		1.3		2.0		2.9		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{FSU}$	Register setup time of fast input		1.0		1.5		1.5		ns
$t_{FH}$	Register hold time of fast input		1.5		1.5		1.5		ns
$t_{RD}$	Register delay			0.7		1.2		1.6	ns
$t_{COMB}$	Combinatorial delay			0.6		0.9		1.3	ns
$t_{IC}$	Array clock delay			1.2		1.9		2.5	ns

**Table 20. EPM7064AE Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{EN}$	Register enable time			0.6		1.0		1.2	ns
$t_{GLOB}$	Global control delay			1.0		1.5		2.2	ns
$t_{PRE}$	Register preset time			1.3		2.1		2.9	ns
$t_{CLR}$	Register clear time			1.3		2.1		2.9	ns
$t_{PIA}$	PIA delay	(2)		1.0		1.7		2.3	ns
$t_{LPA}$	Low-power adder	(6)		3.5		4.0		5.0	ns

**Table 24. EPM7256AE Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		0.9		1.2	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		0.9		1.2	ns
$t_{FIN}$	Fast input delay			2.4		2.9		3.4	ns
$t_{SEXP}$	Shared expander delay			2.1		2.8		3.7	ns
$t_{PEXP}$	Parallel expander delay			0.3		0.5		0.6	ns
$t_{LAD}$	Logic array delay			1.7		2.2		2.8	ns
$t_{LAC}$	Logic control array delay			0.8		1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.6	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.4		1.7		2.1	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		1.5		2.1		2.9		ns
$t_H$	Register hold time		0.7		0.9		1.2		ns
$t_{FSU}$	Register setup time of fast input		1.1		1.6		1.6		ns
$t_{FH}$	Register hold time of fast input		1.4		1.4		1.4		ns
$t_{RD}$	Register delay			0.9		1.2		1.6	ns
$t_{COMB}$	Combinatorial delay			0.5		0.8		1.2	ns

**Table 26. EPM7512AE Internal Timing Parameters (Part 2 of 2)** *Note (1)*

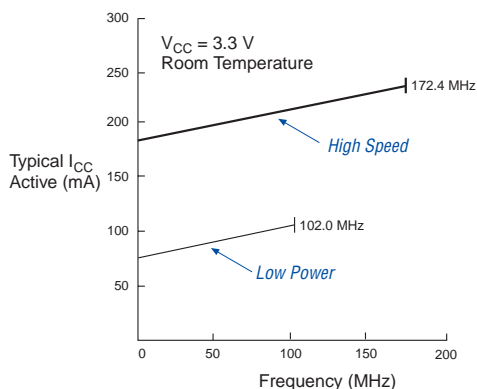
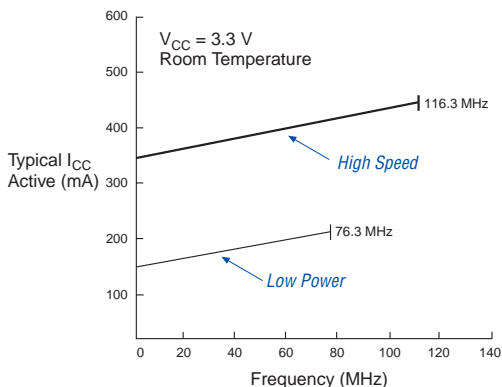
Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
$t_{IC}$	Array clock delay			1.8		2.3		2.9	ns
$t_{EN}$	Register enable time			1.0		1.3		1.7	ns
$t_{GLOB}$	Global control delay			1.7		2.2		2.7	ns
$t_{PRE}$	Register preset time			1.0		1.4		1.7	ns
$t_{CLR}$	Register clear time			1.0		1.4		1.7	ns
$t_{PIA}$	PIA delay	(2)		3.0		4.0		4.8	ns
$t_{LPA}$	Low-power adder	(6)		4.5		5.0		5.0	ns



Table 27. EPM7128A External Timing Parameters

Note (1)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		6.0		7.5		10.0		12.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		6.0		7.5		10.0		12.0	ns
t <sub>SU</sub>	Global clock setup time	(2)	4.2		5.3		7.0		8.5		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.7	1.0	4.6	1.0	6.1	1.0	7.3	ns
t <sub>CH</sub>	Global clock high time		3.0		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.9		2.4		3.1		3.8		ns
t <sub>AH</sub>	Array clock hold time	(2)	1.5		2.2		3.3		4.3		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	6.0	1.0	7.5	1.0	10.0	1.0	12.0	ns
t <sub>ACH</sub>	Array clock high time		3.0		3.0		4.0		5.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		3.0		4.0		5.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	3.0		3.0		4.0		5.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		6.9		8.6		11.5		13.8	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	144.9		116.3		87.0		72.5		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		6.9		8.6		11.5		13.8	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	144.9		116.3		87		72.5		MHz

**Figure 13.  $I_{CC}$  vs. Frequency for MAX 7000A Devices (Part 2 of 2)****EPM7256A & EPM7256AE****EPM7512AE**

## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figures 14 through 23 show the package pin-out diagrams for MAX 7000A devices.

**Figure 14. 44-Pin PLCC/TQFP Package Pin-Out Diagram**

Package outlines not drawn to scale.

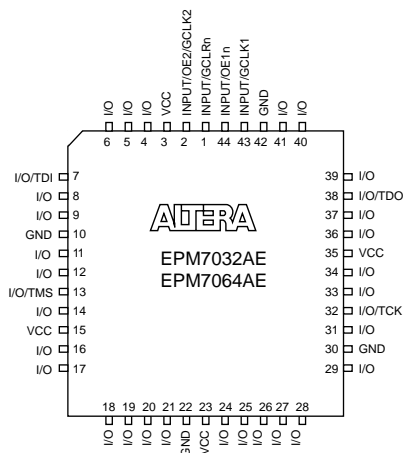
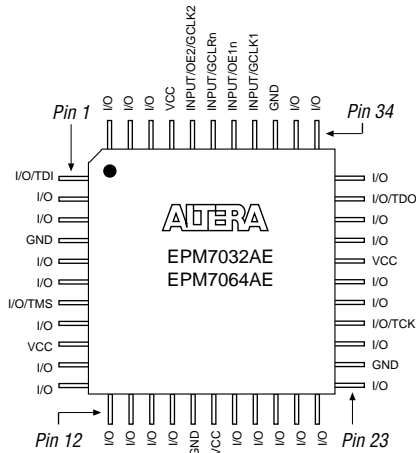
**44-Pin PLCC****44-Pin TQFP**

Figure 19. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

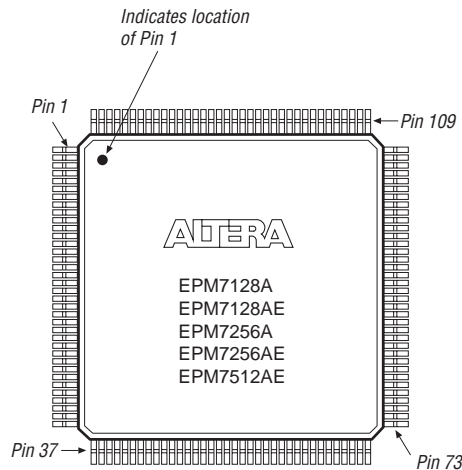
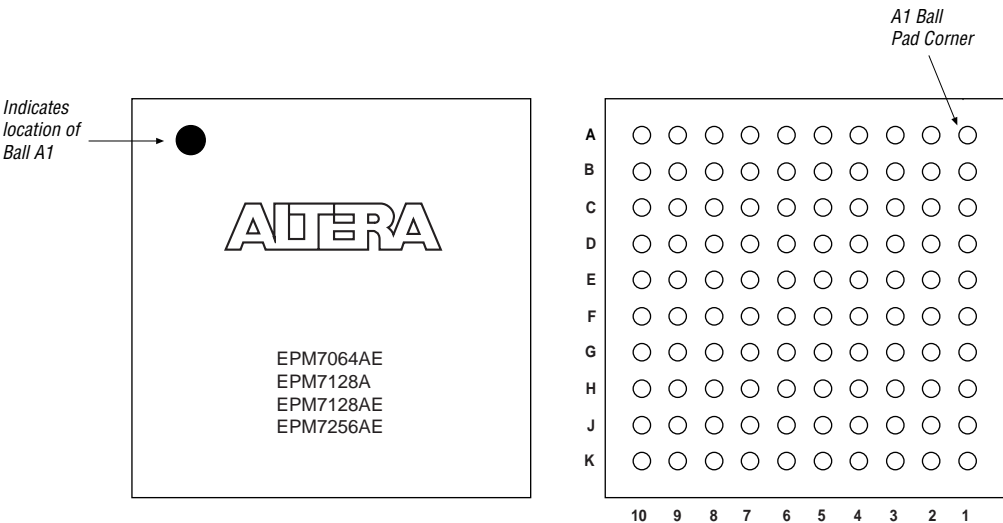


Figure 20. 169-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



**Figure 21. 208-Pin PQFP Package Pin-Out Diagram**

Package outline not drawn to scale.

