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Intel - EPM7128AETC100-10 Datasheet



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Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128aetc100-10

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Table 1. MAX 700	IOA Device Featur	es			
Feature	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
t _{PD} (ns)	4.5	4.5	5.0	5.5	7.5
t _{SU} (ns)	2.9	2.8	3.3	3.9	5.6
t _{FSU} (ns)	2.5	2.5	2.5	2.5	3.0
t _{CO1} (ns)	3.0	3.1	3.4	3.5	4.7
f _{CNT} (MHz)	227.3	222.2	192.3	172.4	116.3

...and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt[™] I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), spacesaving FineLine BGA[™], and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins



Figure 1. MAX 7000A Device Block Diagram

Note:

(1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables. EPM7512AE devices have 10 output enables.

Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- **3**6 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Macrocells

MAX 7000A macrocells can be individually configured for either sequential or combinatorial logic operation. The macrocells consist of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows a MAX 7000A macrocell.



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000A architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.



Shareable expanders can be shared by any or all macrocells in an LAB.



In-System Programmability

MAX 7000A devices can be programmed in-system via an industrystandard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k Ω .

MAX 7000AE devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is only available in EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, and EPM7512AE devices.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster serial/USB communications cable, ByteBlasterMV parallel port download cable, and BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a predefined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000AE devices can be programmed with either an adaptive or constant (non-adaptive) algorithm. EPM7128A and EPM7256A device can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD 71, can be used to program MAX 7000A devices with incircuit testers, PCs, or embedded processors.

Table 7. MAX 7000A Stand-Alone Verification Times for Different Test Clock Frequencies													
Device		f _{TCK}											
	10 MHz	VHz 5 MHz 2 MHz 1 MHz 500 kHz 200 kHz 100 kHz 50 kHz											
EPM7032AE	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	S				
EPM7064AE	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	S				
EPM7128AE	0.01	0.02	0.04	0.07	0.14	0.34	0.68	1.36	S				
EPM7256AE	0.02	0.03	0.08	0.15	0.30	0.75	1.49	2.98	S				
EPM7512AE	0.03	0.06	0.15	0.30	0.60	1.49	2.97	5.94	S				
EPM7128A (1)	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	S				
EPM7256A (1)	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	S				

Note to tables:

(1) EPM7128A and EPM7256A devices can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

Programming with External Hardware

MAX 7000A devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checks to ensure adequate electrical contact between the adapter and the device.



For more information, see the Altera Programming Hardware Data Sheet.

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices.



For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) **Boundary-Scan** Support

MAX 7000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1. Table 8 describes the JTAG instructions supported by MAX 7000A devices. The pin-out tables, available from the Altera web site (http://www.altera.com), show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Open-Drain Output Option

MAX 7000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Open-drain output pins on MAX 7000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high V_{IH} . When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V to meet CMOS V_{OH} requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Programmable Ground Pins

Each unused I/O pin on MAX 7000A devices may be used as an additional ground pin. In EPM7128A and EPM7256A devices, utilizing unused I/O pins as additional ground pins requires using the associated macrocell. In MAX 7000AE devices, this programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Power Sequencing & Hot-Socketing	Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The $\rm V_{CCIO}$ and $\rm V_{CCINT}$ power planes can be powered in any order.
	Signals can be driven into MAX 7000AE devices before and during power- up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.
	MAX 7000AE device I/O pins will not source or sink more than 300 μA of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the OE1 and GLCRn pins. The OE1 and GLCRn pins can be driven up to 3.6 V during hot-socketing. After V _{CCINT} and V _{CCIO} reach the recommended operating conditions, these two pins are 5.0-V tolerant.
	EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.
Design Security	All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.
Generic Testing	MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9. Test patterns can be used and then erased during early stages of the production flow.

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capacitance)

Figure 9. MAX 7000A AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests 703 Ω [521 Ω] *≶* must not be performed under AC conditions. Large-amplitude, fast-ground-Device Output current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between 586 Ω [481 Ω] *≥* the device ground pin and the test system ground, significant reductions in Device input observable noise immunity can result. rise and fall Numbers in brackets are for 2.5-V times < 2 ns outputs. Numbers without brackets are for 3.3-V outputs.

Operating Conditions

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000A devices.

Table 1	3. MAX 7000A Device Absolute	e Maximum Ratings Note (1)			
Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage	With respect to ground (2)	-0.5	4.6	V
VI	DC input voltage		-2.0	5.75	V
I _{OUT}	DC output current, per pin		-25	25	mA
T _{STG}	Storage temperature	No bias	-65	150	°C
T _A	Ambient temperature	Under bias	-65	135	°C
TJ	Junction temperature	BGA, FineLine BGA, PQFP, and TQFP packages, under bias		135	°C

Table 1	4. MAX 7000A Device Recomm	7000A Device Recommended Operating Conditions Parameter Conditions Min Max Unit voltage for internal logic ut buffers (3), (13) 3.0 3.6 V voltage for output 3.3-V operation (3) 3.0 3.6 V voltage for output 2.5-V operation (3) 2.3 2.7 V voltage during in- programming (3) 3.0 3.6 V voltage (4) -0.5 5.75 V voltage 0 V _{CCIO} V t temperature Commercial range 0 70 °C Industrial range (5) -40 85 °C			
Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (13)	3.0	3.6	V
V _{CCIO}	Supply voltage for output drivers, 3.3-V operation	(3)	3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation	(3)	2.3	2.7	V
V _{CCISP}	Supply voltage during in- system programming		3.0	3.6	V
VI	Input voltage	(4)	-0.5	5.75	V
Vo	Output voltage		0	V _{CCIO}	V
T _A	Ambient temperature	Commercial range	0	70	°C
		Industrial range (5)	-40	85	°C
Τ _J	Junction temperature	Commercial range	0	90	°C
		Industrial range (5)	-40	105	°C
		Extended range (5)	-40	130	°C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

Tables 17 through 30 show EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, EPM7512AE, EPM7128A, and EPM7256A timing information.

Table 1	7. EPM7032AE External Timi	ng Parameters	Note (1)					
Symbol	Parameter	Conditions			Speed	Grade			Unit
			-	4	-	7	-1	0	
			Min	Мах	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t _{SU}	Global clock setup time	(2)	2.9		4.7		6.3		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.6		2.5		3.6		ns
t _{AH}	Array clock hold time	(2)	0.3		0.5		0.5		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.4	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		4.4		7.2		9.7	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	227.3		138.9		103.1		MHz
t _{ACNT}	Minimum array clock period	(2)		4.4		7.2		9.7	ns
facnt	Maximum internal array clock frequency	(2), (4)	227.3		138.9		103.1		MHz

Symbol	Parameter	Conditions			Speed	Grade			Unit
			-	5	-	7		10	
			Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.7		1.0		1.4	ns
t _{IO}	I/O input pad and buffer delay			0.7		1.0		1.4	ns
t _{FIN}	Fast input delay			2.5		3.0		3.4	ns
t _{SEXP}	Shared expander delay			2.0		2.9		3.8	ns
t _{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t _{LAD}	Logic array delay			1.6		2.4		3.1	ns
t _{LAC}	Logic control array delay			0.7		1.0		1.3	ns
t _{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t _{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		0.8		1.2		1.6	ns
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		1.3		1.7		2.1	ns
t _{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		5.8		6.2		6.6	ns
t _{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		4.0		5.0	ns
t _{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		4.5		5.5	ns
t _{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3 V$	C1 = 35 pF		9.0		9.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t _{SU}	Register setup time		1.4		2.1		2.9		ns
t _H	Register hold time		0.6		1.0		1.3		ns
t _{FSU}	Register setup time of fast input		1.1		1.6		1.6		ns
t _{FH}	Register hold time of fast input		1.4		1.4		1.4		ns
t _{RD}	Register delay			0.8		1.2		1.6	ns
t _{COMB}	Combinatorial delay			0.5		0.9		1.3	ns
t _{IC}	Array clock delay			1.2		1.7		2.2	ns

Altera Corporation

Table 2	3. EPM7256AE External	Timing Parai	neters	Note (1,)				
Symbol	Parameter	Conditions			Speed	Grade			Unit
			-;	5	-	7	-1	0	_
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non- registered output	C1 = 35 pF (2)		5.5		7.5		10	ns
t _{PD2}	I/O input to non- registered output	C1 = 35 pF (2)		5.5		7.5		10	ns
t _{SU}	Global clock setup time	(2)	3.9		5.2		6.9		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.5	1.0	4.8	1.0	6.4	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	2.0		2.7		3.6		ns
t _{AH}	Array clock hold time	(2)	0.2		0.3		0.5		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	5.4	1.0	7.3	1.0	9.7	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		5.8		7.9		10.5	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	172.4		126.6		95.2		MHz
t _{acnt}	Minimum array clock period	(2)		5.8		7.9		10.5	ns
f _{acnt}	Maximum internal array clock frequency	(2), (4)	172.4		126.6		95.2		MHz

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Table 2	Table 28. EPM7128A Internal Timing Parameters (Part 1 of 2) Note (1)												
Symbol	Parameter	Conditions				Speed	Grade				Unit		
			-	6	-	7	-1	10	-1	12	1		
			Min	Мах	Min	Max	Min	Мах	Min	Max			
t _{IN}	Input pad and buffer delay			0.6		0.7		0.9		1.1	ns		
t _{IO}	I/O input pad and buffer delay			0.6		0.7		0.9		1.1	ns		
t _{FIN}	Fast input delay			2.7		3.1		3.6		3.9	ns		
t _{SEXP}	Shared expander delay			2.5		3.2		4.3		5.1	ns		
t _{PEXP}	Parallel expander delay			0.7		0.8		1.1		1.3	ns		
t _{LAD}	Logic array delay			2.4		3.0		4.1		4.9	ns		
t _{LAC}	Logic control array delay			2.4		3.0		4.1		4.9	ns		
t _{IOE}	Internal output enable delay			0.0		0.0		0.0		0.0	ns		
t _{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.4		0.6		0.7		0.9	ns		
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		0.9		1.1		1.2		1.4	ns		
t _{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5$ V or 3.3 V	C1 = 35 pF		5.4		5.6		5.7		5.9	ns		
t _{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 \text{ V}$	C1 = 35 pF		4.0		4.0		5.0		5.0	ns		
t _{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		4.5		5.5		5.5	ns		
t _{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3 V$	C1 = 35 pF		9.0		9.0		10.0		10.0	ns		
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		5.0	ns		
t _{SU}	Register setup time		1.9		2.4		3.1		3.8		ns		
t _H	Register hold time		1.5		2.2		3.3		4.3		ns		
t _{FSU}	Register setup time of fast input		0.8		1.1		1.1		1.1		ns		
t _{FH}	Register hold time of fast input		1.7		1.9		1.9		1.9		ns		

Table 2	9. EPM7256A External Til	ning Parame	eters	Note	(1)						
Symbol	Parameter	Conditions				Speed	Grade				Unit
			-	6	-	7	-1	10	-1	12	
			Min	Max	Min	Max	Min	Мах	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		6.0		7.5		10.0		12.0	ns
t _{PD2}	I/O input to non- registered output	C1 = 35 pF (2)		6.0		7.5		10.0		12.0	ns
t _{SU}	Global clock setup time	(2)	3.7		4.6		6.2		7.4		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	4.2	1.0	5.5	1.0	6.6	ns
t _{CH}	Global clock high time		3.0		3.0		4.0		4.0		ns
t _{CL}	Global clock low time		3.0		3.0		4.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	0.8		1.0		1.4		1.6		ns
t _{AH}	Array clock hold time	(2)	1.9		2.7		4.0		5.1		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	6.2	1.0	7.8	1.0	10.3	1.0	12.4	ns
t _{ACH}	Array clock high time		3.0		3.0		4.0		4.0		ns
t _{ACL}	Array clock low time		3.0		3.0		4.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		3.0		4.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		6.4		8.0		10.7		12.8	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	156.3		125.0		93.5		78.1		MHz
t _{acnt}	Minimum array clock period	(2)		6.4		8.0		10.7		12.8	ns
f _{acnt}	Maximum internal array clock frequency	(2), (4)	156.3		125.0		93.5		78.1		MHz

Symbol	Parameter	Conditions		Speed Grade							
			-	6	-	7	-	10	-	12	1
			Min	Мах	Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.3		0.4		0.5		0.6	ns
t _{IO}	I/O input pad and buffer delay			0.3		0.4		0.5		0.6	ns
t _{FIN}	Fast input delay			2.4		3.0		3.4		3.8	ns
t _{SEXP}	Shared expander delay			2.8		3.5		4.7		5.6	ns
t _{PEXP}	Parallel expander delay			0.5		0.6		0.8		1.0	ns
t _{LAD}	Logic array delay			2.5		3.1		4.2		5.0	ns
t _{LAC}	Logic control array delay			2.5		3.1		4.2		5.0	ns
t _{IOE}	Internal output enable delay			0.2		0.3		0.4		0.5	ns
t _{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		0.3		0.4		0.5		0.6	ns
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		0.8		0.9		1.0		1.1	ns
t _{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.3		5.4		5.5		5.6	ns
t _{ZX1}	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		4.0		5.0		5.0	ns
t _{ZX2}	Output buffer enable delay slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		4.5		5.5		5.5	ns
t _{ZX3}	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5$ V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		5.0	ns
t _{SU}	Register setup time		1.0		1.3		1.7		2.0		ns
t _H	Register hold time		1.7		2.4		3.7		4.7		ns
t _{FSU}	Register setup time of fast input		1.2		1.4		1.4		1.4		ns
t _{FH}	Register hold time of fast input		1.3		1.6		1.6		1.6		ns
t _{RD}	Register delay			1.6		2.0		2.7		3.2	ns

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The parameters in this equation are:

MC _{TON}	=	Number of macrocells with the Turbo Bit option turned	
		on, as reported in the MAX+PLUS II Report File (.rpt)	
MC _{DEV}	=	Number of macrocells in the device	
MC _{USED}	=	Total number of macrocells in the design, as reported in	
		the Report File	
f _{MAX}	=	Highest clock frequency to the device	
togLC	=	Average percentage of logic cells toggling at each clock	
-20		(typically 12.5%)	
A, B, C	=	Constants, shown in Table 31	

Table 31. MAX 7000A I _{CC} Equation Constants					
Device	A	В	C		
EPM7032AE	0.71	0.30	0.014		
EPM7064AE	0.71	0.30	0.014		
EPM7128A	0.71	0.30	0.014		
EPM7128AE	0.71	0.30	0.014		
EPM7256A	0.71	0.30	0.014		
EPM7256AE	0.71	0.30	0.014		
EPM7512AE	0.71	0.30	0.014		

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 17. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.



Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram



Figure 22. 256-Pin BGA Package Pin-Out Diagram

Package outline not drawn to scale.



Figure 23. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5 supersedes information published in previous versions.

Version 4.5

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5:

■ Updated text in the "Power Sequencing & Hot-Socketing" section.

Version 4.4

The following changes were made in the *MAX* 7000A Programmable Logic Device Data Sheet version 4.4:

- Added Tables 5 through 7.
 - Added "Programming Sequence" on page 17 and "Programming Times" on page 18.