Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	100
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128aetc144-5

Table 1. MAX 7000A Device Features

Feature	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
t_{PD} (ns)	4.5	4.5	5.0	5.5	7.5
t_{SU} (ns)	2.9	2.8	3.3	3.9	5.6
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3.0
t_{CO1} (ns)	3.0	3.1	3.4	3.5	4.7
f_{CNT} (MHz)	227.3	222.2	192.3	172.4	116.3

...and More Features

■ 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz

■ MultiVolt™ I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels

■ Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, and plastic J-lead chip carrier (PLCC) packages

■ Supports hot-socketing in MAX 7000AE devices

■ Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance

■ PCI-compatible

■ Bus-friendly architecture, including programmable slew-rate control

■ Open-drain output option

■ Programmable macrocell registers with individual clear, preset, clock, and clock enable controls

■ Programmable power-up states for macrocell registers in MAX 7000AE devices

■ Programmable power-saving mode for 50% or greater power reduction in each macrocell

■ Configurable expander product-term distribution, allowing up to 32 product terms per macrocell

■ Programmable security bit for protection of proprietary designs

■ 6 to 10 pin- or logic-driven output enable signals

■ Two global clock signals with optional inversion

■ Enhanced interconnect resources for improved routability

■ Fast input setup times provided by a dedicated path from I/O pin to macrocell registers

■ Programmable output slew-rate control

■ Programmable ground pins

Altera Corporation

The MAX 7000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices including PALs, GALs, and 22V10s devices. MAX 7000A devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, Ultra FineLine BGA, PQFP, and TQFP packages. See Table 3 and Table 4.

Table 3. MAX 7000A Maximum User I/O Pins *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	49-Pin Ultra FineLine BGA *(2)*	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine BGA *(3)*
EPM7032AE	36	36				
EPM7064AE	36	36	41		68	68
EPM7128A				68	84	84
EPM7128AE				68	84	84
EPM7256A					84	
EPM7256AE					84	84
EPM7512AE						

Table 4. MAX 7000A Maximum User I/O Pins *Note (1)*

Device	144-Pin TQFP	169-Pin Ultra FineLine BGA *(2)*	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA *(3)*
EPM7032AE					
EPM7064AE					
EPM7128A	100				100
EPM7128AE	100	100			100
EPM7256A	120		164		164
EPM7256AE	120		164		164
EPM7512AE	120		176	212	212

*Notes to tables:*

(1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

(2) All Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.

(3) All FineLine BGA packages are footprint-compatible via the SameFrame feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.

Macrocells

MAX 7000A macrocells can be individually configured for either sequential or combinatorial logic operation. The macrocells consist of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows a MAX 7000A macrocell.

Figure 2. MAX 7000A Macrocell
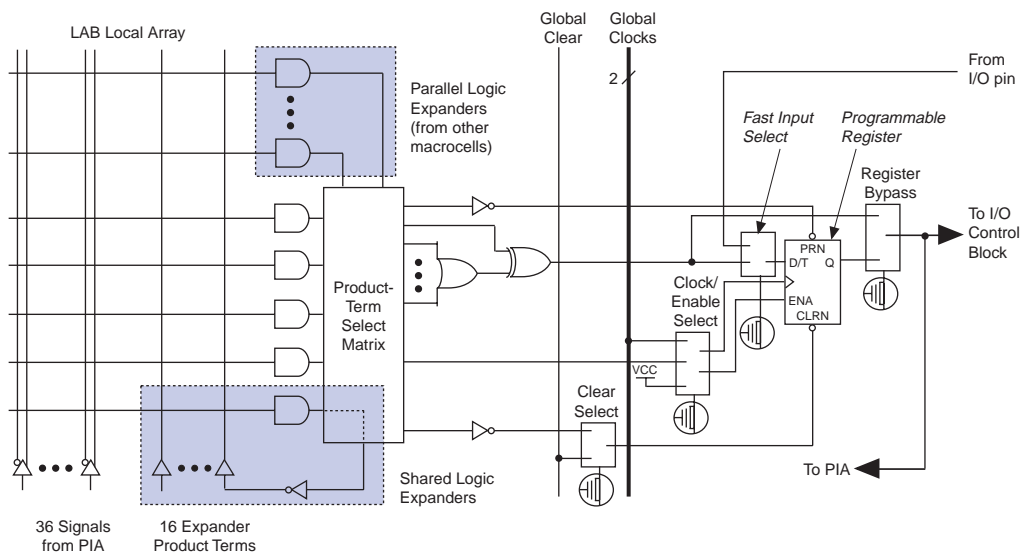
Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

■ Shareable expanders, which are inverted product terms that are fed back into the logic array

■ Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.
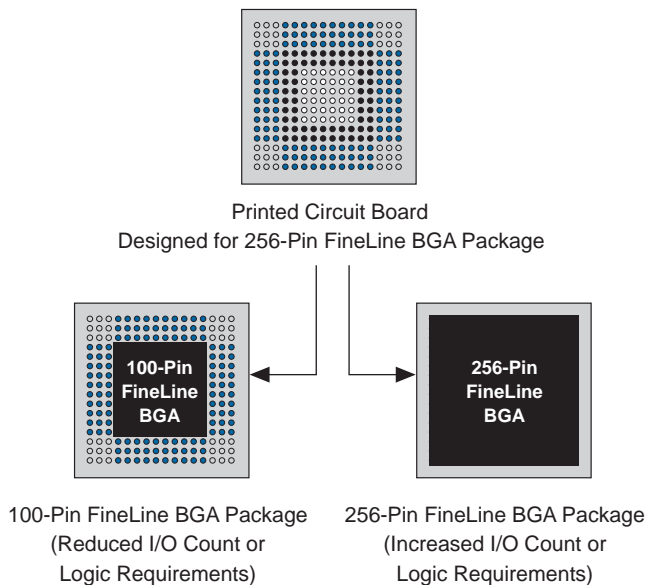
Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders, and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 7).

Figure 7. SameFrame Pin-Out Example

Printed Circuit Board
Designed for 256-Pin FineLine BGA Package

100-Pin FineLine BGA Package
(Reduced I/O Count or
Logic Requirements)

256-Pin FineLine BGA Package
(Increased I/O Count or
Logic Requirements)

Table 8. MAX 7000A JTAG Instructions	
JTAG Instruction	**Description**
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO. The USERCODE instruction is available for MAX 7000AE devices only
UESCODE	These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be shifted out of TDO. UESCODE instructions are available for EPM7128A and EPM7256A devices only.
ISP Instructions	These instructions are used when programming MAX 7000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam STAPL File, JBC File, or SVF File via an embedded processor or test equipment.

The instruction register length of MAX 7000A devices is 10 bits. The user electronic signature (UES) register length in MAX 7000A devices is 16 bits. The MAX 7000AE USERCODE register length is 32 bits. Tables 9 and 10 show the boundary-scan register length and device IDCODE information for MAX 7000A devices.

Table 9. MAX 7000A Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032AE	96
EPM7064AE	192
EPM7128A	288
EPM7128AE	288
EPM7256A	480
EPM7256AE	480
EPM7512AE	624

Table 10. 32-Bit MAX 7000A Device IDCODE   Note (1)

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM7032AE	0001	0111 0000 0011 0010	00001101110	1
EPM7064AE	0001	0111 0000 0110 0100	00001101110	1
EPM7128A	0000	0111 0001 0010 1000	00001101110	1
EPM7128AE	0001	0111 0001 0010 1000	00001101110	1
EPM7256A	0000	0111 0010 0101 0110	00001101110	1
EPM7256AE	0001	0111 0010 0101 0110	00001101110	1
EPM7512AE	0001	0111 0101 0001 0010	00001101110	1

Notes:

(1)   The most significant bit (MSB) is on the left.

(2)   The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST.

Programmable Speed/Power Control

MAX 7000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000A device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power operation (i.e., with the Turbo Bit option turned off). As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters.

Output Configuration

MAX 7000A device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000A devices to connect to systems with differing supply voltages. MAX 7000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 3.0 V incur a slightly greater timing delay of t_{OD2} instead of t_{OD1}. Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 12 describes the MAX 7000A MultiVolt I/O support.

Table 12. MAX 7000A MultiVolt I/O Support

V_{CCIO} Voltage	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓		✓	✓

Table 15. MAX 7000A Device DC Operating Conditions   *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		1.7	5.75	V
V_{IL}	Low-level input voltage		−0.5	0.8	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = −8 mA DC, V_{CCIO} = 3.00 V *(7)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = −0.1 mA DC, V_{CCIO} = 3.00 V *(7)*	V_{CCIO} − 0.2		V
	2.5-V high-level output voltage	I_{OH} = −100 µA DC, V_{CCIO} = 2.30 V *(7)*	2.1		V
		I_{OH} = −1 mA DC, V_{CCIO} = 2.30 V *(7)*	2.0		V
		I_{OH} = −2 mA DC, V_{CCIO} = 2.30 V *(7)*	1.7		V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 3.00 V *(8)*		0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(8)*		0.2	V
	2.5-V low-level output voltage	I_{OL} = 100 µA DC, V_{CCIO} = 2.30 V *(8)*		0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(8)*		0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(8)*		0.7	V
I_I	Input leakage current	V_I = −0.5 to 5.5 V *(9)*	−10	10	µA
I_{OZ}	Tri-state output off-state current	V_I = −0.5 to 5.5 V *(9)*	−10	10	µA
R_{ISP}	Value of I/O pin pull-up resistor during in-system programming or during power-up	V_{CCIO} = 3.0 to 3.6 V *(10)*	20	50	kΩ
		V_{CCIO} = 2.3 to 2.7 V *(10)*	30	80	kΩ
		V_{CCIO} = 2.3 to 3.6 V *(11)*	20	74	kΩ

Table 16. MAX 7000A Device Capacitance   *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Table 23. EPM7256AE External Timing Parameters   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		**-7**		**-10**		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		5.5		7.5		10	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		5.5		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	3.9		5.2		6.9		ns
t_H	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.5	1.0	4.8	1.0	6.4	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	2.0		2.7		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	5.4	1.0	7.3	1.0	9.7	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		5.8		7.9		10.5	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	172.4		126.6		95.2		MHz
t_{ACNT}	Minimum array clock period	*(2)*		5.8		7.9		10.5	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	172.4		126.6		95.2		MHz

Table 24. EPM7256AE Internal Timing Parameters (Part 2 of 2)   Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			\-5		\-7		\-10		
			Min	Max	Min	Max	Min	Max	
t_{IC}	Array clock delay			1.2		1.6		2.1	ns
t_{EN}	Register enable time			0.8		1.0		1.3	ns
t_{GLOB}	Global control delay			1.0		1.5		2.0	ns
t_{PRE}	Register preset time			1.6		2.3		3.0	ns
t_{CLR}	Register clear time			1.6		2.3		3.0	ns
t_{PIA}	PIA delay	(2)		1.7		2.4		3.2	ns
t_{LPA}	Low-power adder	(6)		4.0		4.0		5.0	ns

Table 26. EPM7512AE Internal Timing Parameters (Part 1 of 2)   Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		**-10**		**-12**		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		0.9		1.0	ns
t_{IO}	I/O input pad and buffer delay			0.7		0.9		1.0	ns
t_{FIN}	Fast input delay			3.1		3.6		4.1	ns
t_{SEXP}	Shared expander delay			2.7		3.5		4.4	ns
t_{PEXP}	Parallel expander delay			0.4		0.5		0.6	ns
t_{LAD}	Logic array delay			2.2		2.8		3.5	ns
t_{LAC}	Logic control array delay			1.0		1.3		1.7	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.0		1.5		1.7	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		1.5		2.0		2.2	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.0		6.5		6.7	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0		5.0	ns
t_{SU}	Register setup time		2.1		3.0		3.5		ns
t_{H}	Register hold time		0.6		0.8		1.0		ns
t_{FSU}	Register setup time of fast input		1.6		1.6		1.6		ns
t_{FH}	Register hold time of fast input		1.4		1.4		1.4		ns
t_{RD}	Register delay			1.3		1.7		2.1	ns
t_{COMB}	Combinatorial delay			0.6		0.8		1.0	ns

Table 27. EPM7128A External Timing Parameters   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		**-7**		**-10**		**-12**		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		6.0		7.5		10.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		6.0		7.5		10.0		12.0	ns
t_{SU}	Global clock setup time	*(2)*	4.2		5.3		7.0		8.5		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.7	1.0	4.6	1.0	6.1	1.0	7.3	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.9		2.4		3.1		3.8		ns
t_{AH}	Array clock hold time	*(2)*	1.5		2.2		3.3		4.3		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	6.0	1.0	7.5	1.0	10.0	1.0	12.0	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		5.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		5.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		3.0		4.0		5.0		ns
t_{CNT}	Minimum global clock period	*(2)*		6.9		8.6		11.5		13.8	ns
f_{CNT}	Maximum internal global clock frequency	*(2), (4)*	144.9		116.3		87.0		72.5		MHz
t_{ACNT}	Minimum array clock period	*(2)*		6.9		8.6		11.5		13.8	ns
f_{ACNT}	Maximum internal array clock frequency	*(2), (4)*	144.9		116.3		87		72.5		MHz

Table 30. EPM7256A Internal Timing Parameters (Part 2 of 2)   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{COMB}	Combinatorial delay			1.6		2.0		2.7		3.2	ns
t_{IC}	Array clock delay			2.7		3.4		4.5		5.4	ns
t_{EN}	Register enable time			2.5		3.1		4.2		5.0	ns
t_{GLOB}	Global control delay			1.1		1.4		1.8		2.2	ns
t_{PRE}	Register preset time			2.3		2.9		3.8		4.6	ns
t_{CLR}	Register clear time			2.3		2.9		3.8		4.6	ns
t_{PIA}	PIA delay	*(2)*		1.3		1.6		2.1		2.6	ns
t_{LPA}	Low-power adder	*(6)*		11.0		10.0		10.0		10.0	ns

Notes to tables:

(1) These values are specified under the recommended operating conditions shown in Table 14 on page 28. See Figure 12 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(4) This parameter is measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) Operating conditions: $V_{CCIO} = 2.5 \pm 0.2$ V for commercial and industrial use.

(6) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, t_{ACL}, and t_{CPPW} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency (f_{MAX}, in MHz) for MAX 7000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times tog_{LC})$$

Altera Corporation

The parameters in this equation are:

MC_{TON}	=	Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV}	=	Number of macrocells in the device
MC_{USED}	=	Total number of macrocells in the design, as reported in the Report File
f_{MAX}	=	Highest clock frequency to the device
tog_{LC}	=	Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C	=	Constants, shown in Table 31

Table 31. MAX 7000A I_{CC} Equation Constants

Device	A	B	C
EPM7032AE	0.71	0.30	0.014
EPM7064AE	0.71	0.30	0.014
EPM7128A	0.71	0.30	0.014
EPM7128AE	0.71	0.30	0.014
EPM7256A	0.71	0.30	0.014
EPM7256AE	0.71	0.30	0.014
EPM7512AE	0.71	0.30	0.014

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.
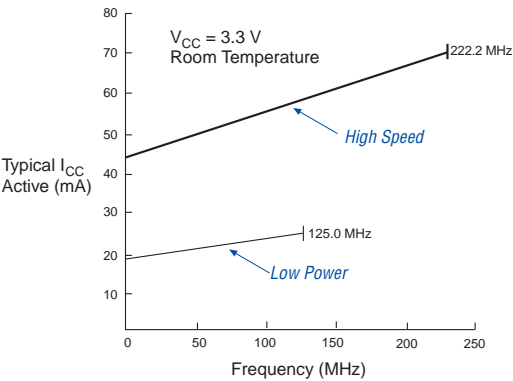
Figure 13 shows the typical supply current versus frequency for MAX 7000A devices.

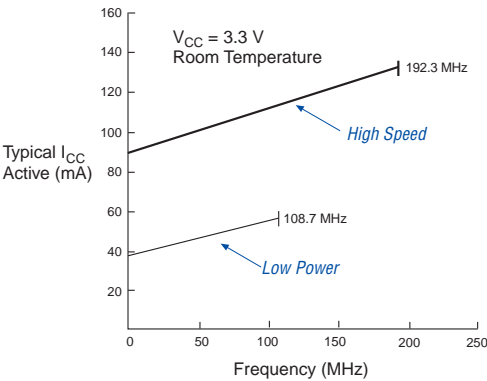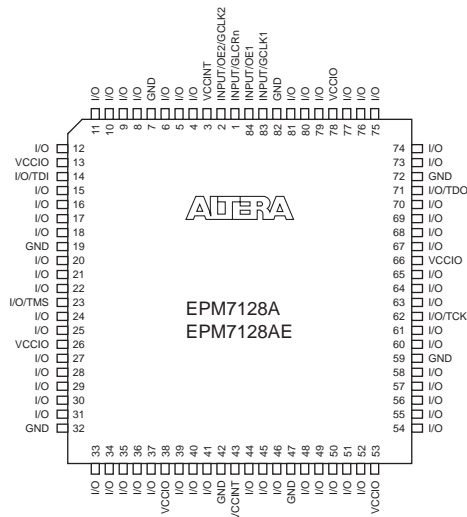*Figure 13. I$_{CC}$ vs. Frequency for MAX 7000A Devices (Part 1 of 2)*
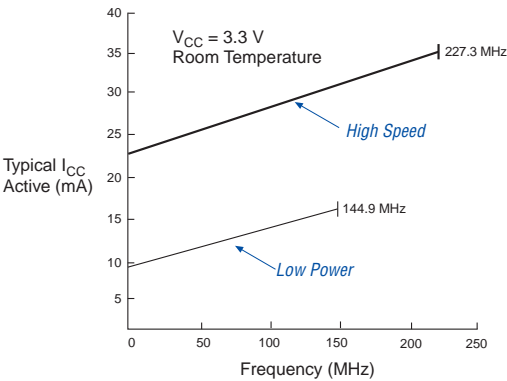
Figure 15. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outlines not drawn to scale.

Figure 16. 84-Pin PLCC Package Pin-Out Diagram
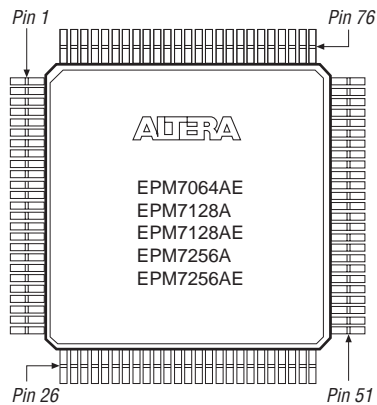
Package outline not drawn to scale.

Figure 17. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

EPM7064AE
EPM7128A
EPM7128AE
EPM7256A
EPM7256AE

Pin 1   Pin 76

Pin 26   Pin 51

Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

Indicates
location of
Ball A1

A1 Ball
Pad Corner

EPM7064AE
EPM7128A
EPM7128AE
EPM7256AE

A B C D E F G H J K

10 9 8 7 6 5 4 3 2 1

Figure 19. 144-Pin TQFP Package Pin-Out Diagram

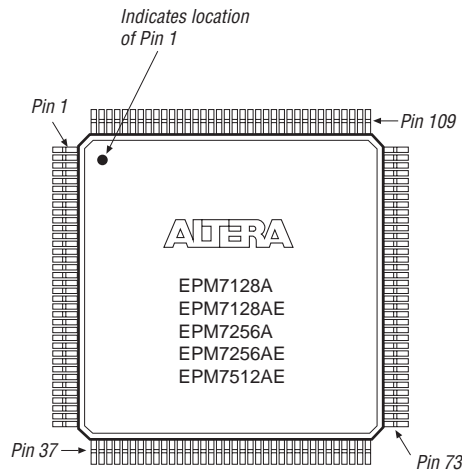*Package outline not drawn to scale.*

Figure 20. 169-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

Figure 22. 256-Pin BGA Package Pin-Out Diagram

Package outline not drawn to scale.