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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

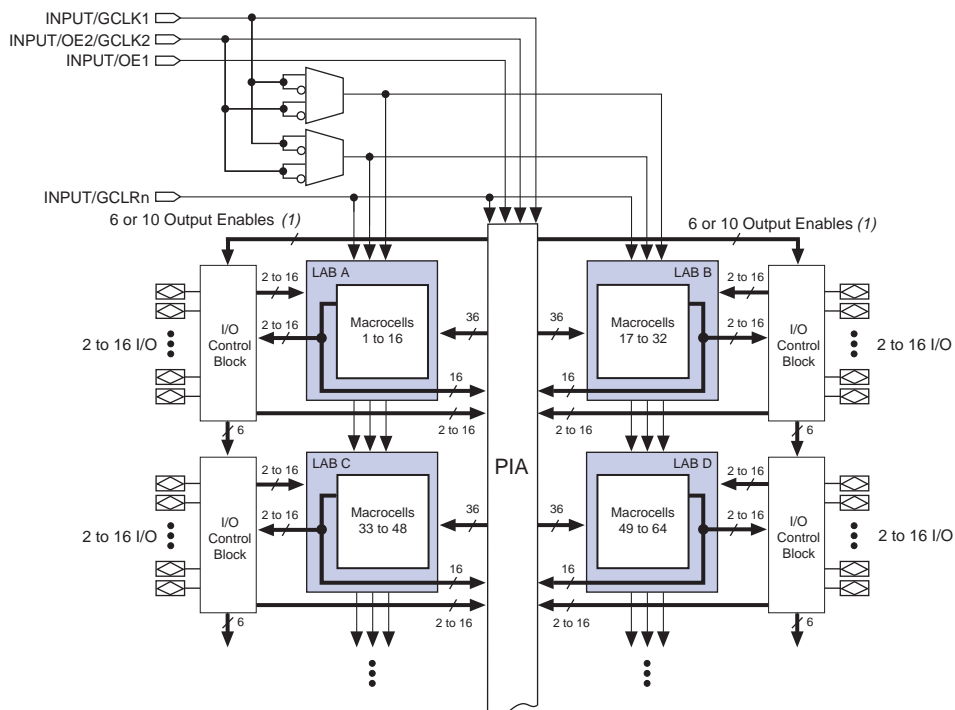
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	100
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7128aetc144-7">https://www.e-xfl.com/product-detail/intel/epm7128aetc144-7</a>

## Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. [Figure 1](#) shows the architecture of MAX 7000A devices.

**Figure 1. MAX 7000A Device Block Diagram****Note:**

- (1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables. EPM7512AE devices have 10 output enables.

## Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in [Figure 1](#). Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000A devices. As shown in [Figure 1](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figure 2](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in a MAX 7000AE device may be set to either a high or low state. This power-up state is specified at design entry. Upon power-up, each register in EPM7128A and EPM7256A devices are set to a low state.

All MAX 7000A I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (as low as 2.5 ns) input setup time.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 7000A Device*

The time required to program a single MAX 7000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:  $t_{PROG}$  = Programming time  
 $t_{PPULSE}$  = Sum of the fixed times to erase, program, and verify the EEPROM cells  
 $Cycle_{PTCK}$  = Number of TCK cycles to program a device  
 $f_{TCK}$  = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:  $t_{VER}$  = Verify time  
 $t_{VPULSE}$  = Sum of the fixed times to verify the EEPROM cells  
 $Cycle_{VTCK}$  = Number of TCK cycles to verify a device

Figure 8 shows timing information for the JTAG signals.

**Figure 8. MAX 7000A JTAG Waveforms**

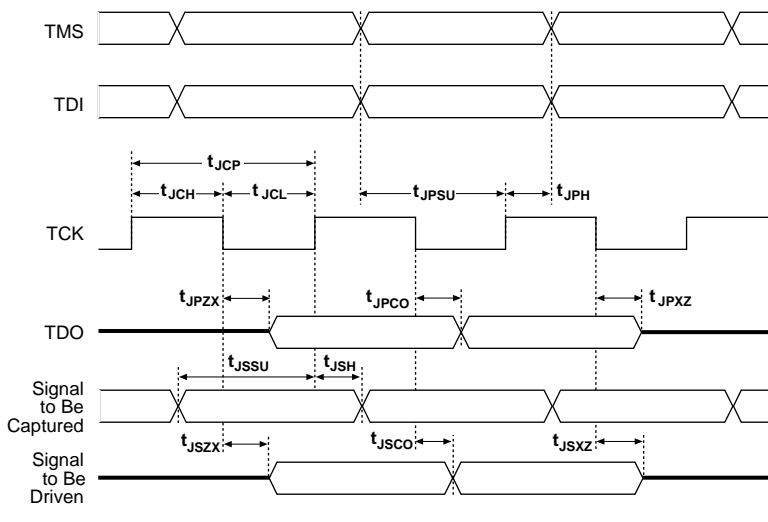


Table 11 shows the JTAG timing parameters and values for MAX 7000A devices.

**Table 11. JTAG Timing Parameters & Values for MAX 7000A Devices** *Note (1)*

Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns

**Note:**

(1) Timing parameters shown in this table apply for all specified VCCIO levels.

## Open-Drain Output Option

MAX 7000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Open-drain output pins on MAX 7000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high  $V_{IH}$ . When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V to meet CMOS  $V_{OH}$  requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

## Programmable Ground Pins

Each unused I/O pin on MAX 7000A devices may be used as an additional ground pin. In EPM7128A and EPM7256A devices, utilizing unused I/O pins as additional ground pins requires using the associated macrocell. In MAX 7000AE devices, this programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

## Slew-Rate Control

The output buffer for each MAX 7000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

## Power Sequencing & Hot-Socketing

Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

Signals can be driven into MAX 7000AE devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.

MAX 7000AE device I/O pins will not source or sink more than 300  $\mu$ A of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the OE1 and GLCRn pins. The OE1 and GLCRn pins can be driven up to 3.6 V during hot-socketing. After  $V_{CCINT}$  and  $V_{CCIO}$  reach the recommended operating conditions, these two pins are 5.0-V tolerant.

EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.

## Design Security

All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 9](#). Test patterns can be used and then erased during early stages of the production flow.



**Table 14. MAX 7000A Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (13)	3.0	3.6	V
$V_{CCIO}$	Supply voltage for output drivers, 3.3-V operation	(3)	3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation	(3)	2.3	2.7	V
$V_{CCISP}$	Supply voltage during in-system programming		3.0	3.6	V
$V_I$	Input voltage	(4)	−0.5	5.75	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_A$	Ambient temperature	Commercial range	0	70	°C
		Industrial range (5)	−40	85	°C
$T_J$	Junction temperature	Commercial range	0	90	°C
		Industrial range (5)	−40	105	°C
		Extended range (5)	−40	130	°C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 15. MAX 7000A Device DC Operating Conditions** *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{IH}$	High-level input voltage		1.7	5.75	V
$V_{IL}$	Low-level input voltage		-0.5	0.8	V
$V_{OH}$	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (7)	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (7)	$V_{CCIO} - 0.2$		V
	2.5-V high-level output voltage	$I_{OH} = -100$ $\mu$ A DC, $V_{CCIO} = 2.30$ V (7)	2.1		V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (7)	2.0		V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (7)	1.7		V
$V_{OL}$	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 3.00$ V (8)		0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)		0.2	V
	2.5-V low-level output voltage	$I_{OL} = 100$ $\mu$ A DC, $V_{CCIO} = 2.30$ V (8)		0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (8)		0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (8)		0.7	V
$I_I$	Input leakage current	$V_I = -0.5$ to $5.5$ V (9)	-10	10	$\mu$ A
$I_{OZ}$	Tri-state output off-state current	$V_I = -0.5$ to $5.5$ V (9)	-10	10	$\mu$ A
$R_{ISP}$	Value of I/O pin pull-up resistor during in-system programming or during power-up	$V_{CCIO} = 3.0$ to $3.6$ V (10)	20	50	k $\Omega$
		$V_{CCIO} = 2.3$ to $2.7$ V (10)	30	80	k $\Omega$
		$V_{CCIO} = 2.3$ to $3.6$ V (11)	20	74	k $\Omega$

**Table 16. MAX 7000A Device Capacitance** *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		8	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		8	pF

**Table 20. EPM7064AE Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.6		1.1		1.4	ns
$t_{IO}$	I/O input pad and buffer delay			0.6		1.1		1.4	ns
$t_{FIN}$	Fast input delay			2.5		3.0		3.7	ns
$t_{SEXP}$	Shared expander delay			1.8		3.0		3.9	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.7		0.9	ns
$t_{LAD}$	Logic array delay			1.5		2.5		3.2	ns
$t_{LAC}$	Logic control array delay			0.6		1.0		1.2	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.3		1.8	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.3		1.8		2.3	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.8		6.3		6.8	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		1.3		2.0		2.9		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{FSU}$	Register setup time of fast input		1.0		1.5		1.5		ns
$t_{FH}$	Register hold time of fast input		1.5		1.5		1.5		ns
$t_{RD}$	Register delay			0.7		1.2		1.6	ns
$t_{COMB}$	Combinatorial delay			0.6		0.9		1.3	ns
$t_{IC}$	Array clock delay			1.2		1.9		2.5	ns

**Table 22. EPM7128AE Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		1.0		1.4	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		1.0		1.4	ns
$t_{FIN}$	Fast input delay			2.5		3.0		3.4	ns
$t_{SEXP}$	Shared expander delay			2.0		2.9		3.8	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.7		0.9	ns
$t_{LAD}$	Logic array delay			1.6		2.4		3.1	ns
$t_{LAC}$	Logic control array delay			0.7		1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.2		1.6	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.3		1.7		2.1	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.8		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		1.4		2.1		2.9		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{FSU}$	Register setup time of fast input		1.1		1.6		1.6		ns
$t_{FH}$	Register hold time of fast input		1.4		1.4		1.4		ns
$t_{RD}$	Register delay			0.8		1.2		1.6	ns
$t_{COMB}$	Combinatorial delay			0.5		0.9		1.3	ns
$t_{IC}$	Array clock delay			1.2		1.7		2.2	ns

**Table 22. EPM7128AE Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{EN}$	Register enable time			0.7		1.0		1.3	ns
$t_{GLOB}$	Global control delay			1.1		1.6		2.0	ns
$t_{PRE}$	Register preset time			1.4		2.0		2.7	ns
$t_{CLR}$	Register clear time			1.4		2.0		2.7	ns
$t_{PIA}$	PIA delay	(2)		1.4		2.0		2.6	ns
$t_{LPA}$	Low-power adder	(6)		4.0		4.0		5.0	ns

**Table 26. EPM7512AE Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		0.9		1.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		0.9		1.0	ns
$t_{FIN}$	Fast input delay			3.1		3.6		4.1	ns
$t_{SEXP}$	Shared expander delay			2.7		3.5		4.4	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.5		0.6	ns
$t_{LAD}$	Logic array delay			2.2		2.8		3.5	ns
$t_{LAC}$	Logic control array delay			1.0		1.3		1.7	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.0		1.5		1.7	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.5		2.0		2.2	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.0		6.5		6.7	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		5.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		5.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		10.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		5.0		5.0	ns
$t_{SU}$	Register setup time		2.1		3.0		3.5		ns
$t_H$	Register hold time		0.6		0.8		1.0		ns
$t_{FSU}$	Register setup time of fast input		1.6		1.6		1.6		ns
$t_{FH}$	Register hold time of fast input		1.4		1.4		1.4		ns
$t_{RD}$	Register delay			1.3		1.7		2.1	ns
$t_{COMB}$	Combinatorial delay			0.6		0.8		1.0	ns

**Table 26. EPM7512AE Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
$t_{IC}$	Array clock delay			1.8		2.3		2.9	ns
$t_{EN}$	Register enable time			1.0		1.3		1.7	ns
$t_{GLOB}$	Global control delay			1.7		2.2		2.7	ns
$t_{PRE}$	Register preset time			1.0		1.4		1.7	ns
$t_{CLR}$	Register clear time			1.0		1.4		1.7	ns
$t_{PIA}$	PIA delay	(2)		3.0		4.0		4.8	ns
$t_{LPA}$	Low-power adder	(6)		4.5		5.0		5.0	ns

**Table 28. EPM7128A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{RD}$	Register delay			1.7		2.1		2.8		3.3	ns
$t_{COMB}$	Combinatorial delay			1.7		2.1		2.8		3.3	ns
$t_{IC}$	Array clock delay			2.4		3.0		4.1		4.9	ns
$t_{EN}$	Register enable time			2.4		3.0		4.1		4.9	ns
$t_{GLOB}$	Global control delay			1.0		1.2		1.7		2.0	ns
$t_{PRE}$	Register preset time			3.1		3.9		5.2		6.2	ns
$t_{CLR}$	Register clear time			3.1		3.9		5.2		6.2	ns
$t_{PIA}$	PIA delay	(2)		0.9		1.1		1.5		1.8	ns
$t_{LPA}$	Low-power adder	(6)		11.0		10.0		10.0		10.0	ns



The parameters in this equation are:

- $MC_{TON}$  = Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)  
 $MC_{DEV}$  = Number of macrocells in the device  
 $MC_{USED}$  = Total number of macrocells in the design, as reported in the Report File  
 $f_{MAX}$  = Highest clock frequency to the device  
 $to_{gLC}$  = Average percentage of logic cells toggling at each clock (typically 12.5%)  
A, B, C = Constants, shown in [Table 31](#)

**Table 31. MAX 7000A  $I_{CC}$  Equation Constants**

Device	A	B	C
EPM7032AE	0.71	0.30	0.014
EPM7064AE	0.71	0.30	0.014
EPM7128A	0.71	0.30	0.014
EPM7128AE	0.71	0.30	0.014
EPM7256A	0.71	0.30	0.014
EPM7256AE	0.71	0.30	0.014
EPM7512AE	0.71	0.30	0.014

This calculation provides an  $I_{CC}$  estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual  $I_{CC}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

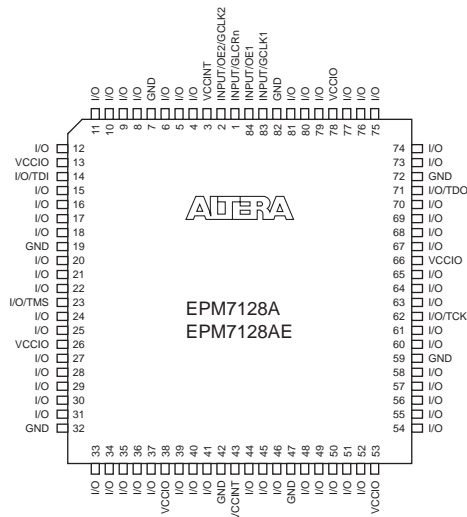
Figure 15. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outlines not drawn to scale.



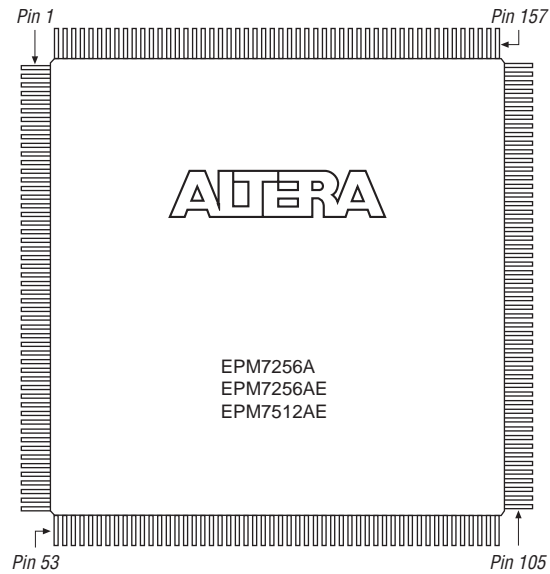
Figure 16. 84-Pin PLCC Package Pin-Out Diagram

Package outline not drawn to scale.



**Figure 21. 208-Pin PQFP Package Pin-Out Diagram**

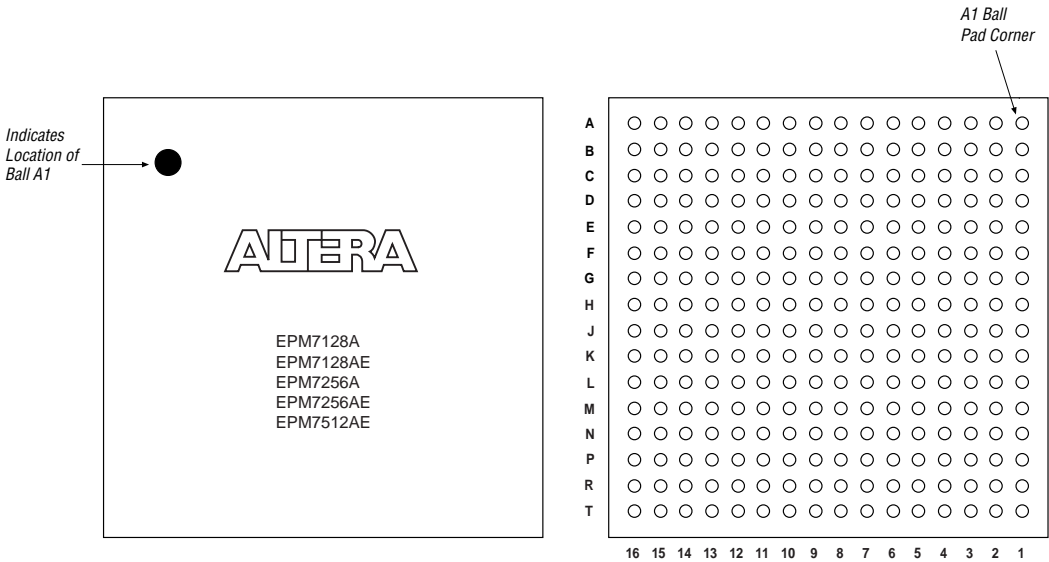
Package outline not drawn to scale.





**Figure 23. 256-Pin FineLine BGA Package Pin-Out Diagram**

Package outline not drawn to scale.



## Revision History

The information contained in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5 supersedes information published in previous versions.

### Version 4.5

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5:

- Updated text in the “Power Sequencing & Hot-Socketing” section.

### Version 4.4

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.4:

- Added Tables 5 through 7.
- Added “Programming Sequence” on page 17 and “Programming Times” on page 18.