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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	100
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7128aetc144-7n">https://www.e-xfl.com/product-detail/intel/epm7128aetc144-7n</a>



MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000A devices contain from 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms, providing up to 32 product terms per macrocell.

MAX 7000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5-V, 3.3-V, and 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems.

MAX 7000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0 and 3.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

## Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000A devices.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

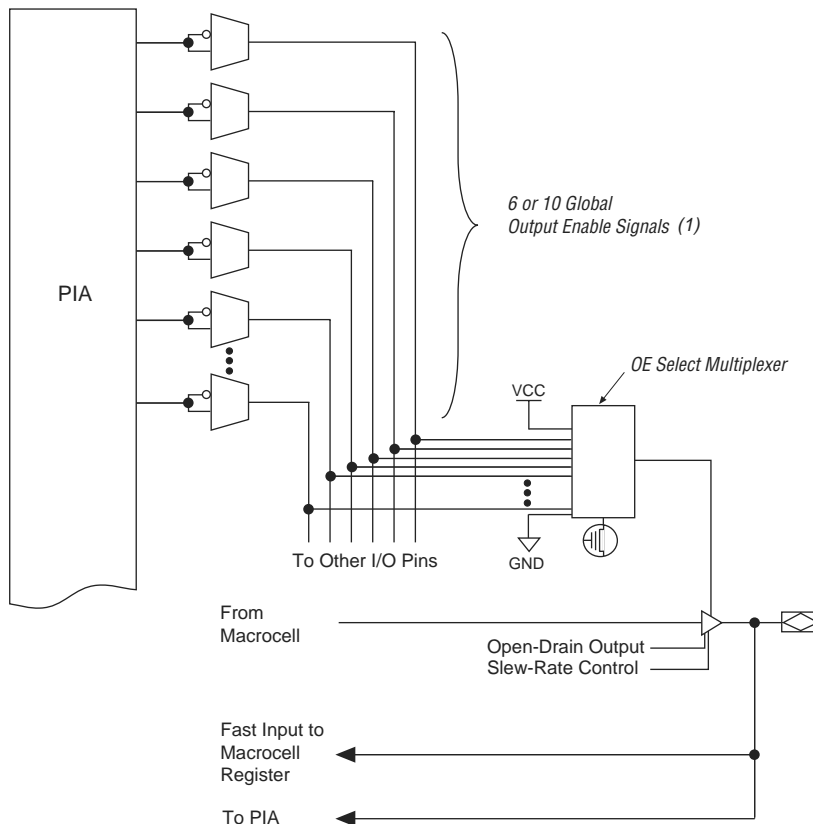
Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000A devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLR<sub>n</sub>). Upon power-up, each register in a MAX 7000AE device may be set to either a high or low state. This power-up state is specified at design entry. Upon power-up, each register in EPM7128A and EPM7256A devices are set to a low state.

All MAX 7000A I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (as low as 2.5 ns) input setup time.

**Figure 6. I/O Control Block of MAX 7000A Devices****Note:**

- (1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enable signals. EPM7512AE devices have 10 output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to  $V_{CC}$ , the output is enabled.

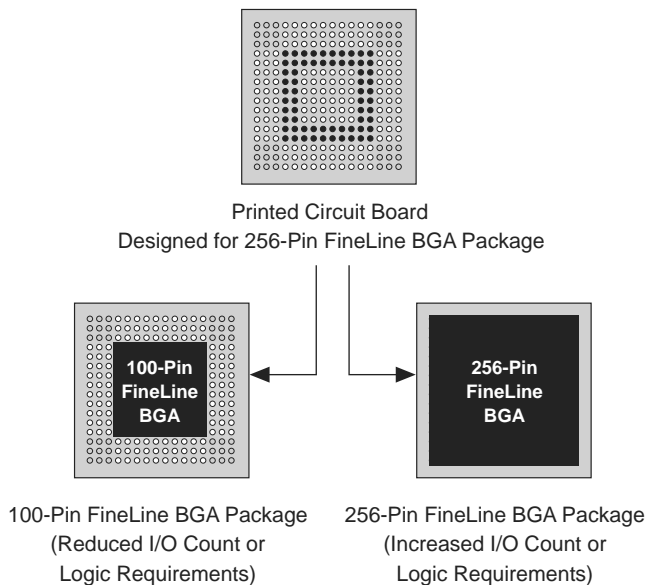
The MAX 7000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 7).

**Figure 7. SameFrame Pin-Out Example**



## In-System Programmability

MAX 7000A devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k $\Omega$ .

MAX 7000AE devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP\_Done bit that provides safe operation when in-system programming is interrupted. This ISP\_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is only available in EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, and EPM7512AE devices.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster serial/USB communications cable, ByteBlasterMV parallel port download cable, and BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000AE devices can be programmed with either an adaptive or constant (non-adaptive) algorithm. EPM7128A and EPM7256A device can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD 71, can be used to program MAX 7000A devices with in-circuit testers, PCs, or embedded processors.





For more information on using the Jam STAPL language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)*.

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

The instruction register length of MAX 7000A devices is 10 bits. The user electronic signature (UES) register length in MAX 7000A devices is 16 bits. The MAX 7000AE USERCODE register length is 32 bits. Tables 9 and 10 show the boundary-scan register length and device IDCODE information for MAX 7000A devices.

**Table 9. MAX 7000A Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPM7032AE	96
EPM7064AE	192
EPM7128A	288
EPM7128AE	288
EPM7256A	480
EPM7256AE	480
EPM7512AE	624

**Table 10. 32-Bit MAX 7000A Device IDCODE** *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM7032AE	0001	0111 0000 0011 0010	00001101110	1
EPM7064AE	0001	0111 0000 0110 0100	00001101110	1
EPM7128A	0000	0111 0001 0010 1000	00001101110	1
EPM7128AE	0001	0111 0001 0010 1000	00001101110	1
EPM7256A	0000	0111 0010 0101 0110	00001101110	1
EPM7256AE	0001	0111 0010 0101 0110	00001101110	1
EPM7512AE	0001	0111 0101 0001 0010	00001101110	1

**Notes:**

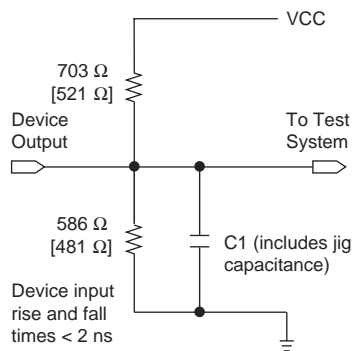
- (1) The most significant bit (MSB) is on the left.  
 (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



See Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices) for more information on JTAG BST.

**Figure 9. MAX 7000A AC Test Conditions**

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs.



## Operating Conditions

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000A devices.

**Table 13. MAX 7000A Device Absolute Maximum Ratings** Note (1)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to ground (2)	-0.5	4.6	V
$V_I$	DC input voltage		-2.0	5.75	V
$I_{OUT}$	DC output current, per pin		-25	25	mA
$T_{STG}$	Storage temperature	No bias	-65	150	°C
$T_A$	Ambient temperature	Under bias	-65	135	°C
$T_J$	Junction temperature	BGA, FineLine BGA, PQFP, and TQFP packages, under bias		135	°C

**Table 14. MAX 7000A Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (13)	3.0	3.6	V
$V_{CCIO}$	Supply voltage for output drivers, 3.3-V operation	(3)	3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation	(3)	2.3	2.7	V
$V_{CCISP}$	Supply voltage during in-system programming		3.0	3.6	V
$V_I$	Input voltage	(4)	-0.5	5.75	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_A$	Ambient temperature	Commercial range	0	70	°C
		Industrial range (5)	-40	85	°C
$T_J$	Junction temperature	Commercial range	0	90	°C
		Industrial range (5)	-40	105	°C
		Extended range (5)	-40	130	°C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 15. MAX 7000A Device DC Operating Conditions** *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{IH}$	High-level input voltage		1.7	5.75	V
$V_{IL}$	Low-level input voltage		-0.5	0.8	V
$V_{OH}$	3.3-V high-level TTL output voltage	$I_{OH} = -8 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (7)	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (7)	$V_{CCIO} - 0.2$		V
	2.5-V high-level output voltage	$I_{OH} = -100 \text{ } \mu\text{A DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (7)	2.1		V
		$I_{OH} = -1 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (7)	2.0		V
		$I_{OH} = -2 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (7)	1.7		V
$V_{OL}$	3.3-V low-level TTL output voltage	$I_{OL} = 8 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (8)		0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (8)		0.2	V
	2.5-V low-level output voltage	$I_{OL} = 100 \text{ } \mu\text{A DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (8)		0.2	V
		$I_{OL} = 1 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (8)		0.4	V
		$I_{OL} = 2 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (8)		0.7	V
$I_I$	Input leakage current	$V_I = -0.5 \text{ to } 5.5 \text{ V}$ (9)	-10	10	$\mu\text{A}$
$I_{OZ}$	Tri-state output off-state current	$V_I = -0.5 \text{ to } 5.5 \text{ V}$ (9)	-10	10	$\mu\text{A}$
$R_{ISP}$	Value of I/O pin pull-up resistor during in-system programming or during power-up	$V_{CCIO} = 3.0 \text{ to } 3.6 \text{ V}$ (10)	20	50	$\text{k}\Omega$
		$V_{CCIO} = 2.3 \text{ to } 2.7 \text{ V}$ (10)	30	80	$\text{k}\Omega$
		$V_{CCIO} = 2.3 \text{ to } 3.6 \text{ V}$ (11)	20	74	$\text{k}\Omega$

**Table 16. MAX 7000A Device Capacitance** *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input pin capacitance	$V_{IN} = 0 \text{ V}$ , $f = 1.0 \text{ MHz}$		8	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0 \text{ V}$ , $f = 1.0 \text{ MHz}$		8	pF

**Table 18. EPM7032AE Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IC}$	Array clock delay			1.2		2.0		2.5	ns
$t_{EN}$	Register enable time			0.6		1.0		1.2	ns
$t_{GLOB}$	Global control delay			0.8		1.3		1.9	ns
$t_{PRE}$	Register preset time			1.2		1.9		2.6	ns
$t_{CLR}$	Register clear time			1.2		1.9		2.6	ns
$t_{PIA}$	PIA delay	(2)		0.9		1.5		2.1	ns
$t_{LPA}$	Low-power adder	(6)		2.5		4.0		5.0	ns

**Table 24. EPM7256AE Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		0.9		1.2	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		0.9		1.2	ns
$t_{FIN}$	Fast input delay			2.4		2.9		3.4	ns
$t_{SEXP}$	Shared expander delay			2.1		2.8		3.7	ns
$t_{PEXP}$	Parallel expander delay			0.3		0.5		0.6	ns
$t_{LAD}$	Logic array delay			1.7		2.2		2.8	ns
$t_{LAC}$	Logic control array delay			0.8		1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.6	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.4		1.7		2.1	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.9		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		1.5		2.1		2.9		ns
$t_H$	Register hold time		0.7		0.9		1.2		ns
$t_{FSU}$	Register setup time of fast input		1.1		1.6		1.6		ns
$t_{FH}$	Register hold time of fast input		1.4		1.4		1.4		ns
$t_{RD}$	Register delay			0.9		1.2		1.6	ns
$t_{COMB}$	Combinatorial delay			0.5		0.8		1.2	ns

**Table 28. EPM7128A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{RD}$	Register delay			1.7		2.1		2.8		3.3	ns
$t_{COMB}$	Combinatorial delay			1.7		2.1		2.8		3.3	ns
$t_{IC}$	Array clock delay			2.4		3.0		4.1		4.9	ns
$t_{EN}$	Register enable time			2.4		3.0		4.1		4.9	ns
$t_{GLOB}$	Global control delay			1.0		1.2		1.7		2.0	ns
$t_{PRE}$	Register preset time			3.1		3.9		5.2		6.2	ns
$t_{CLR}$	Register clear time			3.1		3.9		5.2		6.2	ns
$t_{PIA}$	PIA delay	(2)		0.9		1.1		1.5		1.8	ns
$t_{LPA}$	Low-power adder	(6)		11.0		10.0		10.0		10.0	ns



**Table 30. EPM7256A Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.4		0.5		0.6	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.4		0.5		0.6	ns
$t_{FIN}$	Fast input delay			2.4		3.0		3.4		3.8	ns
$t_{SEXP}$	Shared expander delay			2.8		3.5		4.7		5.6	ns
$t_{PEXP}$	Parallel expander delay			0.5		0.6		0.8		1.0	ns
$t_{LAD}$	Logic array delay			2.5		3.1		4.2		5.0	ns
$t_{LAC}$	Logic control array delay			2.5		3.1		4.2		5.0	ns
$t_{IOE}$	Internal output enable delay			0.2		0.3		0.4		0.5	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.3		0.4		0.5		0.6	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		0.8		0.9		1.0		1.1	ns
$t_{OD3}$	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.3		5.4		5.5		5.6	ns
$t_{ZX1}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0		5.0	ns
$t_{SU}$	Register setup time		1.0		1.3		1.7		2.0		ns
$t_H$	Register hold time		1.7		2.4		3.7		4.7		ns
$t_{FSU}$	Register setup time of fast input		1.2		1.4		1.4		1.4		ns
$t_{FH}$	Register hold time of fast input		1.3		1.6		1.6		1.6		ns
$t_{RD}$	Register delay			1.6		2.0		2.7		3.2	ns

**Table 30. EPM7256A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{COMB}$	Combinatorial delay			1.6		2.0		2.7		3.2	ns
$t_{IC}$	Array clock delay			2.7		3.4		4.5		5.4	ns
$t_{EN}$	Register enable time			2.5		3.1		4.2		5.0	ns
$t_{GLOB}$	Global control delay			1.1		1.4		1.8		2.2	ns
$t_{PRE}$	Register preset time			2.3		2.9		3.8		4.6	ns
$t_{CLR}$	Register clear time			2.3		2.9		3.8		4.6	ns
$t_{PIA}$	PIA delay	(2)		1.3		1.6		2.1		2.6	ns
$t_{LPA}$	Low-power adder	(6)		11.0		10.0		10.0		10.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14 on page 28. See Figure 12 for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (3) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (4) This parameter is measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) Operating conditions:  $V_{CCIO} = 2.5 \pm 0.2$  V for commercial and industrial use.
- (6) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPW}$  parameters for macrocells running in low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{MAX}$ , in MHz) for MAX 7000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The  $I_{CCINT}$  value depends on the switching frequency and the application logic. The  $I_{CCINT}$  value is calculated with the following equation:

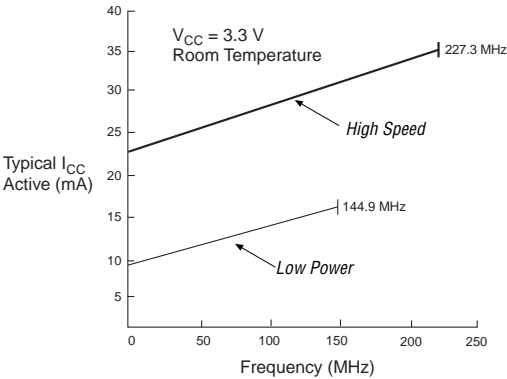
$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times \log_{LC})$$

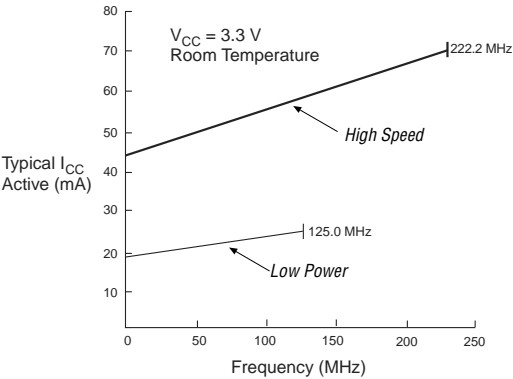
Figure 13 shows the typical supply current versus frequency for MAX 7000A devices.

Figure 13.  $I_{CC}$  vs. Frequency for MAX 7000A Devices (Part 1 of 2)

EPM7032AE



EPM7064AE



EPM7128A & EPM7128AE

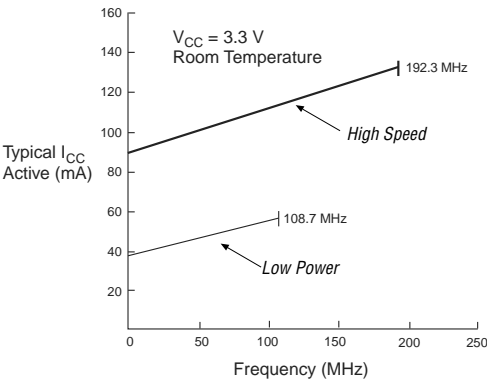


Figure 19. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

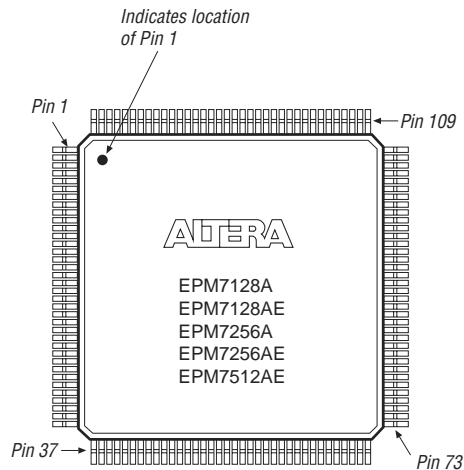


Figure 20. 169-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

