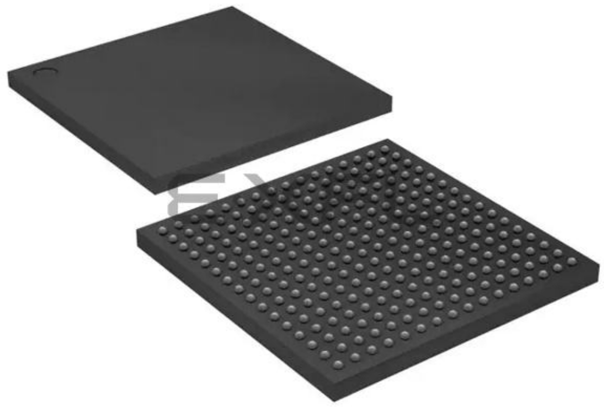
Intel - EPM7256AEFC256-10 Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	164
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256aefc256-10

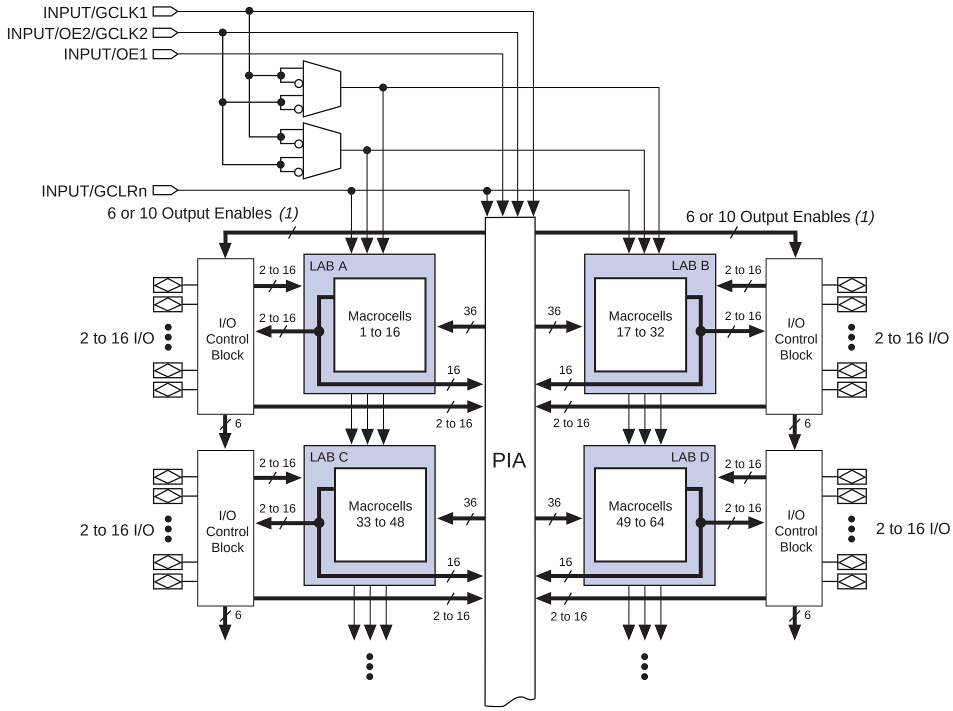
Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000A devices.

Figure 1. MAX 7000A Device Block Diagram



Note:

(1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables. EPM7512AE devices have 10 output enables.

Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

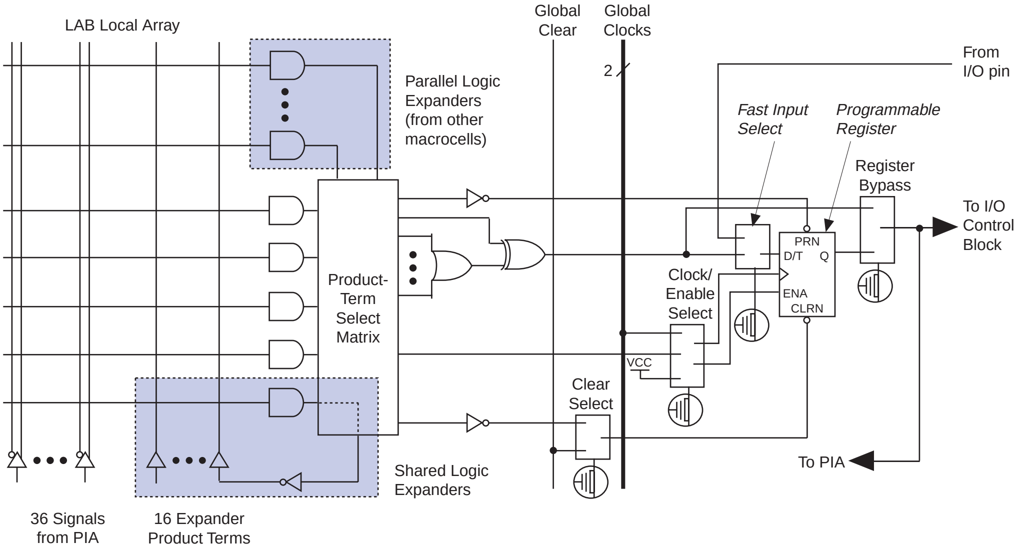
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Macrocells

MAX 7000A macrocells can be individually configured for either sequential or combinatorial logic operation. The macrocells consist of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows a MAX 7000A macrocell.

Figure 2. MAX 7000A Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the `OR` and `XOR` gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

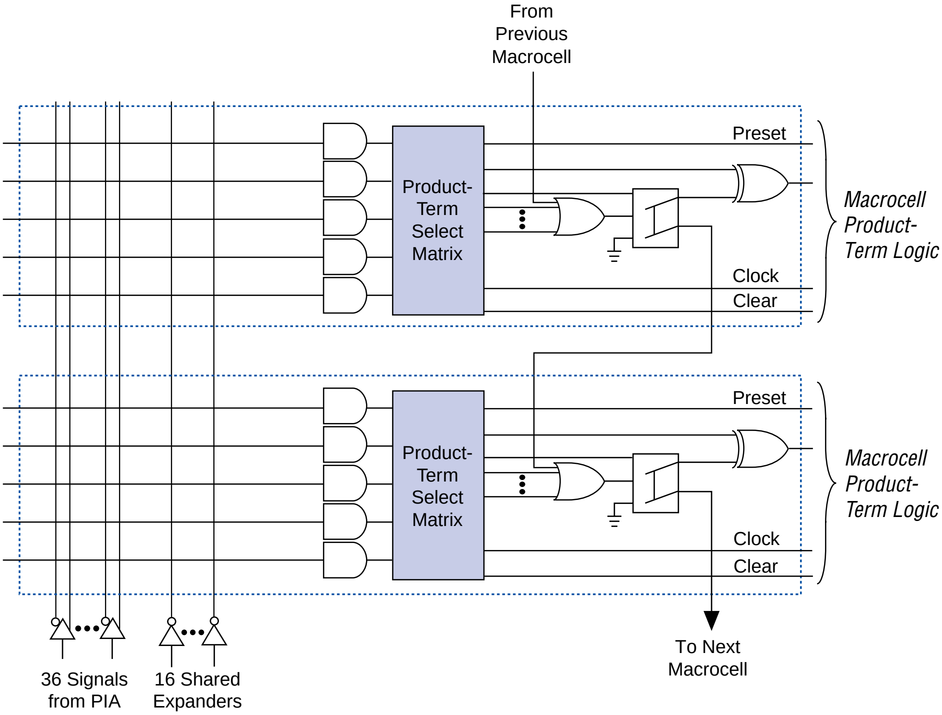
Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

Figure 4. MAX 7000A Parallel Expanders

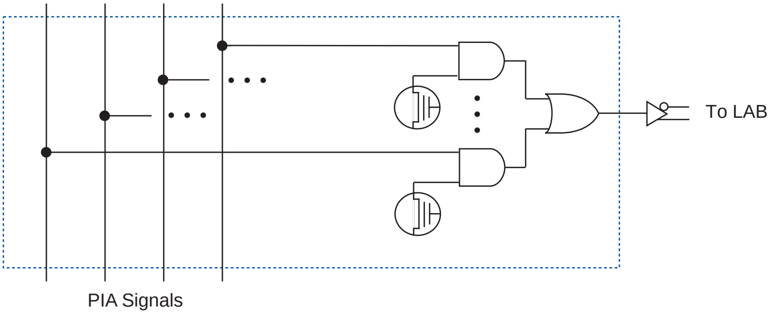
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 5. MAX 7000A PIA Routing



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 7000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Table 8. MAX 7000A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the `TDI` and `TDO` pins, allowing the IDCODE to be serially shifted out of `TDO`
USERCODE	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE value to be shifted out of `TDO`. The USERCODE instruction is available for MAX 7000AE devices only
UESCODE	These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be shifted out of `TDO`. UESCODE instructions are available for EPM7128A and EPM7256A devices only.
ISP Instructions	These instructions are used when programming MAX 7000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam STAPL File, JBC File, or SVF File via an embedded processor or test equipment.

Programmable Speed/Power Control

MAX 7000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000A device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power operation (i.e., with the Turbo Bit option turned off). As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters.

Output Configuration

MAX 7000A device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000A devices to connect to systems with differing supply voltages. MAX 7000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of `VCC` pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The `VCCIO` pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the `VCCIO` pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 3.0 V incur a slightly greater timing delay of t_{OD2} instead of t_{OD1}. Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 12 describes the MAX 7000A MultiVolt I/O support.

Table 12. MAX 7000A MultiVolt I/O Support

V_{CCIO} Voltage	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓		✓	✓

Open-Drain Output Option

MAX 7000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-`OR` plane.

Open-drain output pins on MAX 7000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high V_{IH}. When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V to meet CMOS V_{OH} requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Programmable Ground Pins

Each unused I/O pin on MAX 7000A devices may be used as an additional ground pin. In EPM7128A and EPM7256A devices, utilizing unused I/O pins as additional ground pins requires using the associated macrocell. In MAX 7000AE devices, this programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Power Sequencing & Hot-Socketing

Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000AE devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.

MAX 7000AE device I/O pins will not source or sink more than 300 µA of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the `OE1` and `GLCRn` pins. The `OE1` and `GLCRn` pins can be driven up to 3.6 V during hot-socketing. After V_{CCINT} and V_{CCIO} reach the recommended operating conditions, these two pins are 5.0-V tolerant.

EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.

Design Security

All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9. Test patterns can be used and then erased during early stages of the production flow.

Table 14. MAX 7000A Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(13)*	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation	*(3)*	3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation	*(3)*	2.3	2.7	V
V_{CCISP}	Supply voltage during in-system programming		3.0	3.6	V
V_I	Input voltage	*(4)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	Commercial range	0	70	° C
		Industrial range *(5)*	–40	85	° C
T_J	Junction temperature	Commercial range	0	90	° C
		Industrial range *(5)*	–40	105	° C
		Extended range *(5)*	–40	130	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 20. EPM7064AE Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		1.1		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.6		1.1		1.4	ns
t_{FIN}	Fast input delay			2.5		3.0		3.7	ns
t_{SEXP}	Shared expander delay			1.8		3.0		3.9	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.5		2.5		3.2	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.9		ns
t_{H}	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.7		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.6		0.9		1.3	ns
t_{IC}	Array clock delay			1.2		1.9		2.5	ns

Table 20. EPM7064AE Internal Timing Parameters (Part 2 of 2) Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			1.0		1.5		2.2	ns
t_{PRE}	Register preset time			1.3		2.1		2.9	ns
t_{CLR}	Register clear time			1.3		2.1		2.9	ns
t_{PIA}	PIA delay	*(2)*		1.0		1.7		2.3	ns
t_{LPA}	Low-power adder	*(6)*		3.5		4.0		5.0	ns

Table 21. EPM7128AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		5.0		7.5		10	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		5.0		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	3.3		4.9		6.6		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.4	1.0	5.0	1.0	6.6	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.8		2.8		3.8		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.9	1.0	7.1	1.0	9.4	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		5.2		7.7		10.2	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	192.3		129.9		98.0		MHz
t_{ACNT}	Minimum array clock period	*(2)*		5.2		7.7		10.2	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	192.3		129.9		98.0		MHz

Table 24. EPM7256AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IC}	Array clock delay			1.2		1.6		2.1	ns
t_{EN}	Register enable time			0.8		1.0		1.3	ns
t_{GLOB}	Global control delay			1.0		1.5		2.0	ns
t_{PRE}	Register preset time			1.6		2.3		3.0	ns
t_{CLR}	Register clear time			1.6		2.3		3.0	ns
t_{PIA}	PIA delay	*(2)*		1.7		2.4		3.2	ns
t_{LPA}	Low-power adder	*(6)*		4.0		4.0		5.0	ns

Table 26. EPM7512AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{IC}	Array clock delay			1.8		2.3		2.9	ns
t_{EN}	Register enable time			1.0		1.3		1.7	ns
t_{GLOB}	Global control delay			1.7		2.2		2.7	ns
t_{PRE}	Register preset time			1.0		1.4		1.7	ns
t_{CLR}	Register clear time			1.0		1.4		1.7	ns
t_{PIA}	PIA delay	*(2)*		3.0		4.0		4.8	ns
t_{LPA}	Low-power adder	*(6)*		4.5		5.0		5.0	ns

Table 27. EPM7128A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		6.0		7.5		10.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		6.0		7.5		10.0		12.0	ns
t_{SU}	Global clock setup time	*(2)*	4.2		5.3		7.0		8.5		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.7	1.0	4.6	1.0	6.1	1.0	7.3	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.9		2.4		3.1		3.8		ns
t_{AH}	Array clock hold time	*(2)*	1.5		2.2		3.3		4.3		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	6.0	1.0	7.5	1.0	10.0	1.0	12.0	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		5.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		5.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		3.0		4.0		5.0		ns
t_{CNT}	Minimum global clock period	*(2)*		6.9		8.6		11.5		13.8	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	144.9		116.3		87.0		72.5		MHz
t_{ACNT}	Minimum array clock period	*(2)*		6.9		8.6		11.5		13.8	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	144.9		116.3		87		72.5		MHz

Table 28. EPM7128A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{RD}	Register delay			1.7		2.1		2.8		3.3	ns
t_{COMB}	Combinatorial delay			1.7		2.1		2.8		3.3	ns
t_{IC}	Array clock delay			2.4		3.0		4.1		4.9	ns
t_{EN}	Register enable time			2.4		3.0		4.1		4.9	ns
t_{GLOB}	Global control delay			1.0		1.2		1.7		2.0	ns
t_{PRE}	Register preset time			3.1		3.9		5.2		6.2	ns
t_{CLR}	Register clear time			3.1		3.9		5.2		6.2	ns
t_{PIA}	PIA delay	*(2)*		0.9		1.1		1.5		1.8	ns
t_{LPA}	Low-power adder	*(6)*		11.0		10.0		10.0		10.0	ns

Table 30. EPM7256A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{COMB}	Combinatorial delay			1.6		2.0		2.7		3.2	ns
t_{IC}	Array clock delay			2.7		3.4		4.5		5.4	ns
t_{EN}	Register enable time			2.5		3.1		4.2		5.0	ns
t_{GLOB}	Global control delay			1.1		1.4		1.8		2.2	ns
t_{PRE}	Register preset time			2.3		2.9		3.8		4.6	ns
t_{CLR}	Register clear time			2.3		2.9		3.8		4.6	ns
t_{PIA}	PIA delay	(2)		1.3		1.6		2.1		2.6	ns
t_{LPA}	Low-power adder	(6)		11.0		10.0		10.0		10.0	ns

Notes to tables:

(1) These values are specified under the recommended operating conditions shown in Table 14 on page 28. See Figure 12 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(4) This parameter is measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) Operating conditions: $V_{CCIO} = 2.5 \pm 0.2$ V for commercial and industrial use.

(6) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

Figure 17. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

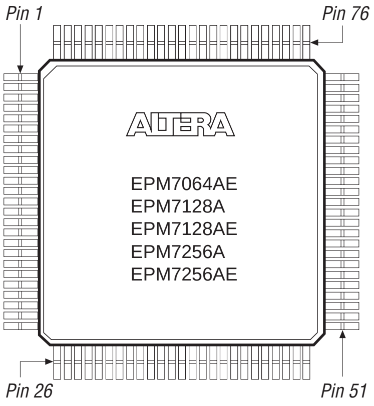
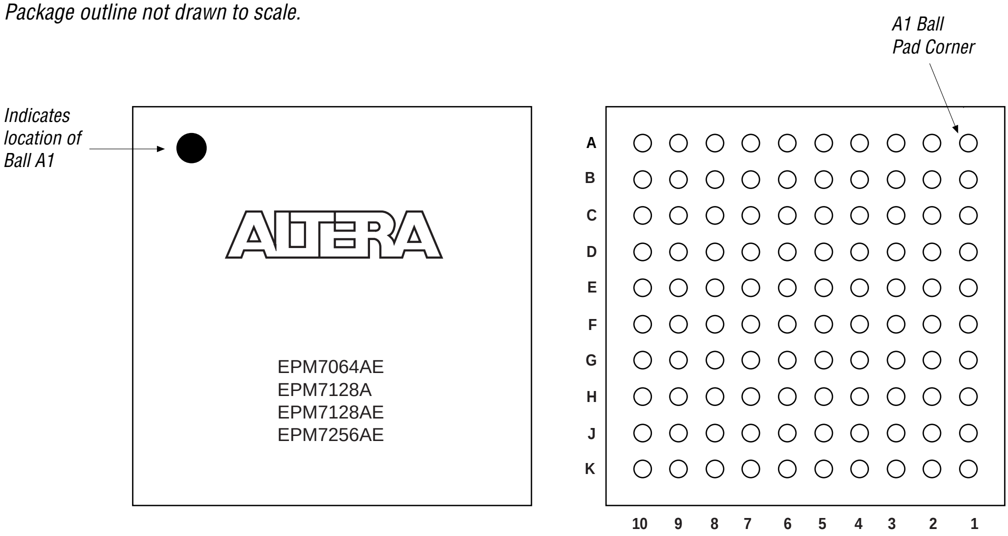


Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



Version 4.3

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.3:

- Added extended temperature devices to document
- Updated Table 14.

Version 4.2

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.2:

- Removed *Note (1)* from Table 2.
- Removed *Note (4)* from Tables 3 and 4.

Version 4.1

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.1:

- Updated leakage current information in Table 15.
- Updated *Note (9)* of Table 15.
- Updated *Note (1)* of Tables 17 through 30.

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