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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	164
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256aefc256-5n

The MAX 7000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices including PALs, GALs, and 22V10s devices. MAX 7000A devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, Ultra FineLine BGA, PQFP, and TQFP packages. See Table 3 and Table 4.

Table 3. MAX 7000A Maximum User I/O Pins   *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	49-Pin Ultra FineLine BGA *(2)*	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine BGA *(3)*
EPM7032AE	36	36				
EPM7064AE	36	36	41		68	68
EPM7128A				68	84	84
EPM7128AE				68	84	84
EPM7256A					84	
EPM7256AE					84	84
EPM7512AE						

Table 4. MAX 7000A Maximum User I/O Pins   *Note (1)*

Device	144-Pin TQFP	169-Pin Ultra FineLine BGA *(2)*	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA *(3)*
EPM7032AE					
EPM7064AE					
EPM7128A	100				100
EPM7128AE	100	100			100
EPM7256A	120		164		164
EPM7256AE	120		164		164
EPM7512AE	120		176	212	212

Notes to tables:

(1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

(2) All Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.

(3) All FineLine BGA packages are footprint-compatible via the SameFrame feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.

MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000A devices contain from 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms, providing up to 32 product terms per macrocell.

MAX 7000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5-V, 3.3-V, and 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems.

MAX 7000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders, and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 7).

Figure 7. SameFrame Pin-Out Example

Printed Circuit Board
Designed for 256-Pin FineLine BGA Package

100-Pin FineLine BGA Package
(Reduced I/O Count or
Logic Requirements)

256-Pin FineLine BGA Package
(Increased I/O Count or
Logic Requirements)
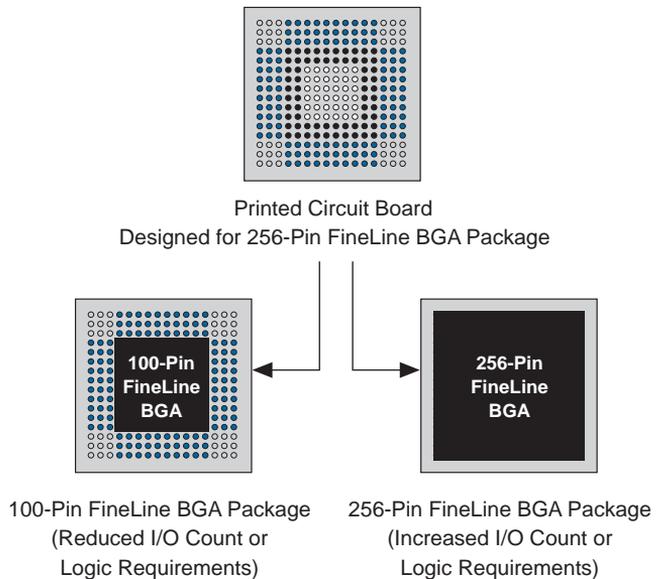
For more information on using the Jam STAPL language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)*.

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000A Device

The time required to program a single MAX 7000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Table 8. MAX 7000A JTAG Instructions	
JTAG Instruction	**Description**
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the `TDI` and `TDO` pins, allowing the IDCODE to be serially shifted out of `TDO`
USERCODE	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE value to be shifted out of `TDO`. The USERCODE instruction is available for MAX 7000AE devices only
UESCODE	These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be shifted out of `TDO`. UESCODE instructions are available for EPM7128A and EPM7256A devices only.
ISP Instructions	These instructions are used when programming MAX 7000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam STAPL File, JBC File, or SVF File via an embedded processor or test equipment.

Figure 8 shows timing information for the JTAG signals.

Figure 8. MAX 7000A JTAG Waveforms
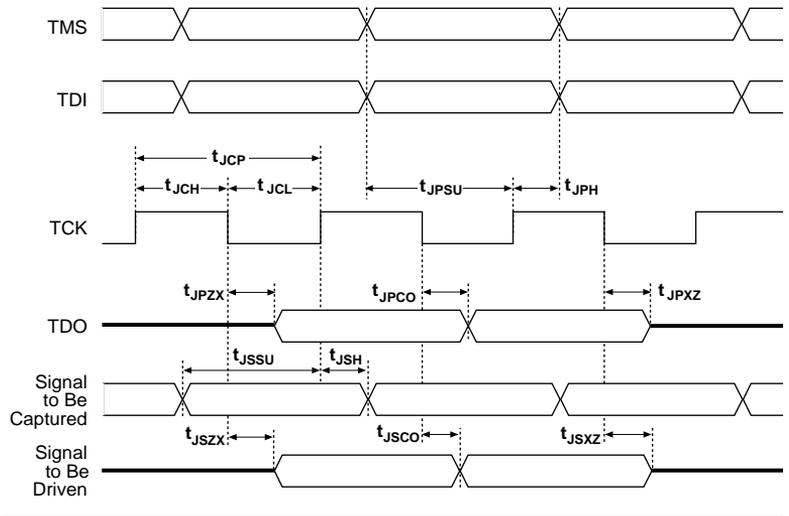
Table 11 shows the JTAG timing parameters and values for MAX 7000A devices.

	Table 11. JTAG Timing Parameters & Values for MAX 7000A Devices *Note (1)*			
Symbol	**Parameter**	**Min**	**Max**	**Unit**
t$_{JCP}$	TCK clock period	100		ns
t$_{JCH}$	TCK clock high time	50		ns
t$_{JCL}$	TCK clock low time	50		ns
t$_{JPSU}$	JTAG port setup time	20		ns
t$_{JPH}$	JTAG port hold time	45		ns
t$_{JPCO}$	JTAG port clock to output		25	ns
t$_{JPZX}$	JTAG port high impedance to valid output		25	ns
t$_{JPXZ}$	JTAG port valid output to high impedance		25	ns
t$_{JSSU}$	Capture register setup time	20		ns
t$_{JSH}$	Capture register hold time	45		ns
t$_{JSCO}$	Update register clock to output		25	ns
t$_{JSZX}$	Update register high impedance to valid output		25	ns
t$_{JSXZ}$	Update register valid output to high impedance		25	ns

Note:

(1)   Timing parameters shown in this table apply for all specified VCCIO levels.

Programmable Speed/Power Control

MAX 7000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000A device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power operation (i.e., with the Turbo Bit option turned off). As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters.

Output Configuration

MAX 7000A device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000A devices to connect to systems with differing supply voltages. MAX 7000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 3.0 V incur a slightly greater timing delay of t_{OD2} instead of t_{OD1}. Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 12 describes the MAX 7000A MultiVolt I/O support.

Table 12. MAX 7000A MultiVolt I/O Support						
V_{CCIO} Voltage	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓		✓	✓

Power Sequencing & Hot-Socketing	Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000AE devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.

MAX 7000AE device I/O pins will not source or sink more than 300 µA of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the OE1 and GLCRn pins. The OE1 and GLCRn pins can be driven up to 3.6 V during hot-socketing. After V_{CCINT} and V_{CCIO} reach the recommended operating conditions, these two pins are 5.0-V tolerant.

EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.

Design Security

All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9. Test patterns can be used and then erased during early stages of the production flow.

Tables 17 through 30 show EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, EPM7512AE, EPM7128A, and EPM7256A timing information.

Table 17. EPM7032AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		**-7**		**-10**		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		4.5		7.5		10	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		4.5		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	2.9		4.7		6.3		ns
t_H	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.6		2.5		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.3		0.5		0.5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.3	1.0	7.2	1.0	9.4	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		4.4		7.2		9.7	ns
f_{CNT}	Maximum internal global clock frequency	*(2), (4)*	227.3		138.9		103.1		MHz
t_{ACNT}	Minimum array clock period	*(2)*		4.4		7.2		9.7	ns
f_{ACNT}	Maximum internal array clock frequency	*(2), (4)*	227.3		138.9		103.1		MHz

Table 18. EPM7032AE Internal Timing Parameters *(Part 1 of 2)* *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		1.2		1.5	ns
t_{IO}	I/O input pad and buffer delay			0.7		1.2		1.5	ns
t_{FIN}	Fast input delay			2.3		2.8		3.4	ns
t_{SEXP}	Shared expander delay			1.9		3.1		4.0	ns
t_{PEXP}	Parallel expander delay			0.5		0.8		1.0	ns
t_{LAD}	Logic array delay			1.5		2.5		3.3	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.8		ns
t_H	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.7		1.2		1.5	ns
t_{COMB}	Combinatorial delay			0.6		1.0		1.3	ns

Table 20. EPM7064AE Internal Timing Parameters (Part 1 of 2) Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		1.1		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.6		1.1		1.4	ns
t_{FIN}	Fast input delay			2.5		3.0		3.7	ns
t_{SEXP}	Shared expander delay			1.8		3.0		3.9	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.5		2.5		3.2	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF (5)		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF (5)		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.9		ns
t_{H}	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.7		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.6		0.9		1.3	ns
t_{IC}	Array clock delay			1.2		1.9		2.5	ns

Table 25. EPM7512AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		**-10**		**-12**		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		7.5		10.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		7.5		10.0		12.0	ns
t_{SU}	Global clock setup time	*(2)*	5.6		7.6		9.1		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	4.7	1.0	6.3	1.0	7.5	ns
t_{CH}	Global clock high time		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time	*(2)*	2.5		3.5		4.1		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	7.8	1.0	10.4	1.0	12.5	ns
t_{ACH}	Array clock high time		3.0		4.0		5.0		ns
t_{ACL}	Array clock low time		3.0		4.0		5.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		4.0		5.0		ns
t_{CNT}	Minimum global clock period	*(2)*		8.6		11.5		13.9	ns
f_{CNT}	Maximum internal global clock frequency	*(2), (4)*	116.3		87.0		71.9		MHz
t_{ACNT}	Minimum array clock period	*(2)*		8.6		11.5		13.9	ns
f_{ACNT}	Maximum internal array clock frequency	*(2), (4)*	116.3		87.0		71.9		MHz

|	*Table 30. EPM7256A Internal Timing Parameters (Part 1 of 2)*		*Note (1)*								
Symbol	**Parameter**	**Conditions**				**Speed Grade**					**Unit**
			-6		**-7**		**-10**		**-12**		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.4		0.5		0.6	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.4		0.5		0.6	ns
t_{FIN}	Fast input delay			2.4		3.0		3.4		3.8	ns
t_{SEXP}	Shared expander delay			2.8		3.5		4.7		5.6	ns
t_{PEXP}	Parallel expander delay			0.5		0.6		0.8		1.0	ns
t_{LAD}	Logic array delay			2.5		3.1		4.2		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.1		4.2		5.0	ns
t_{IOE}	Internal output enable delay			0.2		0.3		0.4		0.5	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.3		0.4		0.5		0.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		0.8		0.9		1.0		1.1	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.3		5.4		5.5		5.6	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		4.5		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		5.0	ns
t_{SU}	Register setup time		1.0		1.3		1.7		2.0		ns
t_{H}	Register hold time		1.7		2.4		3.7		4.7		ns
t_{FSU}	Register setup time of fast input		1.2		1.4		1.4		1.4		ns
t_{FH}	Register hold time of fast input		1.3		1.6		1.6		1.6		ns
t_{RD}	Register delay			1.6		2.0		2.7		3.2	ns

Figure 13 shows the typical supply current versus frequency for MAX 7000A devices.

Figure 13. I$_{CC}$ vs. Frequency for MAX 7000A Devices (Part 1 of 2)

EPM7032AE
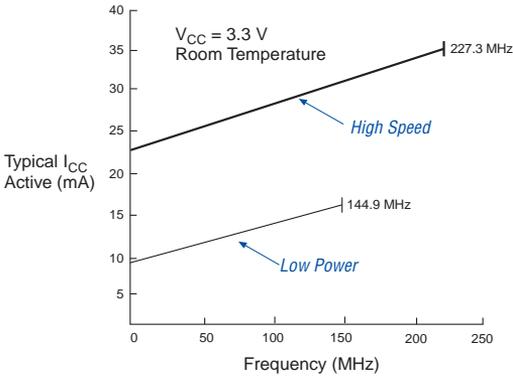
**EPM7064AE**
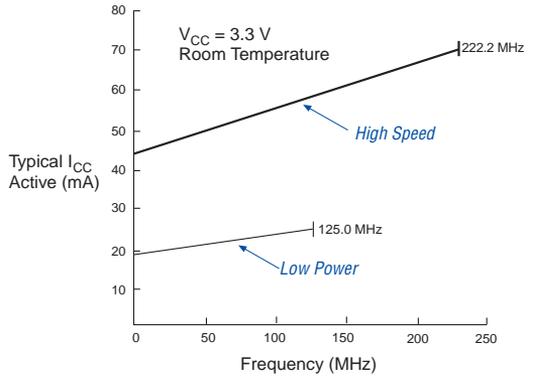
EPM7128A & EPM7128AE
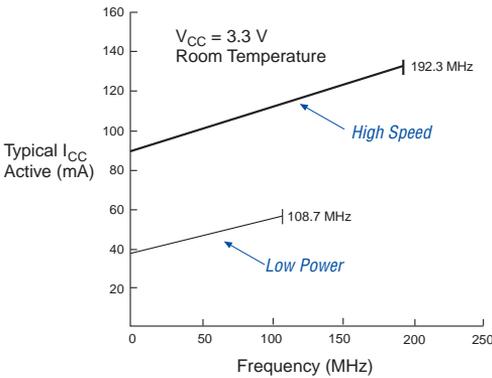
*Figure 15. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram*

Package outlines not drawn to scale.

*Figure 16. 84-Pin PLCC Package Pin-Out Diagram*

Package outline not drawn to scale.
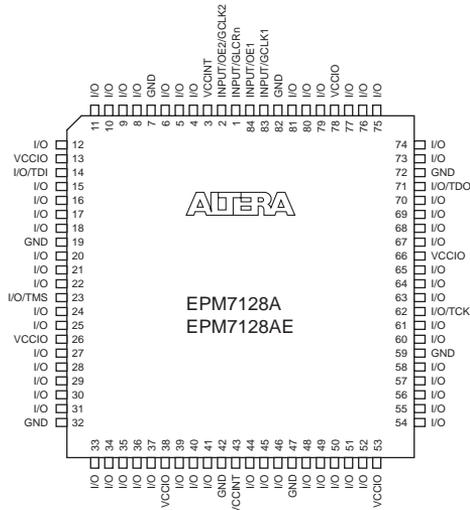
Figure 17. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.
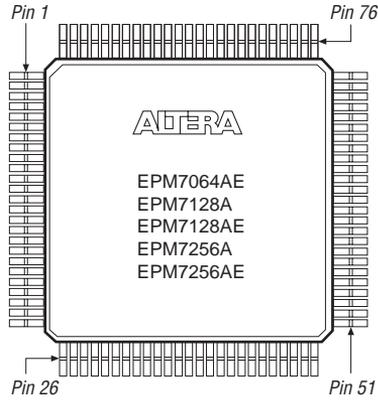
Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.
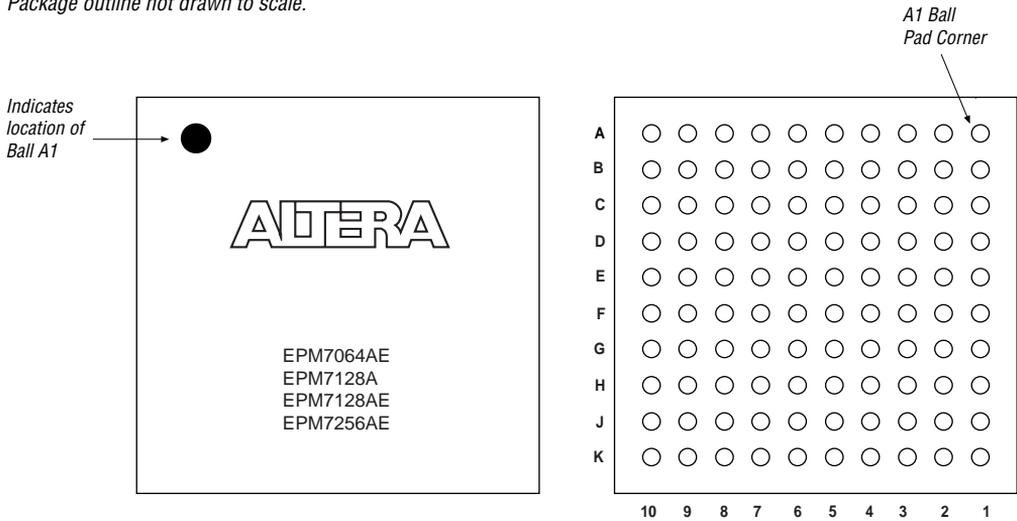
Figure 23. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.
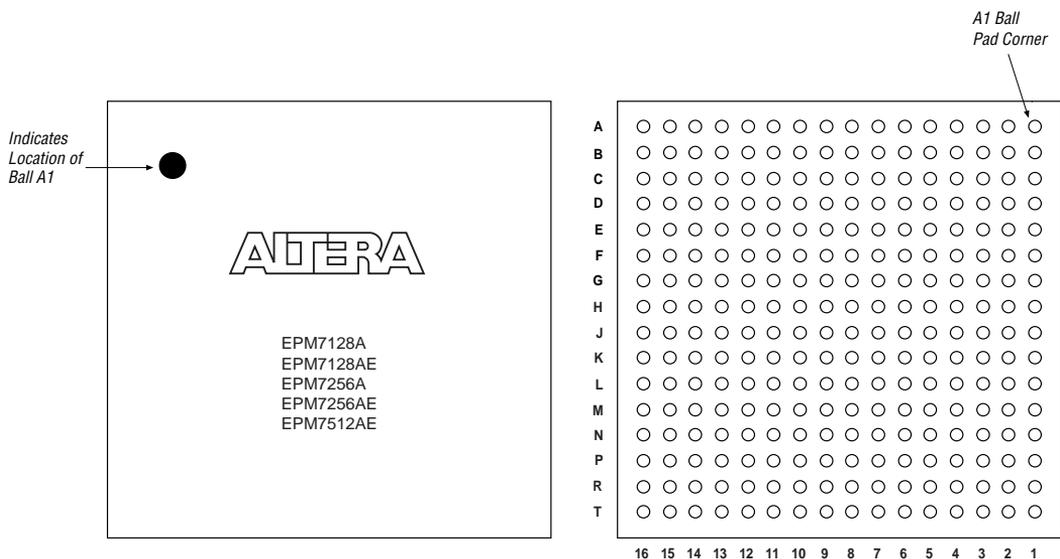
Revision History

The information contained in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5 supersedes information published in previous versions.

Version 4.5

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5:

■ Updated text in the "Power Sequencing & Hot-Socketing" section.

Version 4.4

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.4:

■ Added Tables 5 through 7.
■ Added "Programming Sequence" on page 17 and "Programming Times" on page 18.

Version 4.3

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.3:

■ Added extended temperature devices to document
■ Updated Table 14.

Version 4.2

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.2:

■ Removed *Note (1)* from Table 2.
■ Removed *Note (4)* from Tables 3 and 4.

Version 4.1

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.1:

■ Updated leakage current information in Table 15.
■ Updated *Note (9)* of Table 15.
■ Updated *Note (1)* of Tables 17 through 30.