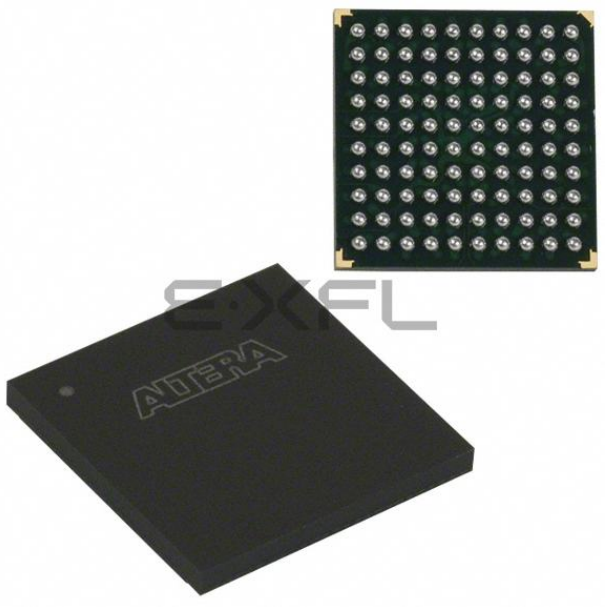

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	84
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LBGA
Supplier Device Package	100-FBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256aefi100-7n

Table 1. MAX 7000A Device Features

Feature	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
t_{PD} (ns)	4.5	4.5	5.0	5.5	7.5
t_{SU} (ns)	2.9	2.8	3.3	3.9	5.6
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3.0
t_{CO1} (ns)	3.0	3.1	3.4	3.5	4.7
f_{CNT} (MHz)	227.3	222.2	192.3	172.4	116.3

…and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt™ I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins

MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000A devices contain from 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms, providing up to 32 product terms per macrocell.

MAX 7000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5-V, 3.3-V, and 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems.

MAX 7000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

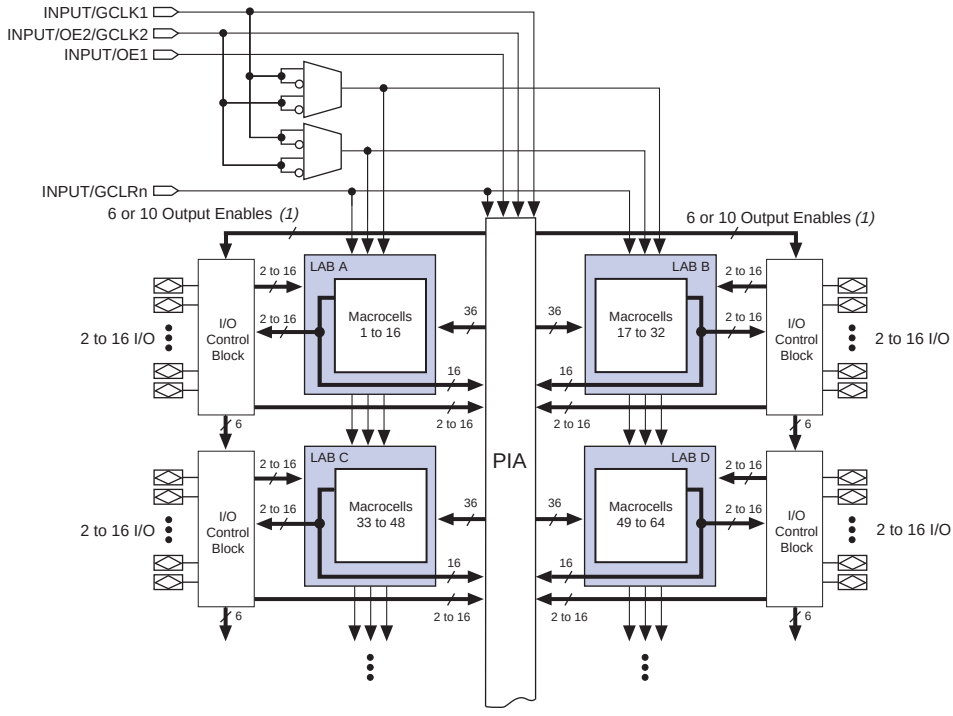
Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000A devices.

Figure 1. MAX 7000A Device Block Diagram



Note:

(1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables. EPM7512AE devices have 10 output enables.

Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Parallel Expanders

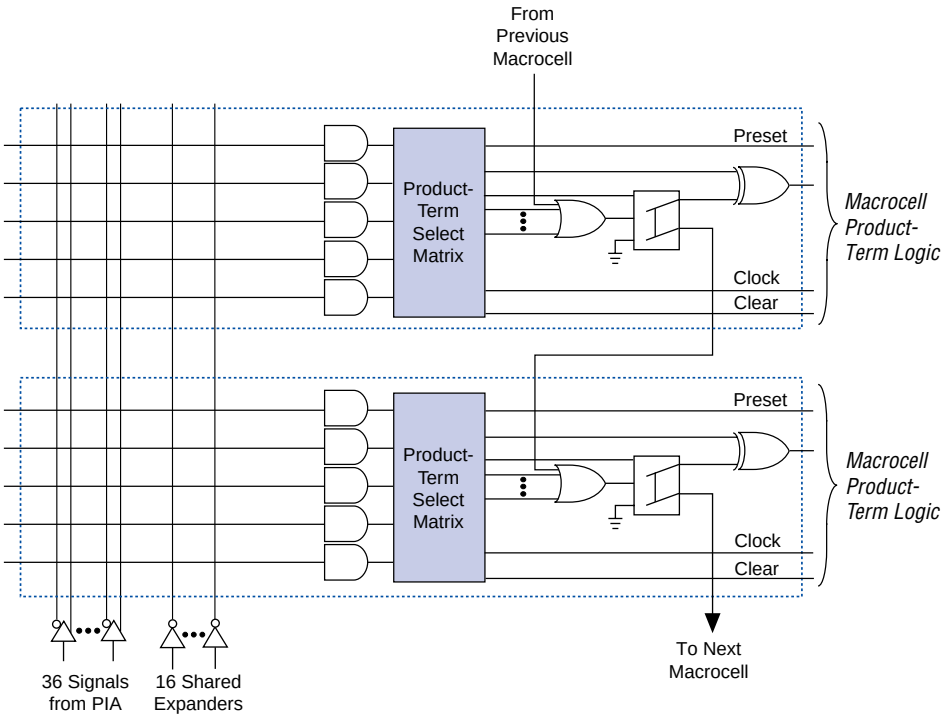
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders, and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 7000A Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

In-System Programmability

MAX 7000A devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 kΩ.

MAX 7000AE devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is only available in EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, and EPM7512AE devices.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster serial/USB communications cable, ByteBlasterMV parallel port download cable, and BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000AE devices can be programmed with either an adaptive or constant (non-adaptive) algorithm. EPM7128A and EPM7256A device can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD 71, can be used to program MAX 7000A devices with in-circuit testers, PCs, or embedded processors.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000A Device

The time required to program a single MAX 7000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Table 7. MAX 7000A Stand-Alone Verification Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032AE	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	s
EPM7064AE	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	s
EPM7128AE	0.01	0.02	0.04	0.07	0.14	0.34	0.68	1.36	s
EPM7256AE	0.02	0.03	0.08	0.15	0.30	0.75	1.49	2.98	s
EPM7512AE	0.03	0.06	0.15	0.30	0.60	1.49	2.97	5.94	s
EPM7128A *(1)*	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	s
EPM7256A *(1)*	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	s

Note to tables:

(1) EPM7128A and EPM7256A devices can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

Programming with External Hardware

MAX 7000A devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checks to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices.

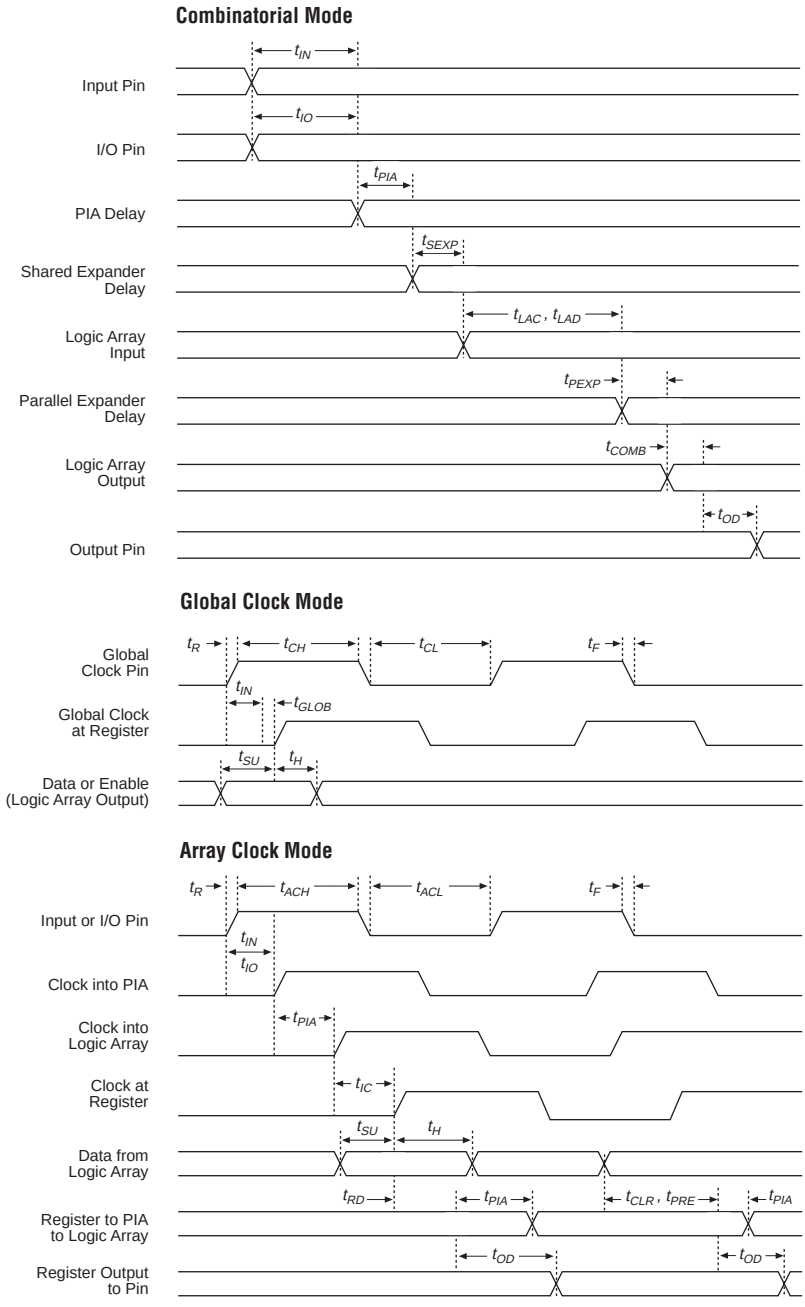
For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1. Table 8 describes the JTAG instructions supported by MAX 7000A devices. The pin-out tables, available from the Altera web site (**http://www.altera.com**), show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Figure 12. MAX 7000A Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Tables 17 through 30 show EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, EPM7512AE, EPM7128A, and EPM7256A timing information.

Table 17. EPM7032AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		4.5		7.5		10	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		4.5		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	2.9		4.7		6.3		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.6		2.5		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.3		0.5		0.5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.3	1.0	7.2	1.0	9.4	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		4.4		7.2		9.7	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	227.3		138.9		103.1		MHz
t_{ACNT}	Minimum array clock period	*(2)*		4.4		7.2		9.7	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	227.3		138.9		103.1		MHz

Table 20. EPM7064AE Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		1.1		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.6		1.1		1.4	ns
t_{FIN}	Fast input delay			2.5		3.0		3.7	ns
t_{SEXP}	Shared expander delay			1.8		3.0		3.9	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.5		2.5		3.2	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.9		ns
t_{H}	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.7		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.6		0.9		1.3	ns
t_{IC}	Array clock delay			1.2		1.9		2.5	ns

Table 25. EPM7512AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		7.5		10.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		7.5		10.0		12.0	ns
t_{SU}	Global clock setup time	*(2)*	5.6		7.6		9.1		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	4.7	1.0	6.3	1.0	7.5	ns
t_{CH}	Global clock high time		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time	*(2)*	2.5		3.5		4.1		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	7.8	1.0	10.4	1.0	12.5	ns
t_{ACH}	Array clock high time		3.0		4.0		5.0		ns
t_{ACL}	Array clock low time		3.0		4.0		5.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		4.0		5.0		ns
t_{CNT}	Minimum global clock period	*(2)*		8.6		11.5		13.9	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	116.3		87.0		71.9		MHz
t_{ACNT}	Minimum array clock period	*(2)*		8.6		11.5		13.9	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	116.3		87.0		71.9		MHz

Table 28. EPM7128A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		0.7		0.9		1.1	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.7		0.9		1.1	ns
t_{FIN}	Fast input delay			2.7		3.1		3.6		3.9	ns
t_{SEXP}	Shared expander delay			2.5		3.2		4.3		5.1	ns
t_{PEXP}	Parallel expander delay			0.7		0.8		1.1		1.3	ns
t_{LAD}	Logic array delay			2.4		3.0		4.1		4.9	ns
t_{LAC}	Logic control array delay			2.4		3.0		4.1		4.9	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.4		0.6		0.7		0.9	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		0.9		1.1		1.2		1.4	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.4		5.6		5.7		5.9	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		4.5		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		9.0		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		5.0	ns
t_{SU}	Register setup time		1.9		2.4		3.1		3.8		ns
t_{H}	Register hold time		1.5		2.2		3.3		4.3		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.7		1.9		1.9		1.9		ns

Table 28. EPM7128A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{RD}	Register delay			1.7		2.1		2.8		3.3	ns
t_{COMB}	Combinatorial delay			1.7		2.1		2.8		3.3	ns
t_{IC}	Array clock delay			2.4		3.0		4.1		4.9	ns
t_{EN}	Register enable time			2.4		3.0		4.1		4.9	ns
t_{GLOB}	Global control delay			1.0		1.2		1.7		2.0	ns
t_{PRE}	Register preset time			3.1		3.9		5.2		6.2	ns
t_{CLR}	Register clear time			3.1		3.9		5.2		6.2	ns
t_{PIA}	PIA delay	*(2)*		0.9		1.1		1.5		1.8	ns
t_{LPA}	Low-power adder	*(6)*		11.0		10.0		10.0		10.0	ns

Table 29. EPM7256A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		6.0		7.5		10.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		6.0		7.5		10.0		12.0	ns
t_{SU}	Global clock setup time	*(2)*	3.7		4.6		6.2		7.4		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	4.2	1.0	5.5	1.0	6.6	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		4.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	0.8		1.0		1.4		1.6		ns
t_{AH}	Array clock hold time	*(2)*	1.9		2.7		4.0		5.1		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	6.2	1.0	7.8	1.0	10.3	1.0	12.4	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		4.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		3.0		4.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		6.4		8.0		10.7		12.8	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	156.3		125.0		93.5		78.1		MHz
t_{ACNT}	Minimum array clock period	*(2)*		6.4		8.0		10.7		12.8	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	156.3		125.0		93.5		78.1		MHz

Figure 15. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outlines not drawn to scale.

Figure 16. 84-Pin PLCC Package Pin-Out Diagram

Package outline not drawn to scale.

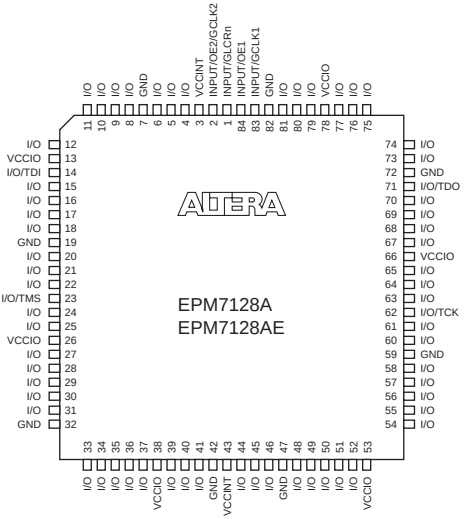


Figure 17. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

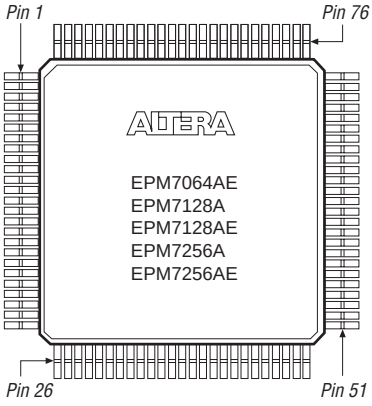


Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

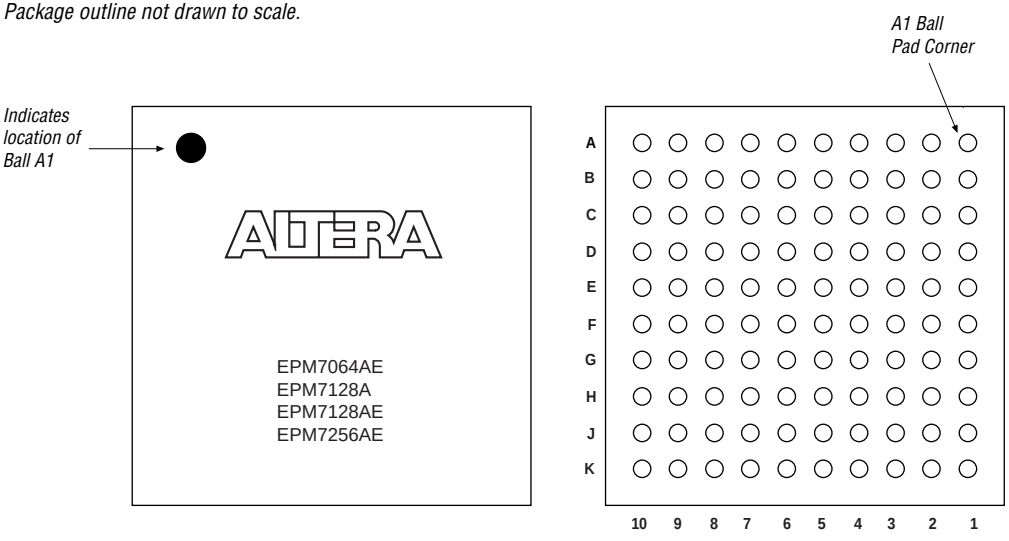


Figure 19. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

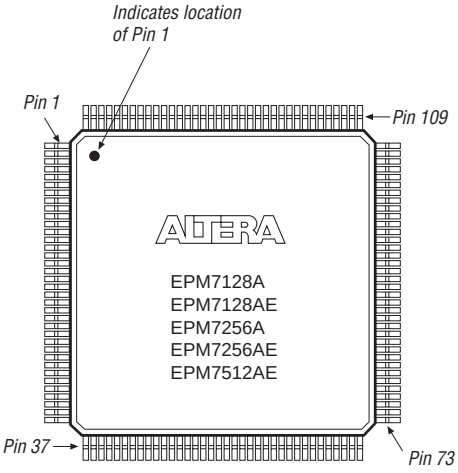


Figure 20. 169-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

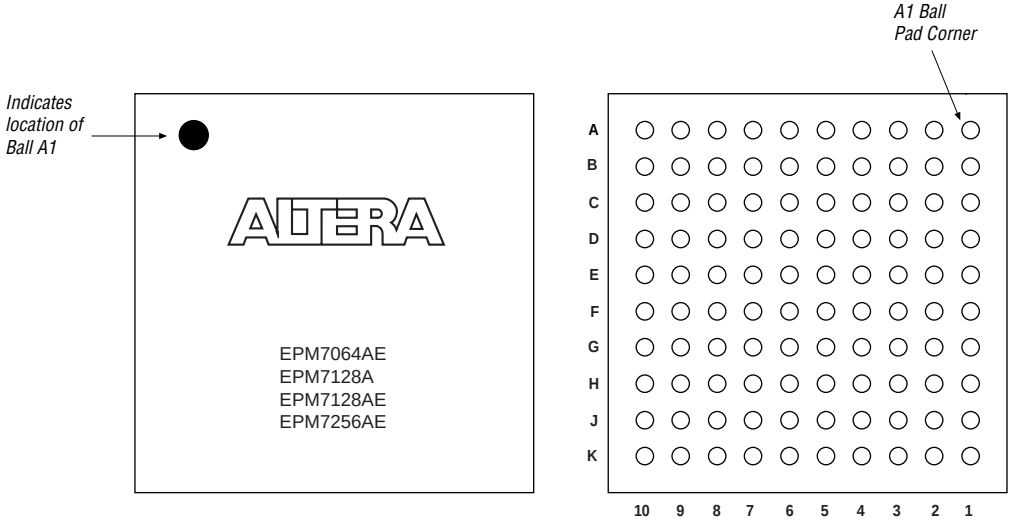


Figure 22. 256-Pin BGA Package Pin-Out Diagram

Package outline not drawn to scale.