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Intel - EPM7256AETC100-5 Datasheet



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Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256aetc100-5

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- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlasterTM serial/universal serial bus (USB) communications cable, ByteBlasterMVTM parallel port download cable, and BitBlasterTM serial download cable, as well as programming hardware from third-party manufacturers and any JamTM STAPL File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File- (.svf) capable in-circuit tester

General Description

MAX 7000A (including MAX 7000AE) devices are high-density, highperformance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROMbased MAX 7000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 7000A devices in the -4, -5, -6, -7, and some -10 speed grades are compatible with the timing requirements for 33 MHz operation of the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See Table 2.

Table 2. MAX 7000A Speed Grades										
Device		Speed Grade								
	-4	-5	-6	-7	-10	-12				
EPM7032AE	~			~	~					
EPM7064AE	\checkmark			\checkmark	~					
EPM7128A			 Image: A set of the set of the	~	~	~				
EPM7128AE		~		~	~					
EPM7256A			\checkmark	\checkmark	\checkmark	\checkmark				
EPM7256AE		\checkmark		\checkmark	\checkmark					
EPM7512AE				\checkmark	\checkmark	 Image: A start of the start of				

The MAX 7000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices including PALs, GALs, and 22V10s devices. MAX 7000A devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, Ultra FineLine BGA, PQFP, and TQFP packages. See Table 3 and Table 4.

Table 3. MAX 700	OA Maximum U	lser I/O Pins	Note (1)			
Device	44-Pin PLCC	44-Pin TQFP	49-Pin Ultra FineLine BGA (2)	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine BGA (3)
EPM7032AE	36	36				
EPM7064AE	36	36	41		68	68
EPM7128A				68	84	84
EPM7128AE				68	84	84
EPM7256A					84	
EPM7256AE					84	84
EPM7512AE						

Table 4. MAX 7000A Maximum User I/O Pins Note (1)									
Device144-Pin TQFP169-Pin Ultra FineLine BGA (2)208-Pin PQFP256-Pin BGA256-FineLine BGA									
EPM7032AE									
EPM7064AE									
EPM7128A	100				100				
EPM7128AE	100	100			100				
EPM7256A	120		164		164				
EPM7256AE	120		164		164				
EPM7512AE	120		176	212	212				

Notes to tables:

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.
- (2) All Ultra FineLine BGA packages are footprint-compatible via the SameFrameTM feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.
- (3) All FineLine BGA packages are footprint-compatible via the SameFrame feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.

Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000A devices.



Figure 1. MAX 7000A Device Block Diagram

Note:

(1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables. EPM7512AE devices have 10 output enables.

Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- **3**6 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Macrocells

MAX 7000A macrocells can be individually configured for either sequential or combinatorial logic operation. The macrocells consist of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows a MAX 7000A macrocell.



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

Figure 5. MAX 7000A PIA Routing



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC} . Figure 6 shows the I/O control block for MAX 7000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.



For more information on using the Jam STAPL language, see *Application Note 88* (Using the Jam Language for ISP & ICR via an Embedded Processor) and *Application Note 122* (Using Jam STAPL for ISP & ICR via an Embedded *Processor*).

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

- 1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
- 2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
- 3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
- 4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
- 5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
- 6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000A Device

The time required to program a single MAX 7000A device in-system can be calculated from the following formula:

$t_{PROG} = t_{PPULSE} +$	Cycle _{PTCK} f _{TCK}
where: t_{PROG}	= Programming time
t _{PPULSE}	= Sum of the fixed times to erase, program, and verify the EEPROM cells
<i>Cycle_{PTCK}</i>	= Number of TCK cycles to program a device
f _{TCK}	= TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000A device can be calculated from the following formula:

$t_{VER} = t_{VPULSE} + \frac{C_1}{2}$	f _{TCK}
where: t_{VER} t_{VPULSE} $Cycle_{VTCK}$	= Verify time= Sum of the fixed times to verify the EEPROM cells= Number of TCK cycles to verify a device

The programming times described in Tables 5 through 7 are associated with the worst-case method using the enhanced ISP algorithm.

Table 5. MAX 7000A t _{PULSE} & Cycle _{TCK} Values									
Device	Device Programming Stand-Alone Verifica								
	<i>t_{PPULSE}</i> (s)	Cycle _{PTCK}	t _{VPULSE} (s)	Cycle _{VTCK}					
EPM7032AE	2.00	55,000	0.002	18,000					
EPM7064AE	2.00	105,000	0.002	35,000					
EPM7128AE	2.00	205,000	0.002	68,000					
EPM7256AE	2.00	447,000	0.002	149,000					
EPM7512AE	2.00	890,000	0.002	297,000					
EPM7128A (1)	5.11	832,000	0.03	528,000					
EPM7256A (1)	6.43	1,603,000	0.03	1,024,000					

Tables 6 and 7 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 6. MAX 7000A In-System Programming Times for Different Test Clock Frequencies											
Device		f _{тск}									
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz			
EPM7032AE	2.01	2.01	2.03	2.06	2.11	2.28	2.55	3.10	S		
EPM7064AE	2.01	2.02	2.05	2.11	2.21	2.53	3.05	4.10	S		
EPM7128AE	2.02	2.04	2.10	2.21	2.41	3.03	4.05	6.10	S		
EPM7256AE	2.05	2.09	2.23	2.45	2.90	4.24	6.47	10.94	S		
EPM7512AE	2.09	2.18	2.45	2.89	3.78	6.45	10.90	19.80	S		
EPM7128A (1)	5.19	5.27	5.52	5.94	6.77	9.27	13.43	21.75	S		
EPM7256A (1)	6.59	6.75	7.23	8.03	9.64	14.45	22.46	38.49	S		

Table 7. MAX 7000A Stand-Alone Verification Times for Different Test Clock Frequencies										
Device		f _{TCK}								
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz		
EPM7032AE	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	S	
EPM7064AE	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	S	
EPM7128AE	0.01	0.02	0.04	0.07	0.14	0.34	0.68	1.36	S	
EPM7256AE	0.02	0.03	0.08	0.15	0.30	0.75	1.49	2.98	S	
EPM7512AE	0.03	0.06	0.15	0.30	0.60	1.49	2.97	5.94	S	
EPM7128A (1)	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	S	
EPM7256A (1)	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	S	

Note to tables:

(1) EPM7128A and EPM7256A devices can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

Programming with External Hardware

MAX 7000A devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checks to ensure adequate electrical contact between the adapter and the device.



For more information, see the Altera Programming Hardware Data Sheet.

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices.



For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) **Boundary-Scan** Support

MAX 7000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1. Table 8 describes the JTAG instructions supported by MAX 7000A devices. The pin-out tables, available from the Altera web site (http://www.altera.com), show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

VCC

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Figure 9. MAX 7000A AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests 703 Ω [521 Ω] *≶* must not be performed under AC conditions. Large-amplitude, fast-ground-Device Output current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between 586 Ω [481 Ω] *≥* the device ground pin and the test system ground, significant reductions in Device input observable noise immunity can result. rise and fall Numbers in brackets are for 2.5-V times < 2 ns outputs. Numbers without brackets are for 3.3-V outputs.

Operating Conditions

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000A devices.

Table 1	Table 13. MAX 7000A Device Absolute Maximum RatingsNote (1)										
Symbol	Parameter	Conditions	Min	Max	Unit						
V _{CC}	Supply voltage	With respect to ground (2)	-0.5	4.6	V						
VI	DC input voltage		-2.0	5.75	V						
I _{OUT}	DC output current, per pin		-25	25	mA						
T _{STG}	Storage temperature	No bias	-65	150	°C						
T _A	Ambient temperature	Under bias	-65	135	°C						
TJ	Junction temperature	BGA, FineLine BGA, PQFP, and TQFP packages, under bias		135	°C						

Tables 17 through 30 show EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, EPM7512AE, EPM7128A, and EPM7256A timing information.

Table 1	Table 17. EPM7032AE External Timing Parameters								
Symbol	Parameter	Conditions		Speed Grade					
			-	4	-	7	-1	0	
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t _{SU}	Global clock setup time	(2)	2.9		4.7		6.3		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.6		2.5		3.6		ns
t _{AH}	Array clock hold time	(2)	0.3		0.5		0.5		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.4	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		4.4		7.2		9.7	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	227.3		138.9		103.1		MHz
t _{ACNT}	Minimum array clock period	(2)		4.4		7.2		9.7	ns
facnt	Maximum internal array clock frequency	(2), (4)	227.3		138.9		103.1		MHz

Table 1	Table 19. EPM7064AE External Timing Parameters Note (1)										
Symbol	Parameter	Conditions	Speed Grade								
				4	-	7	-1	0			
			Min	Max	Min	Max	Min	Max			
t _{PD1}	Input to non- registered output	C1 = 35 pF (2)		4.5		7.5		10.0	ns		
t _{PD2}	I/O input to non- registered output	C1 = 35 pF (2)		4.5		7.5		10.0	ns		
t _{SU}	Global clock setup time	(2)	2.8		4.7		6.2		ns		
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns		
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns		
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns		
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.1	1.0	5.1	1.0	7.0	ns		
t _{CH}	Global clock high time		2.0		3.0		4.0		ns		
t _{CL}	Global clock low time		2.0		3.0		4.0		ns		
t _{ASU}	Array clock setup time	(2)	1.6		2.6		3.6		ns		
t _{AH}	Array clock hold time	(2)	0.3		0.4		0.6		ns		
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.6	ns		
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns		
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns		
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns		
t _{CNT}	Minimum global clock period	(2)		4.5		7.4		10.0	ns		
f _{CNT}	Maximum internal global clock frequency	(2), (4)	222.2		135.1		100.0		MHz		
t _{acnt}	Minimum array clock period	(2)		4.5		7.4		10.0	ns		
f _{acnt}	Maximum internal array clock frequency	(2), (4)	222.2		135.1		100.0		MHz		

Symbol	Parameter	Conditions			Speed	Grade			Unit
			-	4		7	-	10	
			Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.6		1.1		1.4	ns
t _{IO}	I/O input pad and buffer delay			0.6		1.1		1.4	ns
t _{FIN}	Fast input delay			2.5		3.0		3.7	ns
t _{SEXP}	Shared expander delay			1.8		3.0		3.9	ns
t _{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t _{LAD}	Logic array delay			1.5		2.5		3.2	ns
t _{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t _{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t _{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		0.8		1.3		1.8	ns
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		1.3		1.8		2.3	ns
t _{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		5.8		6.3		6.8	ns
t _{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		4.0		5.0	ns
t _{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		4.5		5.5	ns
t _{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3 V$	C1 = 35 pF		9.0		9.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t _{SU}	Register setup time		1.3		2.0		2.9		ns
t _H	Register hold time		0.6		1.0		1.3		ns
t _{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t _{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t _{RD}	Register delay			0.7		1.2		1.6	ns
t _{COMB}	Combinatorial delay			0.6		0.9		1.3	ns
t _{IC}	Array clock delay			1.2		1.9		2.5	ns

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Symbol	Parameter	Conditions				Speed	Grade				Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		6.0		7.5		10.0		12.0	ns
t _{PD2}	I/O input to non- registered output	C1 = 35 pF (2)		6.0		7.5		10.0		12.0	ns
t _{SU}	Global clock setup time	(2)	4.2		5.3		7.0		8.5		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.7	1.0	4.6	1.0	6.1	1.0	7.3	ns
t _{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t _{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t _{ASU}	Array clock setup time	(2)	1.9		2.4		3.1		3.8		ns
t _{AH}	Array clock hold time	(2)	1.5		2.2		3.3		4.3		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	6.0	1.0	7.5	1.0	10.0	1.0	12.0	ns
t _{ACH}	Array clock high time		3.0		3.0		4.0		5.0		ns
t _{ACL}	Array clock low time		3.0		3.0		4.0		5.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		3.0		4.0		5.0		ns
t _{CNT}	Minimum global clock period	(2)		6.9		8.6		11.5		13.8	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	144.9		116.3		87.0		72.5		MHz
t _{acnt}	Minimum array clock period	(2)		6.9		8.6		11.5		13.8	ns
f _{acnt}	Maximum internal array clock frequency	(2), (4)	144.9		116.3		87		72.5		MHz

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Table 28. EPM7128A Internal Timing Parameters (Part 1 of 2)Note (1)												
Symbol	Parameter	Conditions				Speed	Grade				Unit	
			-	6	-	7	-10		-12		1	
			Min	Max	Min	Max	Min	Мах	Min	Max		
t _{IN}	Input pad and buffer delay			0.6		0.7		0.9		1.1	ns	
t _{IO}	I/O input pad and buffer delay			0.6		0.7		0.9		1.1	ns	
t _{FIN}	Fast input delay			2.7		3.1		3.6		3.9	ns	
t _{SEXP}	Shared expander delay			2.5		3.2		4.3		5.1	ns	
t _{PEXP}	Parallel expander delay			0.7		0.8		1.1		1.3	ns	
t _{LAD}	Logic array delay			2.4		3.0		4.1		4.9	ns	
t _{LAC}	Logic control array delay			2.4		3.0		4.1		4.9	ns	
t _{IOE}	Internal output enable delay			0.0		0.0		0.0		0.0	ns	
t _{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.4		0.6		0.7		0.9	ns	
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		0.9		1.1		1.2		1.4	ns	
t _{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5$ V or 3.3 V	C1 = 35 pF		5.4		5.6		5.7		5.9	ns	
t _{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 \text{ V}$	C1 = 35 pF		4.0		4.0		5.0		5.0	ns	
t _{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		4.5		5.5		5.5	ns	
t _{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3 V$	C1 = 35 pF		9.0		9.0		10.0		10.0	ns	
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		5.0	ns	
t _{SU}	Register setup time		1.9		2.4		3.1		3.8		ns	
t _H	Register hold time		1.5		2.2		3.3		4.3		ns	
t _{FSU}	Register setup time of fast input		0.8		1.1		1.1		1.1		ns	
t _{FH}	Register hold time of fast input		1.7		1.9		1.9		1.9		ns	

Symbol	Parameter	Conditions				Speed	Grade				Unit
			-6		-7		-10		-12		1
			Min	Мах	Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.3		0.4		0.5		0.6	ns
t _{IO}	I/O input pad and buffer delay			0.3		0.4		0.5		0.6	ns
t _{FIN}	Fast input delay			2.4		3.0		3.4		3.8	ns
t _{SEXP}	Shared expander delay			2.8		3.5		4.7		5.6	ns
t _{PEXP}	Parallel expander delay			0.5		0.6		0.8		1.0	ns
t _{LAD}	Logic array delay			2.5		3.1		4.2		5.0	ns
t _{LAC}	Logic control array delay			2.5		3.1		4.2		5.0	ns
t _{IOE}	Internal output enable delay			0.2		0.3		0.4		0.5	ns
t _{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 \text{ V}$	C1 = 35 pF		0.3		0.4		0.5		0.6	ns
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		0.8		0.9		1.0		1.1	ns
t _{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.3		5.4		5.5		5.6	ns
t _{ZX1}	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		4.0		5.0		5.0	ns
t _{ZX2}	Output buffer enable delay slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		4.5		5.5		5.5	ns
t _{ZX3}	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5$ V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		5.0	ns
t _{SU}	Register setup time		1.0		1.3		1.7		2.0		ns
t _H	Register hold time		1.7		2.4		3.7		4.7		ns
t _{FSU}	Register setup time of fast input		1.2		1.4		1.4		1.4		ns
t _{FH}	Register hold time of fast input		1.3		1.6		1.6		1.6		ns
t _{RD}	Register delay			1.6		2.0		2.7		3.2	ns

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Symbol	Parameter	Conditions				Speed	Grade				Unit	
			-	-6 -7		-1	-10		12			
			Min	Max	Min	Max	Min	Max	Min	Max		
t _{COMB}	Combinatorial delay			1.6		2.0		2.7		3.2	ns	
t _{IC}	Array clock delay			2.7		3.4		4.5		5.4	ns	
t _{EN}	Register enable time			2.5		3.1		4.2		5.0	ns	
t _{GLOB}	Global control delay			1.1		1.4		1.8		2.2	ns	
t _{PRE}	Register preset time			2.3		2.9		3.8		4.6	ns	
t _{CLR}	Register clear time			2.3		2.9		3.8		4.6	ns	
t _{PIA}	PIA delay	(2)		1.3		1.6		2.1		2.6	ns	
t _{LPA}	Low-power adder	(6)		11.0		10.0		10.0		10.0	ns	

Table 30. EPM7256A Internal Timing Parameters (Part 2 of 2) Note (1)

Notes to tables:

 These values are specified under the recommended operating conditions shown in Table 14 on page 28. See Figure 12 for more information on switching waveforms.

- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (4) This parameter is measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) Operating conditions: $V_{CCIO} = 2.5 \pm 0.2$ V for commercial and industrial use.
- (6) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency (f_{MAX} , in MHz) for MAX 7000A devices is calculated with the following equation:

 $P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note* 74 (*Evaluating Power for Altera Devices*).

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

I_{CCINT} =

 $(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times tog_{LC})$

Figure 13 shows the typical supply current versus frequency for MAX 7000A devices.





EPM7128A & EPM7128AE



Figure 21. 208-Pin PQFP Package Pin-Out Diagram

Package outline not drawn to scale.

