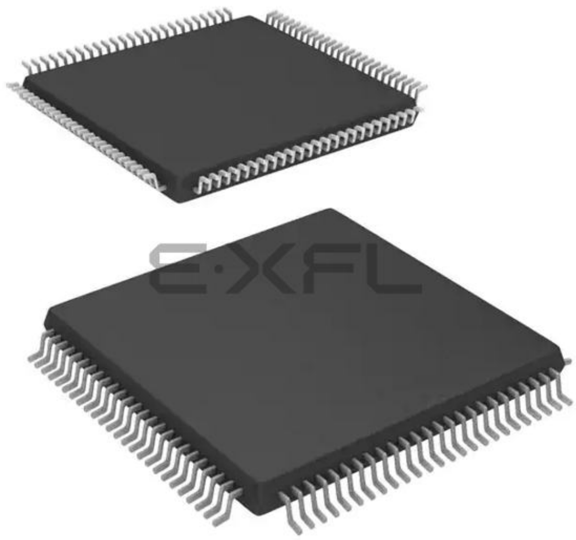
Intel - EPM7256AETC100-5N Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256aetc100-5n

Table 1. MAX 7000A Device Features

Feature	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
t_{PD} (ns)	4.5	4.5	5.0	5.5	7.5
t_{SU} (ns)	2.9	2.8	3.3	3.9	5.6
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3.0
t_{CO1} (ns)	3.0	3.1	3.4	3.5	4.7
f_{CNT} (MHz)	227.3	222.2	192.3	172.4	116.3

...and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt™ I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins

- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, ByteBlasterMV™ parallel port download cable, and BitBlaster™ serial download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File- (**.svf**) capable in-circuit tester

General Description

MAX 7000A (including MAX 7000AE) devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 7000A devices in the -4, -5, -6, -7, and some -10 speed grades are compatible with the timing requirements for 33 MHz operation of the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***. See Table 2.

Table 2. MAX 7000A Speed Grades

Device	Speed Grade					
	-4	-5	-6	-7	-10	-12
EPM7032AE	✓			✓	✓	
EPM7064AE	✓			✓	✓	
EPM7128A			✓	✓	✓	✓
EPM7128AE		✓		✓	✓	
EPM7256A			✓	✓	✓	✓
EPM7256AE		✓		✓	✓	
EPM7512AE				✓	✓	✓

The MAX 7000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices including PALs, GALs, and 22V10s devices. MAX 7000A devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, Ultra FineLine BGA, PQFP, and TQFP packages. See Table 3 and Table 4.

Table 3. MAX 7000A Maximum User I/O Pins *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	49-Pin Ultra FineLine BGA *(2)*	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine BGA *(3)*
EPM7032AE	36	36				
EPM7064AE	36	36	41		68	68
EPM7128A				68	84	84
EPM7128AE				68	84	84
EPM7256A					84	
EPM7256AE					84	84
EPM7512AE						

Table 4. MAX 7000A Maximum User I/O Pins *Note (1)*

Device	144-Pin TQFP	169-Pin Ultra FineLine BGA *(2)*	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA *(3)*
EPM7032AE					
EPM7064AE					
EPM7128A	100				100
EPM7128AE	100	100			100
EPM7256A	120		164		164
EPM7256AE	120		164		164
EPM7512AE	120		176	212	212

Notes to tables:

(1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

(2) All Ultra FineLine BGA packages are footprint-compatible via the SameFrame™ feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.

(3) All FineLine BGA packages are footprint-compatible via the SameFrame feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 15 for more details.

MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000A devices contain from 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms, providing up to 32 product terms per macrocell.

MAX 7000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5-V, 3.3-V, and 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems.

MAX 7000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000A devices.

Parallel Expanders

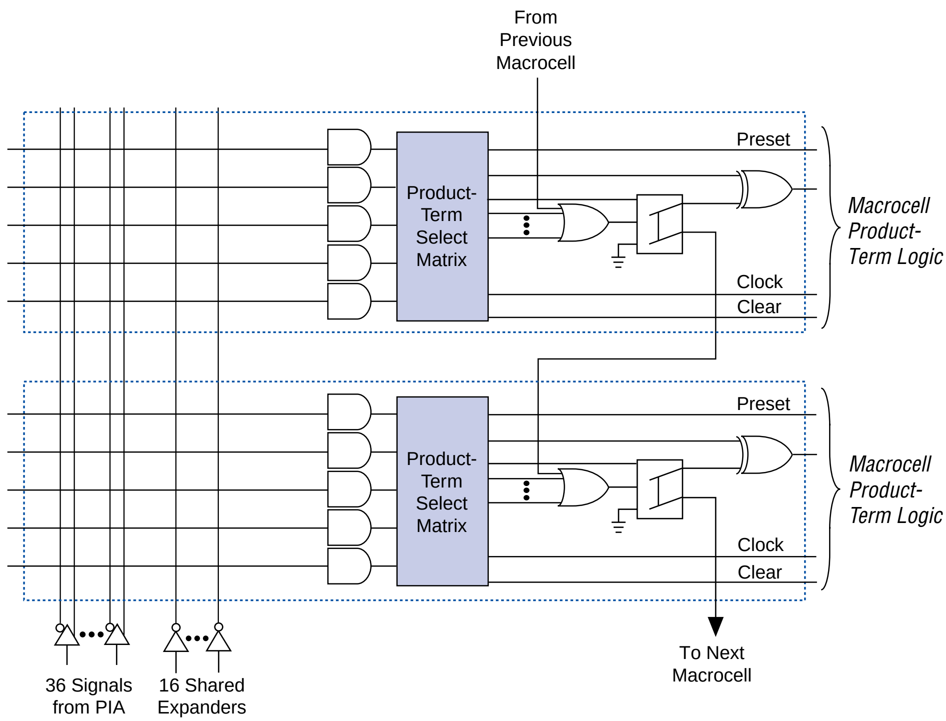
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders, and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 7000A Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

In-System Programmability

MAX 7000A devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 kΩ.

MAX 7000AE devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is only available in EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, and EPM7512AE devices.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster serial/USB communications cable, ByteBlasterMV parallel port download cable, and BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000AE devices can be programmed with either an adaptive or constant (non-adaptive) algorithm. EPM7128A and EPM7256A device can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD 71, can be used to program MAX 7000A devices with in-circuit testers, PCs, or embedded processors.

Table 8. MAX 7000A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the `TDI` and `TDO` pins, allowing the IDCODE to be serially shifted out of `TDO`
USERCODE	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE value to be shifted out of `TDO`. The USERCODE instruction is available for MAX 7000AE devices only
UESCODE	These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be shifted out of `TDO`. UESCODE instructions are available for EPM7128A and EPM7256A devices only.
ISP Instructions	These instructions are used when programming MAX 7000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam STAPL File, JBC File, or SVF File via an embedded processor or test equipment.

Open-Drain Output Option

MAX 7000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Open-drain output pins on MAX 7000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high V_{IH}. When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V to meet CMOS V_{OH} requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Programmable Ground Pins

Each unused I/O pin on MAX 7000A devices may be used as an additional ground pin. In EPM7128A and EPM7256A devices, utilizing unused I/O pins as additional ground pins requires using the associated macrocell. In MAX 7000AE devices, this programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Table 14. MAX 7000A Device Recommended Operating Conditions					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(13)*	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation	*(3)*	3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation	*(3)*	2.3	2.7	V
V_{CCISP}	Supply voltage during in-system programming		3.0	3.6	V
V_I	Input voltage	*(4)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	Commercial range	0	70	° C
		Industrial range *(5)*	–40	85	° C
T_J	Junction temperature	Commercial range	0	90	° C
		Industrial range *(5)*	–40	105	° C
		Extended range *(5)*	–40	130	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) For EPM7128A and EPM7256A devices only, V_{CC} must rise monotonically.

(4) In MAX 7000AE devices, all pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(5) These devices support in-system programming for –40° to 100° C. For in-system programming support between –40° and 0° C, contact Altera Applications.

(6) These values are specified under the recommended operating conditions shown in Table 14 on page 28.

(7) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.

(8) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.

(9) This value is specified for normal device operation. For MAX 7000AE devices, the maximum leakage current during power-up is ±300 µA. For EPM7128A and EPM7256A devices, leakage current during power-up is not specified.

(10) For EPM7128A and EPM7256A devices, this pull-up exists while a device is programmed in-system.

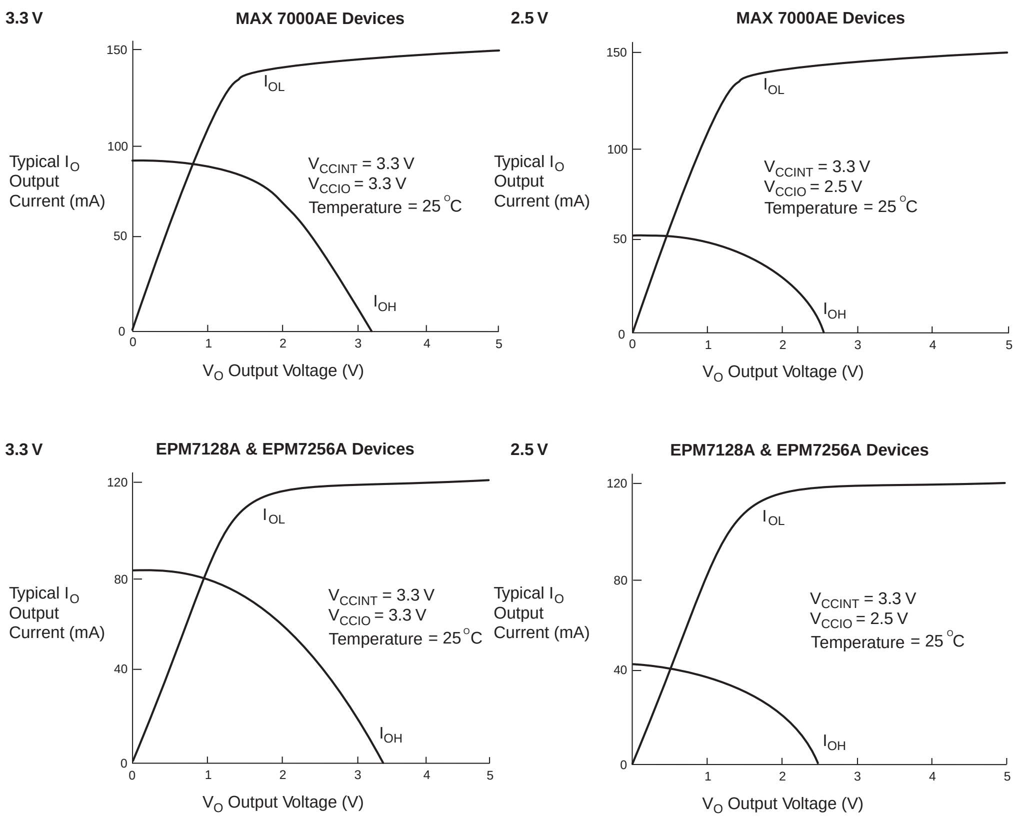
(11) For MAX 7000AE devices, this pull-up exists while devices are programmed in-system and in unprogrammed devices during power-up.

(12) Capacitance is measured at 25 °C and is sample-tested only. The `OE1` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

(13) The POR time for MAX 7000AE devices (except MAX 7128A and MAX 7256A devices) does not exceed 100 µs. The sufficient V_{CCINT} voltage level for POR is 3.0 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.

Figure 10 shows the typical output drive characteristics of MAX 7000A devices.

Figure 10. Output Drive Characteristics of MAX 7000A Devices



Timing Model

MAX 7000A device timing can be analyzed with the Altera software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 11. MAX 7000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Table 18. EPM7032AE Internal Timing Parameters (Part 1 of 2) *Note (1)*

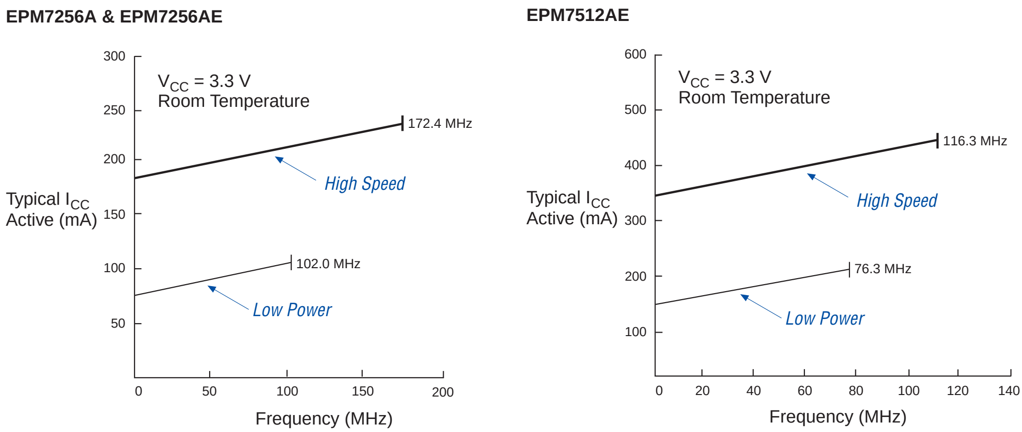
Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		1.2		1.5	ns
t_{IO}	I/O input pad and buffer delay			0.7		1.2		1.5	ns
t_{FIN}	Fast input delay			2.3		2.8		3.4	ns
t_{SEXP}	Shared expander delay			1.9		3.1		4.0	ns
t_{PEXP}	Parallel expander delay			0.5		0.8		1.0	ns
t_{LAD}	Logic array delay			1.5		2.5		3.3	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.8		ns
t_{H}	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.7		1.2		1.5	ns
t_{COMB}	Combinatorial delay			0.6		1.0		1.3	ns

Table 23. EPM7256AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		5.5		7.5		10	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		5.5		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	3.9		5.2		6.9		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.5	1.0	4.8	1.0	6.4	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	2.0		2.7		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	5.4	1.0	7.3	1.0	9.7	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		5.8		7.9		10.5	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	172.4		126.6		95.2		MHz
t_{ACNT}	Minimum array clock period	*(2)*		5.8		7.9		10.5	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	172.4		126.6		95.2		MHz

Table 28. EPM7128A Internal Timing Parameters (Part 1 of 2) Note (1)											
Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		0.7		0.9		1.1	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.7		0.9		1.1	ns
t_{FIN}	Fast input delay			2.7		3.1		3.6		3.9	ns
t_{SEXP}	Shared expander delay			2.5		3.2		4.3		5.1	ns
t_{PEXP}	Parallel expander delay			0.7		0.8		1.1		1.3	ns
t_{LAD}	Logic array delay			2.4		3.0		4.1		4.9	ns
t_{LAC}	Logic control array delay			2.4		3.0		4.1		4.9	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.4		0.6		0.7		0.9	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		0.9		1.1		1.2		1.4	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.4		5.6		5.7		5.9	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF *(5)*		4.5		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		9.0		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		5.0	ns
t_{SU}	Register setup time		1.9		2.4		3.1		3.8		ns
t_H	Register hold time		1.5		2.2		3.3		4.3		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.7		1.9		1.9		1.9		ns

Figure 13. I_{CC} vs. Frequency for MAX 7000A Devices (Part 2 of 2)



Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the ***Altera Digital Library*** for pin-out information.

Figures 14 through 23 show the package pin-out diagrams for MAX 7000A devices.

Figure 14. 44-Pin PLCC/TQFP Package Pin-Out Diagram

Package outlines not drawn to scale.

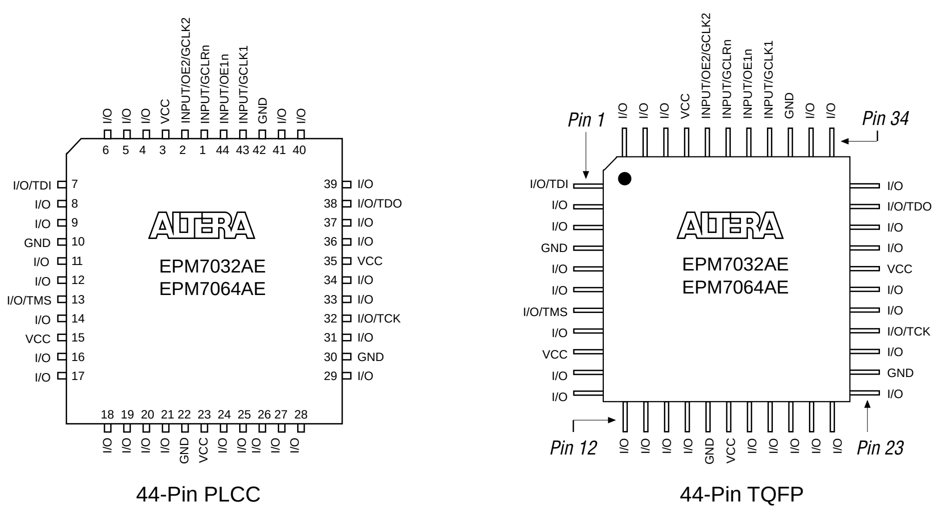


Figure 15. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outlines not drawn to scale.

Figure 16. 84-Pin PLCC Package Pin-Out Diagram

Package outline not drawn to scale.

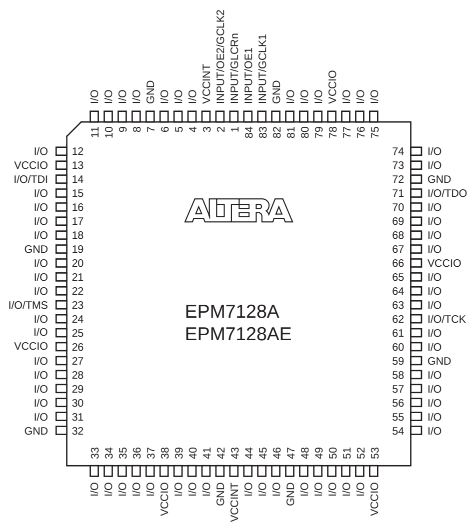


Figure 22. 256-Pin BGA Package Pin-Out Diagram

Package outline not drawn to scale.

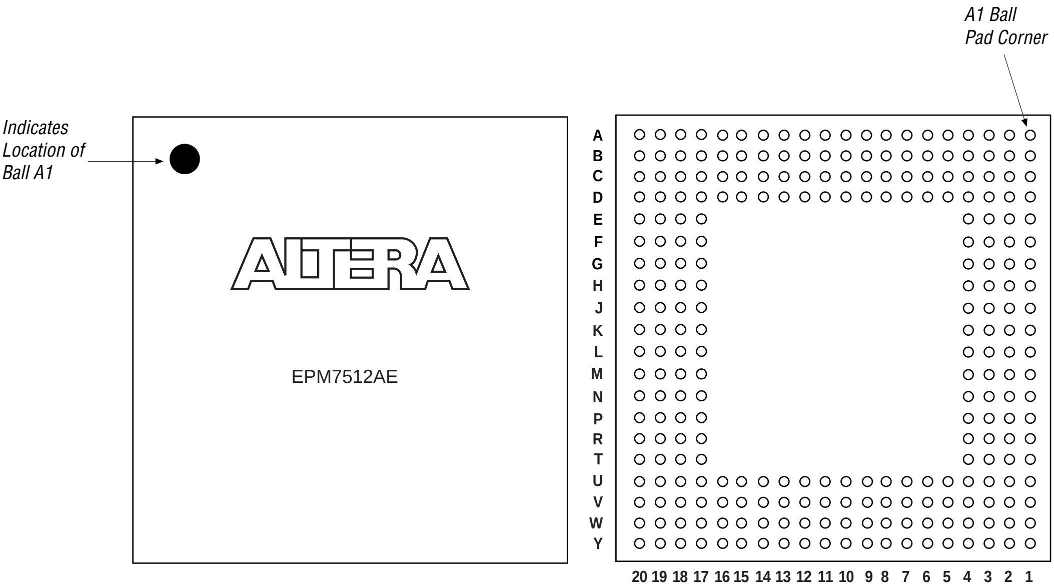


Figure 23. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

Revision History

The information contained in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5 supersedes information published in previous versions.

Version 4.5

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5:

- Updated text in the "Power Sequencing & Hot-Socketing" section.

Version 4.4

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.4:

- Added Tables 5 through 7.
- Added "Programming Sequence" on page 17 and "Programming Times" on page 18.