



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

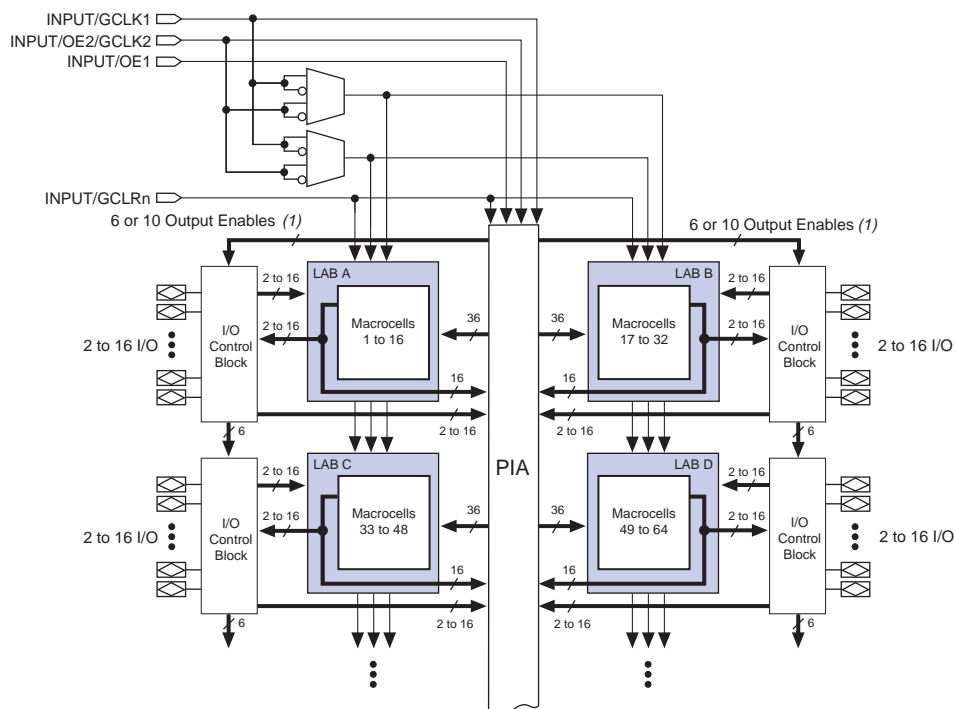
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7256aetc100-7">https://www.e-xfl.com/product-detail/intel/epm7256aetc100-7</a>

**Table 1. MAX 7000A Device Features**

Feature	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
$t_{PD}$ (ns)	4.5	4.5	5.0	5.5	7.5
$t_{SU}$ (ns)	2.9	2.8	3.3	3.9	5.6
$t_{FSU}$ (ns)	2.5	2.5	2.5	2.5	3.0
$t_{CO1}$ (ns)	3.0	3.1	3.4	3.5	4.7
$f_{CNT}$ (MHz)	227.3	222.2	192.3	172.4	116.3

## ...and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt™ I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins



(1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables. EPM7512AE devices have 10 output enables.

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in [Figure 1](#). Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

## Expander Product Terms

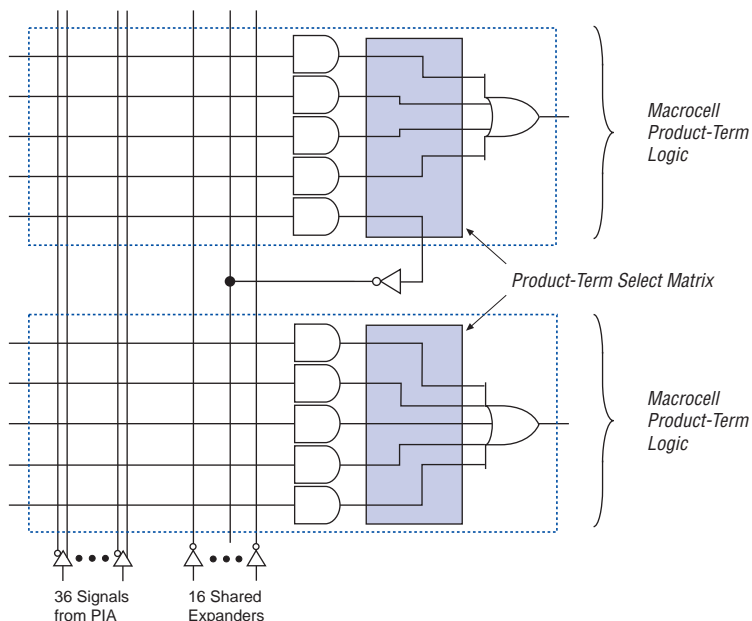
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000A architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ( $t_{SEXP}$ ) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

**Figure 3. MAX 7000A Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in an LAB.*



## In-System Programmability

MAX 7000A devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k $\Omega$ .

MAX 7000AE devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP\_Done bit that provides safe operation when in-system programming is interrupted. This ISP\_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is only available in EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, and EPM7512AE devices.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster serial/USB communications cable, ByteBlasterMV parallel port download cable, and BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000AE devices can be programmed with either an adaptive or constant (non-adaptive) algorithm. EPM7128A and EPM7256A device can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD 71, can be used to program MAX 7000A devices with in-circuit testers, PCs, or embedded processors.



For more information on using the Jam STAPL language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)*.

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 7000A Device*

The time required to program a single MAX 7000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:  $t_{PROG}$  = Programming time  
 $t_{PPULSE}$  = Sum of the fixed times to erase, program, and verify the EEPROM cells  
 $Cycle_{PTCK}$  = Number of TCK cycles to program a device  
 $f_{TCK}$  = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:  $t_{VER}$  = Verify time  
 $t_{VPULSE}$  = Sum of the fixed times to verify the EEPROM cells  
 $Cycle_{VTCK}$  = Number of TCK cycles to verify a device

## Open-Drain Output Option

MAX 7000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Open-drain output pins on MAX 7000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high  $V_{IH}$ . When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V to meet CMOS  $V_{OH}$  requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

## Programmable Ground Pins

Each unused I/O pin on MAX 7000A devices may be used as an additional ground pin. In EPM7128A and EPM7256A devices, utilizing unused I/O pins as additional ground pins requires using the associated macrocell. In MAX 7000AE devices, this programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

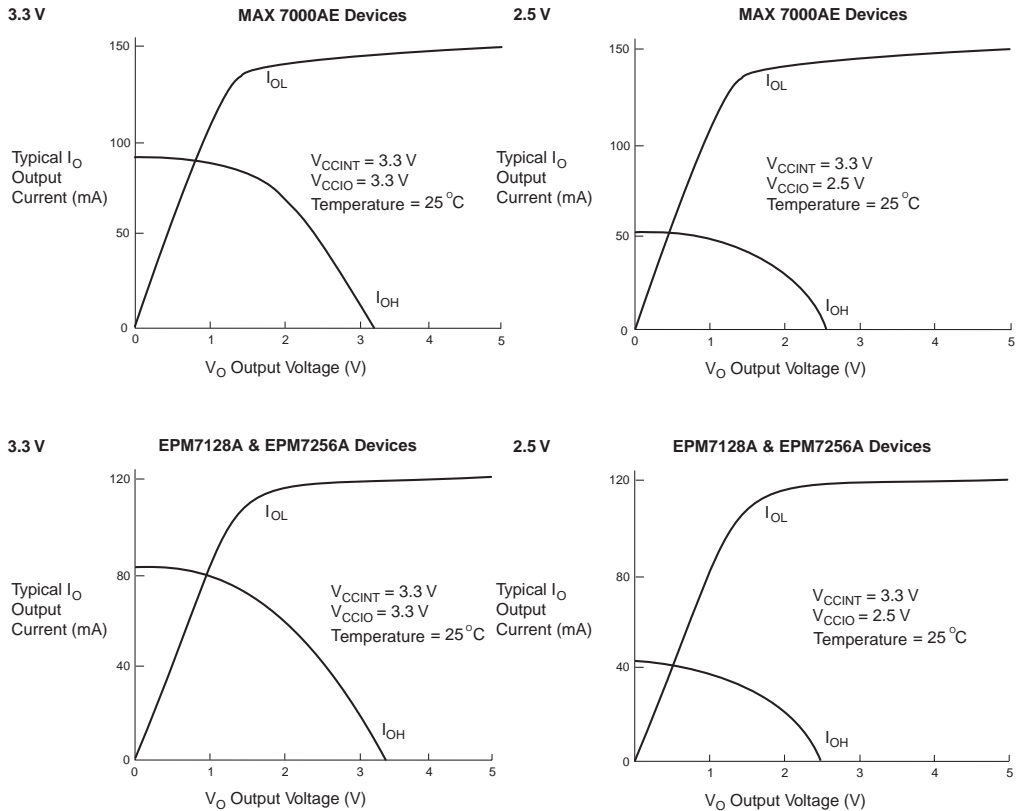
## Slew-Rate Control

The output buffer for each MAX 7000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.



Figure 10 shows the typical output drive characteristics of MAX 7000A devices.

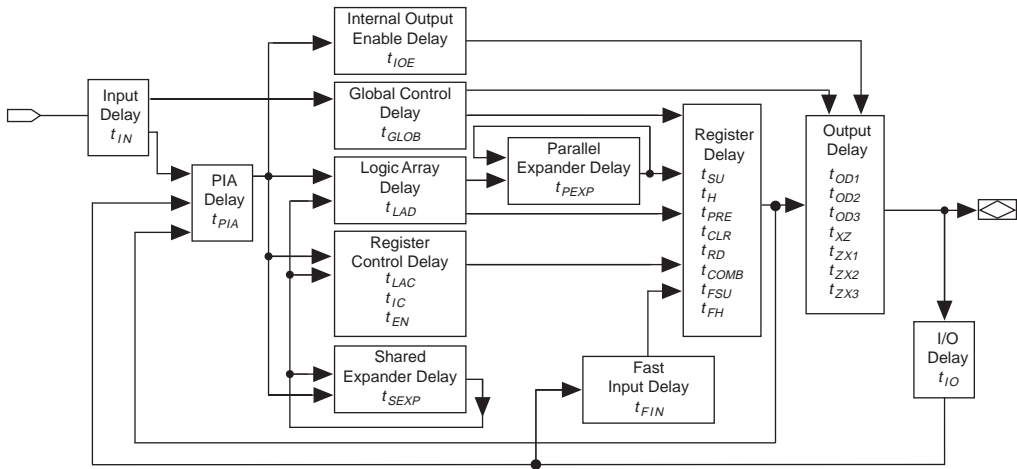
**Figure 10. Output Drive Characteristics of MAX 7000A Devices**



## Timing Model

MAX 7000A device timing can be analyzed with the Altera software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 11. MAX 7000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 11. MAX 7000A Timing Model



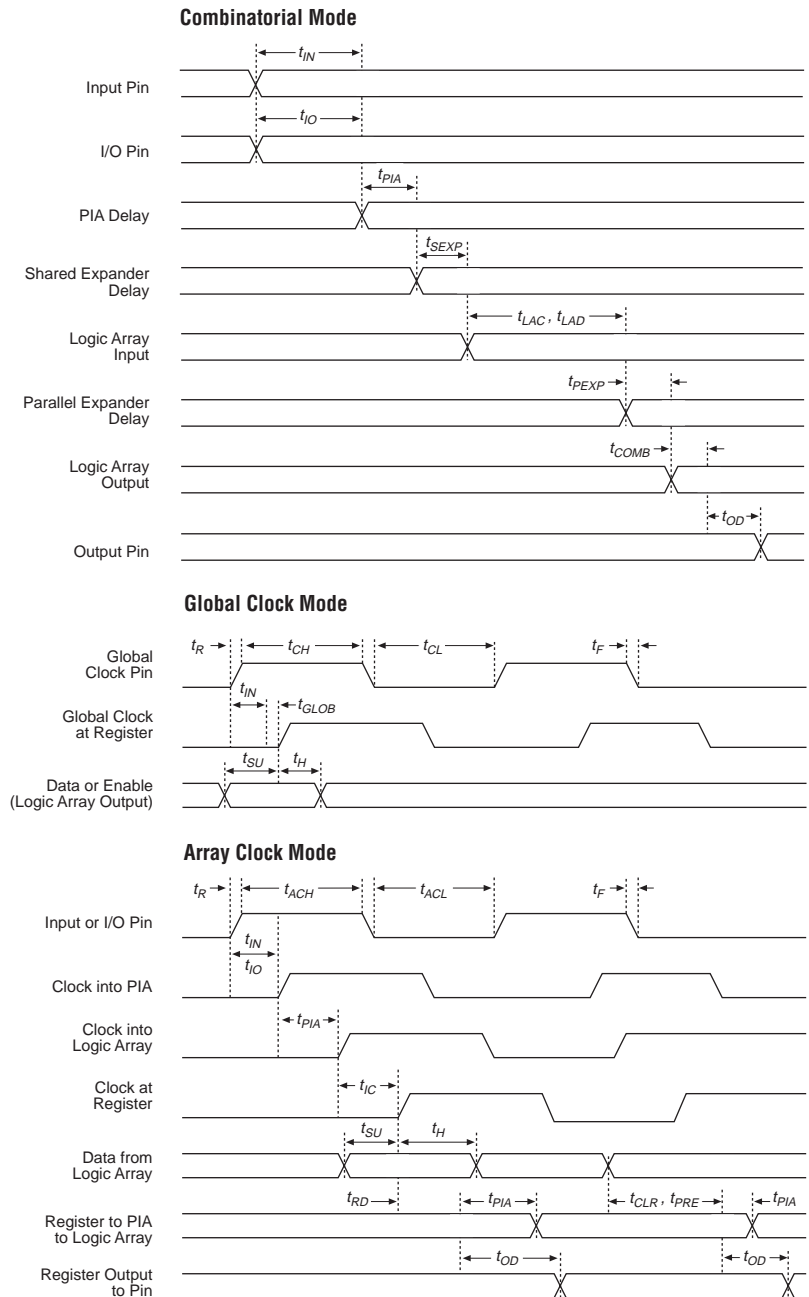
The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 12 shows the timing relationship between internal and external delay parameters.



See [Application Note 94 \(Understanding MAX 7000 Timing\)](#) for more information.

**Figure 12. MAX 7000A Switching Waveforms**

$t_R$  &  $t_F < 2$  ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Tables 17 through 30 show EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, EPM7512AE, EPM7128A, and EPM7256A timing information.

**Table 17. EPM7032AE External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t <sub>SU</sub>	Global clock setup time	(2)	2.9		4.7		6.3		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t <sub>CH</sub>	Global clock high time		2.0		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.6		2.5		3.6		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.3		0.5		0.5		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.4	ns
t <sub>ACH</sub>	Array clock high time		2.0		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.0		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		4.4		7.2		9.7	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	227.3		138.9		103.1		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		4.4		7.2		9.7	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	227.3		138.9		103.1		MHz

**Table 22. EPM7128AE Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{EN}$	Register enable time			0.7		1.0		1.3	ns
$t_{GLOB}$	Global control delay			1.1		1.6		2.0	ns
$t_{PRE}$	Register preset time			1.4		2.0		2.7	ns
$t_{CLR}$	Register clear time			1.4		2.0		2.7	ns
$t_{PIA}$	PIA delay	(2)		1.4		2.0		2.6	ns
$t_{LPA}$	Low-power adder	(6)		4.0		4.0		5.0	ns

**Table 25. EPM7512AE External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		7.5		10.0		12.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		7.5		10.0		12.0	ns
t <sub>SU</sub>	Global clock setup time	(2)	5.6		7.6		9.1		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	4.7	1.0	6.3	1.0	7.5	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	2.5		3.5		4.1		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.2		0.3		0.4		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	7.8	1.0	10.4	1.0	12.5	ns
t <sub>ACH</sub>	Array clock high time		3.0		4.0		5.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		4.0		5.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	3.0		4.0		5.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		8.6		11.5		13.9	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	116.3		87.0		71.9		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		8.6		11.5		13.9	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	116.3		87.0		71.9		MHz

**Table 26. EPM7512AE Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		0.9		1.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		0.9		1.0	ns
$t_{FIN}$	Fast input delay			3.1		3.6		4.1	ns
$t_{SEXP}$	Shared expander delay			2.7		3.5		4.4	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.5		0.6	ns
$t_{LAD}$	Logic array delay			2.2		2.8		3.5	ns
$t_{LAC}$	Logic control array delay			1.0		1.3		1.7	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.0		1.5		1.7	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.5		2.0		2.2	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.0		6.5		6.7	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		5.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		5.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		10.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		5.0		5.0	ns
$t_{SU}$	Register setup time		2.1		3.0		3.5		ns
$t_H$	Register hold time		0.6		0.8		1.0		ns
$t_{FSU}$	Register setup time of fast input		1.6		1.6		1.6		ns
$t_{FH}$	Register hold time of fast input		1.4		1.4		1.4		ns
$t_{RD}$	Register delay			1.3		1.7		2.1	ns
$t_{COMB}$	Combinatorial delay			0.6		0.8		1.0	ns

**Table 26. EPM7512AE Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
$t_{IC}$	Array clock delay			1.8		2.3		2.9	ns
$t_{EN}$	Register enable time			1.0		1.3		1.7	ns
$t_{GLOB}$	Global control delay			1.7		2.2		2.7	ns
$t_{PRE}$	Register preset time			1.0		1.4		1.7	ns
$t_{CLR}$	Register clear time			1.0		1.4		1.7	ns
$t_{PIA}$	PIA delay	(2)		3.0		4.0		4.8	ns
$t_{LPA}$	Low-power adder	(6)		4.5		5.0		5.0	ns



**Table 28. EPM7128A Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.6		0.7		0.9		1.1	ns
$t_{IO}$	I/O input pad and buffer delay			0.6		0.7		0.9		1.1	ns
$t_{FIN}$	Fast input delay			2.7		3.1		3.6		3.9	ns
$t_{SEXP}$	Shared expander delay			2.5		3.2		4.3		5.1	ns
$t_{PEXP}$	Parallel expander delay			0.7		0.8		1.1		1.3	ns
$t_{LAD}$	Logic array delay			2.4		3.0		4.1		4.9	ns
$t_{LAC}$	Logic control array delay			2.4		3.0		4.1		4.9	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.4		0.6		0.7		0.9	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		0.9		1.1		1.2		1.4	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.4		5.6		5.7		5.9	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0		5.0	ns
$t_{SU}$	Register setup time		1.9		2.4		3.1		3.8		ns
$t_H$	Register hold time		1.5		2.2		3.3		4.3		ns
$t_{FSU}$	Register setup time of fast input		0.8		1.1		1.1		1.1		ns
$t_{FH}$	Register hold time of fast input		1.7		1.9		1.9		1.9		ns

The parameters in this equation are:

- $MC_{TON}$  = Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)  
 $MC_{DEV}$  = Number of macrocells in the device  
 $MC_{USED}$  = Total number of macrocells in the design, as reported in the Report File  
 $f_{MAX}$  = Highest clock frequency to the device  
 $to_{gLC}$  = Average percentage of logic cells toggling at each clock (typically 12.5%)  
A, B, C = Constants, shown in [Table 31](#)

**Table 31. MAX 7000A  $I_{CC}$  Equation Constants**

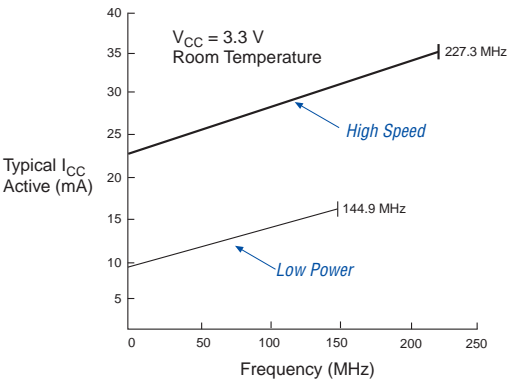
Device	A	B	C
EPM7032AE	0.71	0.30	0.014
EPM7064AE	0.71	0.30	0.014
EPM7128A	0.71	0.30	0.014
EPM7128AE	0.71	0.30	0.014
EPM7256A	0.71	0.30	0.014
EPM7256AE	0.71	0.30	0.014
EPM7512AE	0.71	0.30	0.014

This calculation provides an  $I_{CC}$  estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual  $I_{CC}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

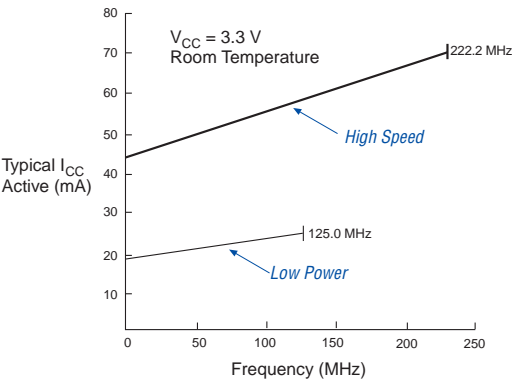
Figure 13 shows the typical supply current versus frequency for MAX 7000A devices.

Figure 13.  $I_{CC}$  vs. Frequency for MAX 7000A Devices (Part 1 of 2)

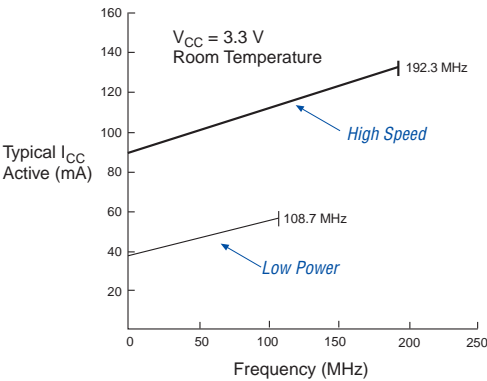
EPM7032AE



EPM7064AE



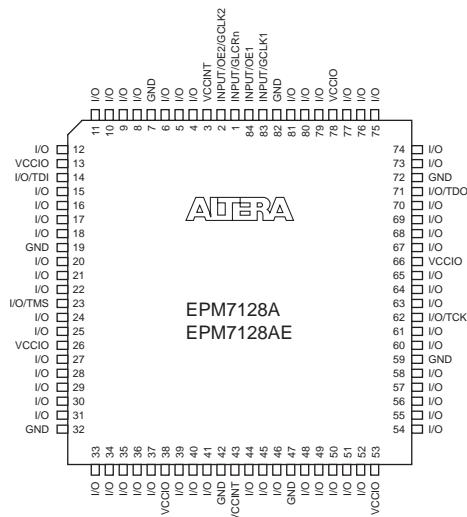
EPM7128A & EPM7128AE



*Package outlines not drawn to scale.*



*Package outline not drawn to scale.*



**Figure 21. 208-Pin PQFP Package Pin-Out Diagram**

Package outline not drawn to scale.

