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Intel - EPM7256AETI144-7 Datasheet



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Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	120
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256aeti144-7

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Table 1. MAX 7000A Device Features									
Feature	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE				
Usable gates	600	1,250	2,500	5,000	10,000				
Macrocells	32	64	128	256	512				
Logic array blocks	2	4	8	16	32				
Maximum user I/O pins	36	68	100	164	212				
t _{PD} (ns)	4.5	4.5	5.0	5.5	7.5				
t _{SU} (ns)	2.9	2.8	3.3	3.9	5.6				
t _{FSU} (ns)	2.5	2.5	2.5	2.5	3.0				
t _{CO1} (ns)	3.0	3.1	3.4	3.5	4.7				
f _{CNT} (MHz)	227.3	222.2	192.3	172.4	116.3				

...and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt[™] I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), spacesaving FineLine BGA[™], and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins



Figure 1. MAX 7000A Device Block Diagram

Note:

(1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enables. EPM7512AE devices have 10 output enables.

Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- **3**6 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Macrocells

MAX 7000A macrocells can be individually configured for either sequential or combinatorial logic operation. The macrocells consist of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows a MAX 7000A macrocell.



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000A devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in a MAX 7000AE device may be set to either a high or low state. This power-up state is specified at design entry. Upon power-up, each register in EPM7128A and EPM7256A devices are set to a low state.

All MAX 7000A I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (as low as 2.5 ns) input setup time.

Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000A architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.



Shareable expanders can be shared by any or all macrocells in an LAB.



SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ballcount packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 7).





Printed Circuit Board Designed for 256-Pin FineLine BGA Package



 100-Pin FineLine BGA Package (Reduced I/O Count or Logic Requirements)
 256-Pin FineLine BGA Package (Increased I/O Count or Logic Requirements)



For more information on using the Jam STAPL language, see *Application Note 88* (Using the Jam Language for ISP & ICR via an Embedded Processor) and *Application Note 122* (Using Jam STAPL for ISP & ICR via an Embedded *Processor*).

ISP circuitry in MAX 7000AE devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

- 1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
- 2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
- 3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
- 4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
- 5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
- 6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Table 7. MAX 7000A Stand-Alone Verification Times for Different Test Clock Frequencies										
Device		f _{TCK}								
	10 MHz	10 MHz 5 MHz 2 MHz 1 MHz 500 kHz 200 kHz 100 kHz 50 kHz								
EPM7032AE	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	S	
EPM7064AE	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	S	
EPM7128AE	0.01	0.02	0.04	0.07	0.14	0.34	0.68	1.36	S	
EPM7256AE	0.02	0.03	0.08	0.15	0.30	0.75	1.49	2.98	S	
EPM7512AE	0.03	0.06	0.15	0.30	0.60	1.49	2.97	5.94	S	
EPM7128A (1)	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	S	
EPM7256A (1)	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	s	

Note to tables:

(1) EPM7128A and EPM7256A devices can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

Programming with External Hardware

MAX 7000A devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checks to ensure adequate electrical contact between the adapter and the device.



For more information, see the Altera Programming Hardware Data Sheet.

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices.



For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) **Boundary-Scan** Support

MAX 7000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1. Table 8 describes the JTAG instructions supported by MAX 7000A devices. The pin-out tables, available from the Altera web site (http://www.altera.com), show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

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JTAG Instruction	Description					
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins					
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins					
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation					
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO					
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO. The USERCODE instruction is available for MAX 7000AE devices only					
UESCODE	These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be shifted out of TDO. UESCODE instructions are available for EPM7128A and EPM7256A devices only.					
ISP Instructions	These instructions are used when programming MAX 7000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam STAPL File, JBC File, or SVF File via an embedded processor or test equipment.					

Table 8. MAX 7000A JTAG Instructions

Figure 8 shows timing information for the JTAG signals.



Figure 8. MAX 7000A JTAG Waveforms

Table 11 shows the JTAG timing parameters and values for MAX 7000A devices.

Table 11. JTAG Timing Parameters & Values for MAX 7000A Devices Note (1)								
Symbol	Parameter	Min	Max	Unit				
t _{JCP}	TCK clock period	100		ns				
t _{JCH}	TCK clock high time	50		ns				
t _{JCL}	TCK clock low time	50		ns				
t _{JPSU}	JTAG port setup time	20		ns				
t _{JPH}	JTAG port hold time	45		ns				
t _{JPCO}	JTAG port clock to output		25	ns				
t _{JPZX}	JTAG port high impedance to valid output		25	ns				
t _{JPXZ}	JTAG port valid output to high impedance		25	ns				
t _{JSSU}	Capture register setup time	20		ns				
t _{JSH}	Capture register hold time	45		ns				
t _{JSCO}	Update register clock to output		25	ns				
t _{JSZX}	Update register high impedance to valid output		25	ns				
t _{JSXZ}	Update register valid output to high impedance		25	ns				

Note:

(1) Timing parameters shown in this table apply for all specified VCCIO levels.

MAX 7000A Programmable Logic Device Data Sheet

Notes to tables:

- (1) See the Operating Requirements for Altera Devices Data Sheet.
- (2) Minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) For EPM7128A and EPM7256A devices only, V_{CC} must rise monotonically.
- (4) In MAX 7000AE devices, all pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (5) These devices support in-system programming for -40° to 100° C. For in-system programming support between -40° and 0° C, contact Altera Applications.
- (6) These values are specified under the recommended operating conditions shown in Table 14 on page 28.
- (7) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (8) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.
- (9) This value is specified for normal device operation. For MAX 7000AE devices, the maximum leakage current during power-up is $\pm 300 \ \mu$ A. For EPM7128A and EPM7256A devices, leakage current during power-up is not specified.
- (10) For EPM7128A and EPM7256A devices, this pull-up exists while a device is programmed in-system.
- (11) For MAX 7000AE devices, this pull-up exists while devices are programmed in-system and in unprogrammed devices during power-up.
- (12) Capacitance is measured at 25 °C and is sample-tested only. The OE1 pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
- (13) The POR time for MAX 7000AE devices (except MAX 7128A and MAX 7256A devices) does not exceed 100 μs. The sufficient V_{CCINT} voltage level for POR is 3.0 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.

Symbol	Parameter	Conditions	Speed Grade Un						
			-	4		7	-10		
			Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.6		1.1		1.4	ns
t _{IO}	I/O input pad and buffer delay			0.6		1.1		1.4	ns
t _{FIN}	Fast input delay			2.5		3.0		3.7	ns
t _{SEXP}	Shared expander delay			1.8		3.0		3.9	ns
t _{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t _{LAD}	Logic array delay			1.5		2.5		3.2	ns
t _{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t _{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t _{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		0.8		1.3		1.8	ns
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		1.3		1.8		2.3	ns
t _{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		5.8		6.3		6.8	ns
t _{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		4.0		5.0	ns
t _{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		4.5		5.5	ns
t _{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3 V$	C1 = 35 pF		9.0		9.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t _{SU}	Register setup time		1.3		2.0		2.9		ns
t _H	Register hold time		0.6		1.0		1.3		ns
t _{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t _{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t _{RD}	Register delay			0.7		1.2		1.6	ns
t _{COMB}	Combinatorial delay			0.6		0.9		1.3	ns
t _{IC}	Array clock delay			1.2		1.9		2.5	ns

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Symbol	Parameter	Conditions	Speed Grade						Unit
-			-	5	-7		7 -10		
			Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.7		0.9		1.2	ns
t _{IO}	I/O input pad and buffer delay			0.7		0.9		1.2	ns
t _{FIN}	Fast input delay			2.4		2.9		3.4	ns
t _{SEXP}	Shared expander delay			2.1		2.8		3.7	ns
t _{PEXP}	Parallel expander delay			0.3		0.5		0.6	ns
t _{LAD}	Logic array delay			1.7		2.2		2.8	ns
t _{LAC}	Logic control array delay			0.8		1.0		1.3	ns
t _{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t _{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		0.9		1.2		1.6	ns
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		1.4		1.7		2.1	ns
t _{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		5.9		6.2		6.6	ns
t _{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		4.0		5.0	ns
t _{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		4.5		5.5	ns
t _{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3 V$	C1 = 35 pF		9.0		9.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t _{SU}	Register setup time		1.5		2.1		2.9		ns
t _H	Register hold time		0.7		0.9		1.2		ns
t _{FSU}	Register setup time of fast input		1.1		1.6		1.6		ns
t _{FH}	Register hold time of fast input		1.4		1.4		1.4		ns
t _{RD}	Register delay			0.9		1.2		1.6	ns
t _{COMB}	Combinatorial delay			0.5		0.8		1.2	ns

7

The parameters in this equation are:

MC _{TON}	=	Number of macrocells with the Turbo Bit option turned
		on, as reported in the MAX+PLUS II Report File (.rpt)
MC _{DEV}	=	Number of macrocells in the device
MC _{USED}	=	Total number of macrocells in the design, as reported in
		the Report File
f _{MAX}	=	Highest clock frequency to the device
togLC	=	Average percentage of logic cells toggling at each clock
-20		(typically 12.5%)
A, B, C	=	Constants, shown in Table 31

Table 31. MAX 7000A I _{CC} Equation Constants									
Device	A	В	C						
EPM7032AE	0.71	0.30	0.014						
EPM7064AE	0.71	0.30	0.014						
EPM7128A	0.71	0.30	0.014						
EPM7128AE	0.71	0.30	0.014						
EPM7256A	0.71	0.30	0.014						
EPM7256AE	0.71	0.30	0.014						
EPM7512AE	0.71	0.30	0.014						

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 13 shows the typical supply current versus frequency for MAX 7000A devices.





EPM7128A & EPM7128AE



Figure 15. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outlines not drawn to scale.



Figure 16. 84-Pin PLCC Package Pin-Out Diagram

Package outline not drawn to scale.



Figure 17. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.



Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram



Figure 21. 208-Pin PQFP Package Pin-Out Diagram

Package outline not drawn to scale.



Figure 23. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5 supersedes information published in previous versions.

Version 4.5

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5:

■ Updated text in the "Power Sequencing & Hot-Socketing" section.

Version 4.4

The following changes were made in the *MAX* 7000A Programmable Logic Device Data Sheet version 4.4:

- Added Tables 5 through 7.
 - Added "Programming Sequence" on page 17 and "Programming Times" on page 18.

Version 4.3

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.3:

- Added extended temperature devices to document
- Updated Table 14.

Version 4.2

The following changes were made in the *MAX* 7000A Programmable Logic Device Data Sheet version 4.2:

- Removed *Note* (1) from Table 2.
- Removed *Note* (4) from Tables 3 and 4.

Version 4.1

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.1:

- Updated leakage current information in Table 15.
- Updated Note (9) of Table 15.
- Updated *Note* (1) of Tables 17 through 30.



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