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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	512
Number of Gates	10000
Number of I/O	212
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7512aefc256-10n

Expander Product Terms

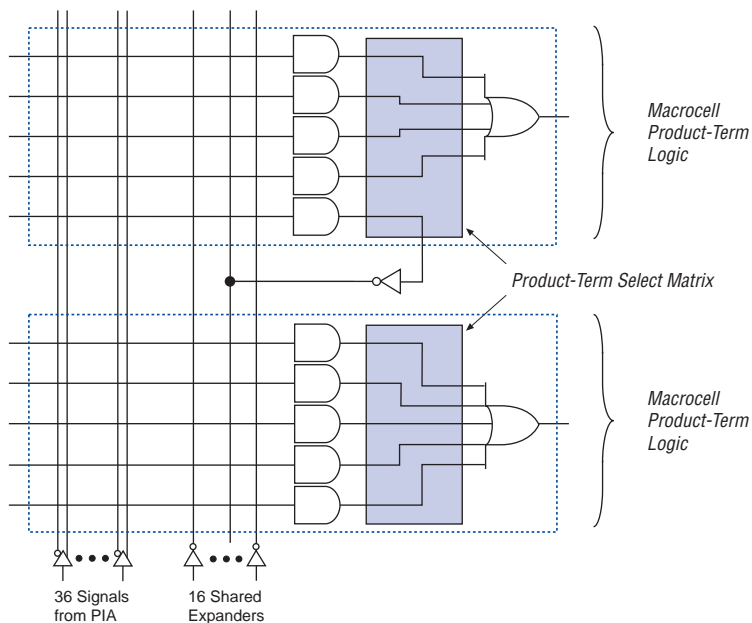
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000A architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 7000A Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

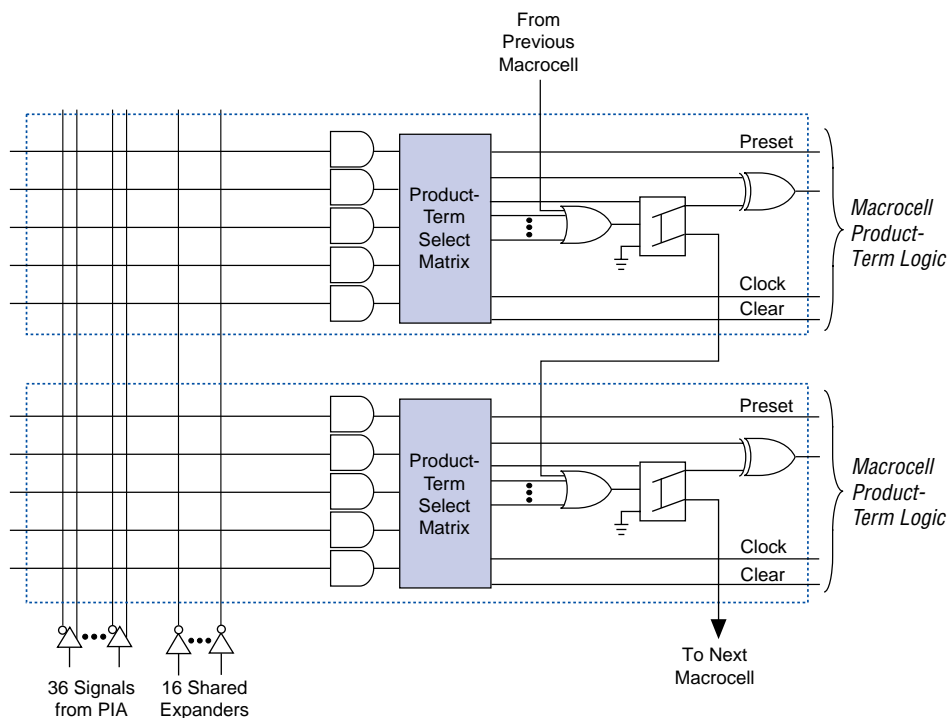
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders, and the highest-numbered macrocell can only borrow them. [Figure 4](#) shows how parallel expanders can be borrowed from a neighboring macrocell.

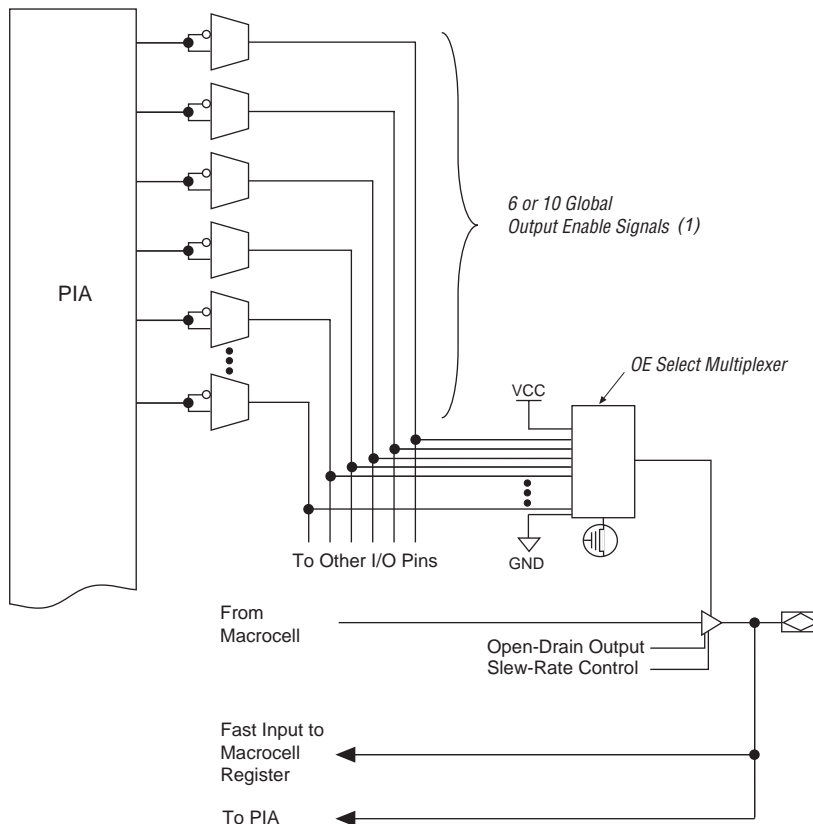
Figure 4. MAX 7000A Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 6. I/O Control Block of MAX 7000A Devices**Note:**

- (1) EPM7032AE, EPM7064AE, EPM7128A, EPM7128AE, EPM7256A, and EPM7256AE devices have six output enable signals. EPM7512AE devices have 10 output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC} , the output is enabled.

The MAX 7000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Power Sequencing & Hot-Socketing

Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000AE devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.

MAX 7000AE device I/O pins will not source or sink more than 300 μ A of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the OE1 and GLCRn pins. The OE1 and GLCRn pins can be driven up to 3.6 V during hot-socketing. After V_{CCINT} and V_{CCIO} reach the recommended operating conditions, these two pins are 5.0-V tolerant.

EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.

Design Security

All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 9](#). Test patterns can be used and then erased during early stages of the production flow.

Table 14. MAX 7000A Device Recommended Operating Conditions

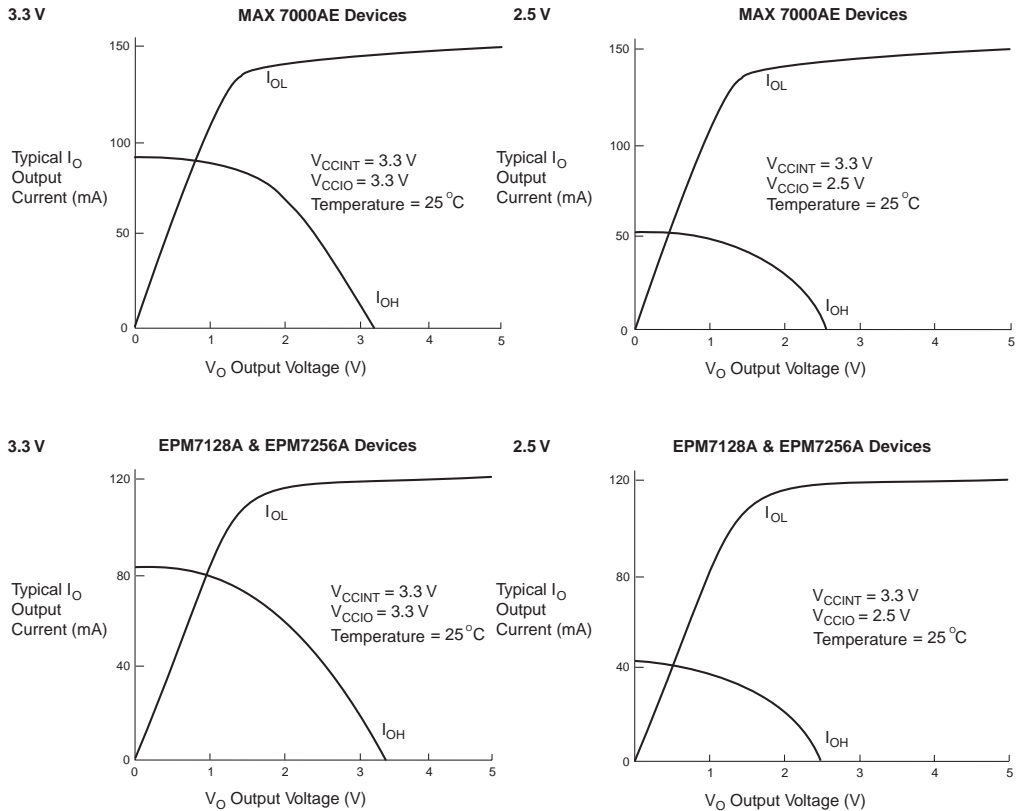
Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (13)	3.0	3.6	V
V _{CCIO}	Supply voltage for output drivers, 3.3-V operation	(3)	3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation	(3)	2.3	2.7	V
V _{CCISP}	Supply voltage during in-system programming		3.0	3.6	V
V _I	Input voltage	(4)	−0.5	5.75	V
V _O	Output voltage		0	V _{CCIO}	V
T _A	Ambient temperature	Commercial range	0	70	°C
		Industrial range (5)	−40	85	°C
T _J	Junction temperature	Commercial range	0	90	°C
		Industrial range (5)	−40	105	°C
		Extended range (5)	−40	130	°C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) For EPM7128A and EPM7256A devices only, V_{CC} must rise monotonically.
- (4) In MAX 7000AE devices, all pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (5) These devices support in-system programming for -40° to 100° C. For in-system programming support between -40° and 0° C, contact Altera Applications.
- (6) These values are specified under the recommended operating conditions shown in [Table 14 on page 28](#).
- (7) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (8) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.
- (9) This value is specified for normal device operation. For MAX 7000AE devices, the maximum leakage current during power-up is ± 300 μ A. For EPM7128A and EPM7256A devices, leakage current during power-up is not specified.
- (10) For EPM7128A and EPM7256A devices, this pull-up exists while a device is programmed in-system.
- (11) For MAX 7000AE devices, this pull-up exists while devices are programmed in-system and in unprogrammed devices during power-up.
- (12) Capacitance is measured at 25° C and is sample-tested only. The $\odot E1$ pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
- (13) The POR time for MAX 7000AE devices (except MAX 7128A and MAX 7256A devices) does not exceed 100 μ s. The sufficient V_{CCINT} voltage level for POR is 3.0 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.

Figure 10 shows the typical output drive characteristics of MAX 7000A devices.

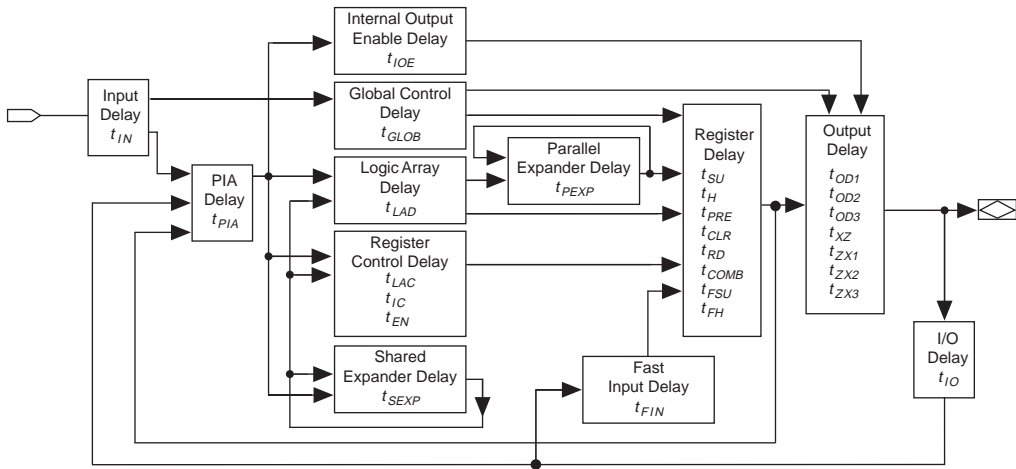
Figure 10. Output Drive Characteristics of MAX 7000A Devices



Timing Model

MAX 7000A device timing can be analyzed with the Altera software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 11. MAX 7000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 11. MAX 7000A Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 12 shows the timing relationship between internal and external delay parameters.



See [Application Note 94 \(Understanding MAX 7000 Timing\)](#) for more information.

Tables 17 through 30 show EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, EPM7512AE, EPM7128A, and EPM7256A timing information.

Table 17. EPM7032AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t _{SU}	Global clock setup time	(2)	2.9		4.7		6.3		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.6		2.5		3.6		ns
t _{AH}	Array clock hold time	(2)	0.3		0.5		0.5		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.4	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		4.4		7.2		9.7	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	227.3		138.9		103.1		MHz
t _{ACNT}	Minimum array clock period	(2)		4.4		7.2		9.7	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (4)	227.3		138.9		103.1		MHz

Table 20. EPM7064AE Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			1.0		1.5		2.2	ns
t_{PRE}	Register preset time			1.3		2.1		2.9	ns
t_{CLR}	Register clear time			1.3		2.1		2.9	ns
t_{PIA}	PIA delay	(2)		1.0		1.7		2.3	ns
t_{LPA}	Low-power adder	(6)		3.5		4.0		5.0	ns

Table 21. EPM7128AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10	ns
t _{SU}	Global clock setup time	(2)	3.3		4.9		6.6		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.4	1.0	5.0	1.0	6.6	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.8		2.8		3.8		ns
t _{AH}	Array clock hold time	(2)	0.2		0.3		0.4		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.9	1.0	7.1	1.0	9.4	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		5.2		7.7		10.2	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	192.3		129.9		98.0		MHz
t _{ACNT}	Minimum array clock period	(2)		5.2		7.7		10.2	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (4)	192.3		129.9		98.0		MHz

Table 25. EPM7512AE External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		7.5		10.0		12.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		7.5		10.0		12.0	ns
t _{SU}	Global clock setup time	(2)	5.6		7.6		9.1		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	4.7	1.0	6.3	1.0	7.5	ns
t _{CH}	Global clock high time		3.0		4.0		5.0		ns
t _{CL}	Global clock low time		3.0		4.0		5.0		ns
t _{ASU}	Array clock setup time	(2)	2.5		3.5		4.1		ns
t _{AH}	Array clock hold time	(2)	0.2		0.3		0.4		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	7.8	1.0	10.4	1.0	12.5	ns
t _{ACH}	Array clock high time		3.0		4.0		5.0		ns
t _{ACL}	Array clock low time		3.0		4.0		5.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		4.0		5.0		ns
t _{CNT}	Minimum global clock period	(2)		8.6		11.5		13.9	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	116.3		87.0		71.9		MHz
t _{ACNT}	Minimum array clock period	(2)		8.6		11.5		13.9	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (4)	116.3		87.0		71.9		MHz

Table 26. EPM7512AE Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		0.9		1.0	ns
t_{IO}	I/O input pad and buffer delay			0.7		0.9		1.0	ns
t_{FIN}	Fast input delay			3.1		3.6		4.1	ns
t_{SEXP}	Shared expander delay			2.7		3.5		4.4	ns
t_{PEXP}	Parallel expander delay			0.4		0.5		0.6	ns
t_{LAD}	Logic array delay			2.2		2.8		3.5	ns
t_{LAC}	Logic control array delay			1.0		1.3		1.7	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.0		1.5		1.7	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		1.5		2.0		2.2	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		6.0		6.5		6.7	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		5.0		5.0	ns
t_{SU}	Register setup time		2.1		3.0		3.5		ns
t_H	Register hold time		0.6		0.8		1.0		ns
t_{FSU}	Register setup time of fast input		1.6		1.6		1.6		ns
t_{FH}	Register hold time of fast input		1.4		1.4		1.4		ns
t_{RD}	Register delay			1.3		1.7		2.1	ns
t_{COMB}	Combinatorial delay			0.6		0.8		1.0	ns

Table 28. EPM7128A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		0.7		0.9		1.1	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.7		0.9		1.1	ns
t_{FIN}	Fast input delay			2.7		3.1		3.6		3.9	ns
t_{SEXP}	Shared expander delay			2.5		3.2		4.3		5.1	ns
t_{PEXP}	Parallel expander delay			0.7		0.8		1.1		1.3	ns
t_{LAD}	Logic array delay			2.4		3.0		4.1		4.9	ns
t_{LAC}	Logic control array delay			2.4		3.0		4.1		4.9	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.4		0.6		0.7		0.9	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		0.9		1.1		1.2		1.4	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.4		5.6		5.7		5.9	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$ (5)		4.5		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0		5.0	ns
t_{SU}	Register setup time		1.9		2.4		3.1		3.8		ns
t_H	Register hold time		1.5		2.2		3.3		4.3		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.7		1.9		1.9		1.9		ns

Table 28. EPM7128A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-12		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{RD}	Register delay			1.7		2.1		2.8		3.3	ns
t_{COMB}	Combinatorial delay			1.7		2.1		2.8		3.3	ns
t_{IC}	Array clock delay			2.4		3.0		4.1		4.9	ns
t_{EN}	Register enable time			2.4		3.0		4.1		4.9	ns
t_{GLOB}	Global control delay			1.0		1.2		1.7		2.0	ns
t_{PRE}	Register preset time			3.1		3.9		5.2		6.2	ns
t_{CLR}	Register clear time			3.1		3.9		5.2		6.2	ns
t_{PIA}	PIA delay	(2)		0.9		1.1		1.5		1.8	ns
t_{LPA}	Low-power adder	(6)		11.0		10.0		10.0		10.0	ns

Figure 15. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outlines not drawn to scale.

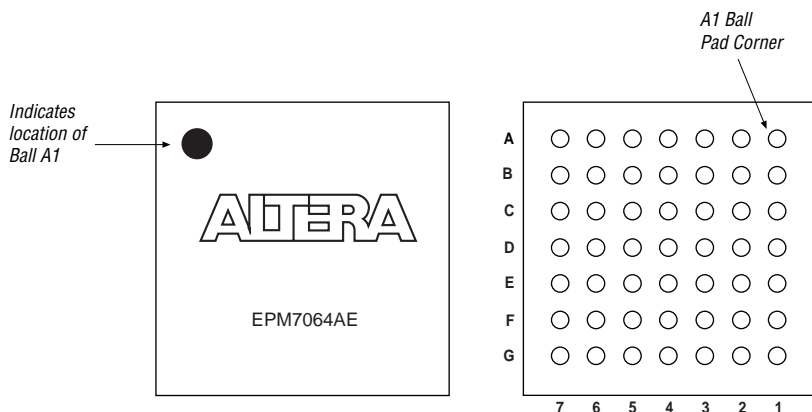


Figure 16. 84-Pin PLCC Package Pin-Out Diagram

Package outline not drawn to scale.

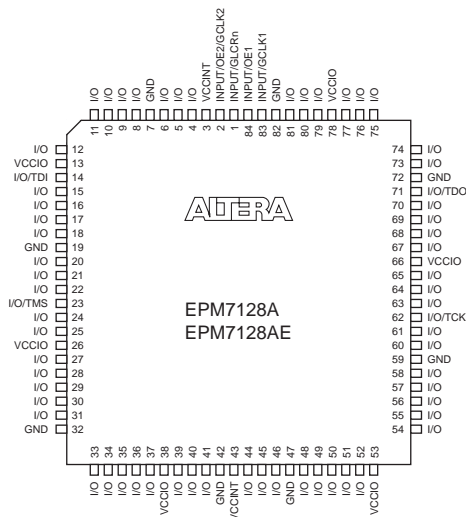


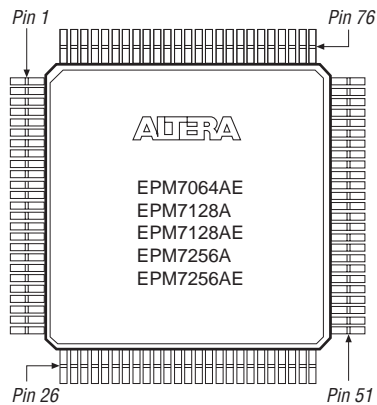
Figure 17. 100-Pin TQFP Package Pin-Out Diagram*Package outline not drawn to scale.***Figure 18. 100-Pin FineLine BGA Package Pin-Out Diagram***Package outline not drawn to scale.*

Figure 19. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

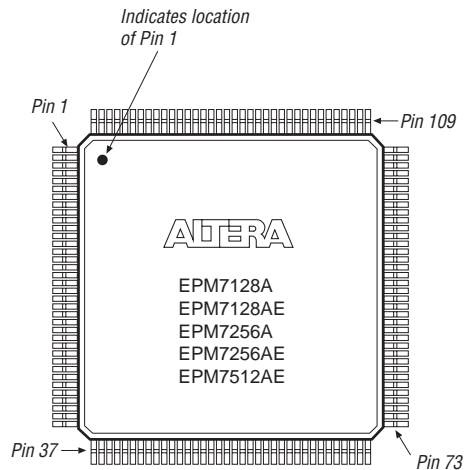


Figure 20. 169-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

