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Intel - EPM7512AEQC208-12 Datasheet



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Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	512
Number of Gates	10000
Number of I/O	176
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7512aeqc208-12

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Table 1. MAX 700	Table 1. MAX 7000A Device Features										
Feature	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE						
Usable gates	600	1,250	2,500	5,000	10,000						
Macrocells	32	64	128	256	512						
Logic array blocks	2	4	8	16	32						
Maximum user I/O pins	36	68	100	164	212						
t _{PD} (ns)	4.5	4.5	5.0	5.5	7.5						
t _{SU} (ns)	2.9	2.8	3.3	3.9	5.6						
t _{FSU} (ns)	2.5	2.5	2.5	2.5	3.0						
t _{CO1} (ns)	3.0	3.1	3.4	3.5	4.7						
f _{CNT} (MHz)	227.3	222.2	192.3	172.4	116.3						

...and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt[™] I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), spacesaving FineLine BGA[™], and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins

Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000A devices.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000A devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in a MAX 7000AE device may be set to either a high or low state. This power-up state is specified at design entry. Upon power-up, each register in EPM7128A and EPM7256A devices are set to a low state.

All MAX 7000A I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (as low as 2.5 ns) input setup time.

Figure 4. MAX 7000A Parallel Expanders





Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 5. MAX 7000A PIA Routing



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC} . Figure 6 shows the I/O control block for MAX 7000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

SameFrame Pin-Outs

MAX 7000A devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ballcount packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7128AE device in a 100-pin FineLine BGA package to an EPM7512AE device in a 256-pin FineLine BGA package.

The Altera design software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 7).





Printed Circuit Board Designed for 256-Pin FineLine BGA Package



 100-Pin FineLine BGA Package (Reduced I/O Count or Logic Requirements)
 256-Pin FineLine BGA Package (Increased I/O Count or Logic Requirements)

In-System Programmability

MAX 7000A devices can be programmed in-system via an industrystandard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k Ω .

MAX 7000AE devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is only available in EPM7032AE, EPM7064AE, EPM7128AE, EPM7256AE, and EPM7512AE devices.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster serial/USB communications cable, ByteBlasterMV parallel port download cable, and BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a predefined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000AE devices can be programmed with either an adaptive or constant (non-adaptive) algorithm. EPM7128A and EPM7256A device can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD 71, can be used to program MAX 7000A devices with incircuit testers, PCs, or embedded processors.

The programming times described in Tables 5 through 7 are associated with the worst-case method using the enhanced ISP algorithm.

Table 5. MAX 7000A t _{PULSE} & Cycle _{TCK} Values									
Device	Progra	amming	Stand-Alone Verification						
	<i>t_{PPULSE}</i> (s)	Cycle _{PTCK}	t _{VPULSE} (s)	Cycle _{VTCK}					
EPM7032AE	2.00	55,000	0.002	18,000					
EPM7064AE	2.00	105,000	0.002	35,000					
EPM7128AE	2.00	205,000	0.002	68,000					
EPM7256AE	2.00	447,000	0.002	149,000					
EPM7512AE	2.00	890,000	0.002	297,000					
EPM7128A (1)	5.11	832,000	0.03	528,000					
EPM7256A (1)	6.43	1,603,000	0.03	1,024,000					

Tables 6 and 7 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 6. MAX 7000A In-System Programming Times for Different Test Clock Frequencies									
Device				f	тск				Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032AE	2.01	2.01	2.03	2.06	2.11	2.28	2.55	3.10	S
EPM7064AE	2.01	2.02	2.05	2.11	2.21	2.53	3.05	4.10	S
EPM7128AE	2.02	2.04	2.10	2.21	2.41	3.03	4.05	6.10	S
EPM7256AE	2.05	2.09	2.23	2.45	2.90	4.24	6.47	10.94	S
EPM7512AE	2.09	2.18	2.45	2.89	3.78	6.45	10.90	19.80	S
EPM7128A (1)	5.19	5.27	5.52	5.94	6.77	9.27	13.43	21.75	S
EPM7256A (1)	6.59	6.75	7.23	8.03	9.64	14.45	22.46	38.49	S

Table 7. MAX 7000A Stand-Alone Verification Times for Different Test Clock Frequencies										
Device				1	тск				Units	
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz		
EPM7032AE	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	S	
EPM7064AE	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	S	
EPM7128AE	0.01	0.02	0.04	0.07	0.14	0.34	0.68	1.36	S	
EPM7256AE	0.02	0.03	0.08	0.15	0.30	0.75	1.49	2.98	S	
EPM7512AE	0.03	0.06	0.15	0.30	0.60	1.49	2.97	5.94	S	
EPM7128A (1)	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	S	
EPM7256A (1)	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	S	

Note to tables:

(1) EPM7128A and EPM7256A devices can only be programmed with an adaptive algorithm; users programming these two devices on platforms that cannot use an adaptive algorithm should use EPM7128AE and EPM7256AE devices.

Programming with External Hardware

MAX 7000A devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checks to ensure adequate electrical contact between the adapter and the device.



For more information, see the Altera Programming Hardware Data Sheet.

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices.



For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) **Boundary-Scan** Support

MAX 7000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1. Table 8 describes the JTAG instructions supported by MAX 7000A devices. The pin-out tables, available from the Altera web site (http://www.altera.com), show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

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JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO. The USERCODE instruction is available for MAX 7000AE devices only
UESCODE	These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be shifted out of TDO. UESCODE instructions are available for EPM7128A and EPM7256A devices only.
ISP Instructions	These instructions are used when programming MAX 7000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or using a Jam STAPL File, JBC File, or SVF File via an embedded processor or test equipment.

Table 8. MAX 7000A JTAG Instructions

Figure 8 shows timing information for the JTAG signals.



Figure 8. MAX 7000A JTAG Waveforms

Table 11 shows the JTAG timing parameters and values for MAX 7000A devices.

Table 1	Table 11. JTAG Timing Parameters & Values for MAX 7000A Devices Note (1)										
Symbol	Parameter	Min	Max	Unit							
t _{JCP}	TCK clock period	100		ns							
t _{JCH}	TCK clock high time	50		ns							
t _{JCL}	TCK clock low time	50		ns							
t _{JPSU}	JTAG port setup time	20		ns							
t _{JPH}	JTAG port hold time	45		ns							
t _{JPCO}	JTAG port clock to output		25	ns							
t _{JPZX}	JTAG port high impedance to valid output		25	ns							
t _{JPXZ}	JTAG port valid output to high impedance		25	ns							
t _{JSSU}	Capture register setup time	20		ns							
t _{JSH}	Capture register hold time	45		ns							
t _{JSCO}	Update register clock to output		25	ns							
t _{JSZX}	Update register high impedance to valid output		25	ns							
t _{JSXZ}	Update register valid output to high impedance		25	ns							

Note:

(1) Timing parameters shown in this table apply for all specified VCCIO levels.

Programmable Speed/Power Control

MAX 7000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000A device for either high-speed (i.e., with the Turbo BitTM option turned on) or low-power operation (i.e., with the Turbo Bit option turned off). As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , \mathbf{t}_{ACL} , and $\mathbf{t_{CPPW}}$ parameters.

Output Configuration

MAX 7000A device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000A devices to connect to systems with differing supply voltages. MAX 7000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 3.0 V incur a slightly greater timing delay of t_{OD2} instead of t_{OD1} . Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 12 describes the MAX 7000A MultiVolt I/O support.

Table 12. MAX 7000A MultiVolt I/O Support										
V _{CCIO} Voltage	Inp	out Signal	(V)	Out	put Signa	I (V)				
	2.5	3.3	5.0	2.5	3.3	5.0				
2.5	~	~	~	~						
3.3	 Image: A set of the set of the	 Image: A start of the start of	\checkmark		\checkmark	~				

Open-Drain Output Option

MAX 7000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Open-drain output pins on MAX 7000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high V_{IH} . When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V to meet CMOS V_{OH} requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Programmable Ground Pins

Each unused I/O pin on MAX 7000A devices may be used as an additional ground pin. In EPM7128A and EPM7256A devices, utilizing unused I/O pins as additional ground pins requires using the associated macrocell. In MAX 7000AE devices, this programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

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Table 1	Table 18. EPM7032AE Internal Timing Parameters (Part 2 of 2) Note (1)									
Symbol	Parameter	Conditions			Speed	Grade			Unit	
			-	-4		-7		-10		
			Min	Max	Min	Max	Min	Max		
t _{IC}	Array clock delay			1.2		2.0		2.5	ns	
t _{EN}	Register enable time			0.6		1.0		1.2	ns	
t _{GLOB}	Global control delay			0.8		1.3		1.9	ns	
t _{PRE}	Register preset time			1.2		1.9		2.6	ns	
t _{CLR}	Register clear time			1.2		1.9		2.6	ns	
t _{PIA}	PIA delay	(2)		0.9		1.5		2.1	ns	
t _{LPA}	Low-power adder	(6)		2.5		4.0		5.0	ns	

Table 20	Table 20. EPM7064AE Internal Timing Parameters (Part 2 of 2) Note (1)									
Symbol	Parameter	Conditions			Speed	Grade			Unit	
			-,	-4		-7		10		
			Min	Max	Min	Max	Min	Max		
t _{EN}	Register enable time			0.6		1.0		1.2	ns	
t _{GLOB}	Global control delay			1.0		1.5		2.2	ns	
t _{PRE}	Register preset time			1.3		2.1		2.9	ns	
t _{CLR}	Register clear time			1.3		2.1		2.9	ns	
t _{PIA}	PIA delay	(2)		1.0		1.7		2.3	ns	
t _{LPA}	Low-power adder	(6)		3.5		4.0		5.0	ns	

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Table 22	Table 22. EPM7128AE Internal Timing Parameters (Part 2 of 2) Note (1)									
Symbol	Parameter	Conditions			Speed	Grade			Unit	
			-		j -7		-10			
			Min	Max	Min	Max	Min	Max		
t _{EN}	Register enable time			0.7		1.0		1.3	ns	
t _{GLOB}	Global control delay			1.1		1.6		2.0	ns	
t _{PRE}	Register preset time			1.4		2.0		2.7	ns	
t _{CLR}	Register clear time			1.4		2.0		2.7	ns	
t _{PIA}	PIA delay	(2)		1.4		2.0		2.6	ns	
t _{LPA}	Low-power adder	(6)		4.0		4.0		5.0	ns	

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Symbol	Parameter	Conditions			Speed	Grade			Unit
-			-	5	-	7	-	10	
			Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.7		0.9		1.2	ns
t _{IO}	I/O input pad and buffer delay			0.7		0.9		1.2	ns
t _{FIN}	Fast input delay			2.4		2.9		3.4	ns
t _{SEXP}	Shared expander delay			2.1		2.8		3.7	ns
t _{PEXP}	Parallel expander delay			0.3		0.5		0.6	ns
t _{LAD}	Logic array delay			1.7		2.2		2.8	ns
t _{LAC}	Logic control array delay			0.8		1.0		1.3	ns
t _{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t _{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		0.9		1.2		1.6	ns
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		1.4		1.7		2.1	ns
t _{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		5.9		6.2		6.6	ns
t _{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		4.0		5.0	ns
t _{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF (5)		4.5		4.5		5.5	ns
t _{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3 V$	C1 = 35 pF		9.0		9.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t _{SU}	Register setup time		1.5		2.1		2.9		ns
t _H	Register hold time		0.7		0.9		1.2		ns
t _{FSU}	Register setup time of fast input		1.1		1.6		1.6		ns
t _{FH}	Register hold time of fast input		1.4		1.4		1.4		ns
t _{RD}	Register delay			0.9		1.2		1.6	ns
t _{COMB}	Combinatorial delay			0.5		0.8		1.2	ns

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Table 24. EPM7256AE Internal Timing Parameters (Part 2 of 2) Note (1)										
Symbol	Parameter	Conditions	Speed Grade							
			-	5	-7		-10		1	
			Min	Max	Min	Max	Min	Max	1	
t _{IC}	Array clock delay			1.2		1.6		2.1	ns	
t _{EN}	Register enable time			0.8		1.0		1.3	ns	
t _{GLOB}	Global control delay			1.0		1.5		2.0	ns	
t _{PRE}	Register preset time			1.6		2.3		3.0	ns	
t _{CLR}	Register clear time			1.6		2.3		3.0	ns	
t _{PIA}	PIA delay	(2)		1.7		2.4		3.2	ns	
t _{LPA}	Low-power adder	(6)		4.0		4.0		5.0	ns	

Table 28. EPM7128A Internal Timing Parameters (Part 2 of 2) Note (1)											
Symbol	Parameter	Conditions	Speed Grade								
			-	6	-7		-10		-12		1
			Min	Мах	Min	Мах	Min	Max	Min	Мах	
t _{RD}	Register delay			1.7		2.1		2.8		3.3	ns
t _{COMB}	Combinatorial delay			1.7		2.1		2.8		3.3	ns
t _{IC}	Array clock delay			2.4		3.0		4.1		4.9	ns
t _{EN}	Register enable time			2.4		3.0		4.1		4.9	ns
t _{GLOB}	Global control delay			1.0		1.2		1.7		2.0	ns
t _{PRE}	Register preset time			3.1		3.9		5.2		6.2	ns
t _{CLR}	Register clear time			3.1		3.9		5.2		6.2	ns
t _{PIA}	PIA delay	(2)		0.9		1.1		1.5		1.8	ns
t _{LPA}	Low-power adder	(6)		11.0		10.0		10.0		10.0	ns

Table 29. EPM7256A External Timing ParametersNote (1)											
Symbol	Parameter	Conditions	Speed Grade I								Unit
			-	-6		-7		-10		-12	
			Min	Max	Min	Max	Min	Мах	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		6.0		7.5		10.0		12.0	ns
t _{PD2}	I/O input to non- registered output	C1 = 35 pF (2)		6.0		7.5		10.0		12.0	ns
t _{SU}	Global clock setup time	(2)	3.7		4.6		6.2		7.4		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	4.2	1.0	5.5	1.0	6.6	ns
t _{CH}	Global clock high time		3.0		3.0		4.0		4.0		ns
t _{CL}	Global clock low time		3.0		3.0		4.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	0.8		1.0		1.4		1.6		ns
t _{AH}	Array clock hold time	(2)	1.9		2.7		4.0		5.1		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	6.2	1.0	7.8	1.0	10.3	1.0	12.4	ns
t _{ACH}	Array clock high time		3.0		3.0		4.0		4.0		ns
t _{ACL}	Array clock low time		3.0		3.0		4.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		3.0		4.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		6.4		8.0		10.7		12.8	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	156.3		125.0		93.5		78.1		MHz
t _{acnt}	Minimum array clock period	(2)		6.4		8.0		10.7		12.8	ns
f _{acnt}	Maximum internal array clock frequency	(2), (4)	156.3		125.0		93.5		78.1		MHz