
Welcome to E-XFL.COM

## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 10 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | 32 |
| Number of Macrocells | 512 |
| Number of Gates | 10000 |
| Number of I/O | 176 |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7512aeqi208-10n |

*Table 1. MAX 7000A Device Features*

| Feature | EPM7032AE | EPM7064AE | EPM7128AE | EPM7256AE | EPM7512AE |
|---|---|---|---|---|---|
| Usable gates | 600 | 1,250 | 2,500 | 5,000 | 10,000 |
| Macrocells | 32 | 64 | 128 | 256 | 512 |
| Logic array blocks | 2 | 4 | 8 | 16 | 32 |
| Maximum user I/O pins | 36 | 68 | 100 | 164 | 212 |
| $t_{PD}$ (ns) | 4.5 | 4.5 | 5.0 | 5.5 | 7.5 |
| $t_{SU}$ (ns) | 2.9 | 2.8 | 3.3 | 3.9 | 5.6 |
| $t_{FSU}$ (ns) | 2.5 | 2.5 | 2.5 | 2.5 | 3.0 |
| $t_{CO1}$ (ns) | 3.0 | 3.1 | 3.4 | 3.5 | 4.7 |
| $f_{CNT}$ (MHz) | 227.3 | 222.2 | 192.3 | 172.4 | 116.3 |

## ...and More Features

- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt™ I/O interface enables device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, and plastic J-lead chip carrier (PLCC) packages
- Supports hot-socketing in MAX 7000AE devices
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- PCI-compatible
- Bus-friendly architecture, including programmable slew-rate control
- Open-drain output option
- Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
- Programmable power-up states for macrocell registers in MAX 7000AE devices
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- 6 to 10 pin- or logic-driven output enable signals
- Two global clock signals with optional inversion
- Enhanced interconnect resources for improved routability
- Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
- Programmable output slew-rate control
- Programmable ground pins

## Expander Product Terms

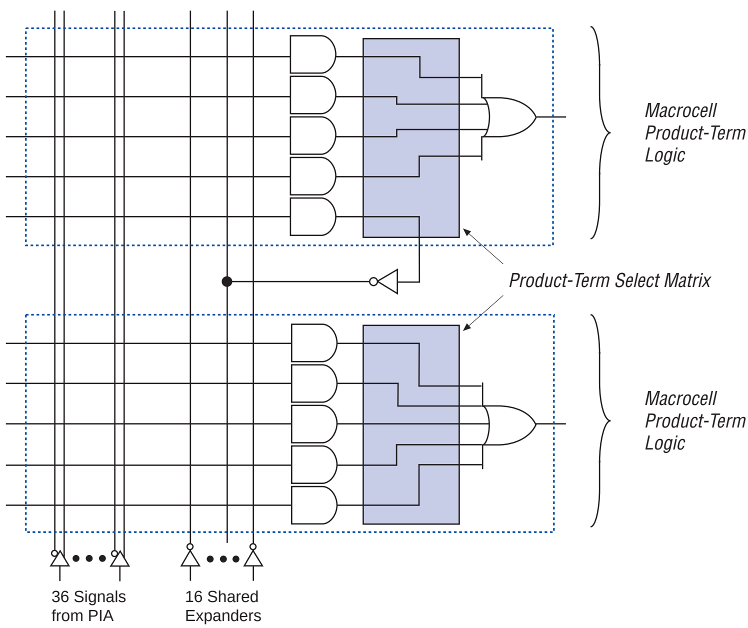
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000A architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

### *Shareable Expanders*

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{SEXP}$) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

***Figure 3. MAX 7000A Shareable Expanders***

*Shareable expanders can be shared by any or all macrocells in an LAB.*



### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders, and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### Programming a Single MAX 7000A Device

The time required to program a single MAX 7000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: $t_{PROG}$ = Programming time
$t_{PPULSE}$ = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
$f_{TCK}$ = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: $t_{VER}$ = Verify time
$t_{VPULSE}$ = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Figure 8 shows timing information for the JTAG signals.

*Figure 8. MAX 7000A JTAG Waveforms*

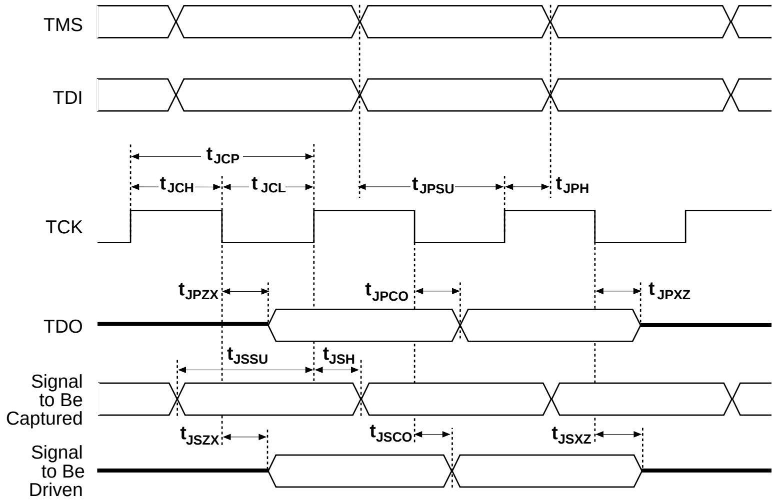



Table 11 shows the JTAG timing parameters and values for MAX 7000A devices.

*Table 11. JTAG Timing Parameters & Values for MAX 7000A Devices Note (1)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 25 | ns |

*Note:*

(1) Timing parameters shown in this table apply for all specified VCCIO levels.

## Power Sequencing & Hot-Socketing

Because MAX 7000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The $V_{CCIO}$ and $V_{CCINT}$ power planes can be powered in any order.

Signals can be driven into MAX 7000AE devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000AE devices do not drive out during power-up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.

MAX 7000AE device I/O pins will not source or sink more than 300 µA of DC current during power-up. All pins can be driven up to 5.75 V during hot-socketing, except the OE1 and GLCRn pins. The OE1 and GLCRn pins can be driven up to 3.6 V during hot-socketing. After $V_{CCINT}$ and $V_{CCIO}$ reach the recommended operating conditions, these two pins are 5.0-V tolerant.

EPM7128A and EPM7256A devices do not support hot-socketing and may drive out during power-up.

## Design Security

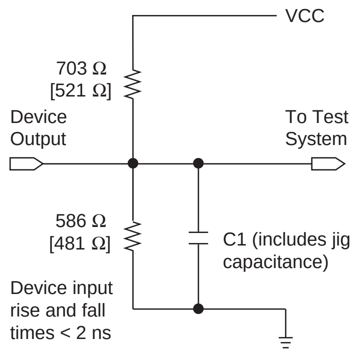
All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

MAX 7000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9. Test patterns can be used and then erased during early stages of the production flow.

***Figure 9. MAX 7000A AC Test Conditions***

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs.*




## Operating Conditions

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000A devices.

***Table 13. MAX 7000A Device Absolute Maximum Ratings*** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_A$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | BGA, FineLine BGA, PQFP, and TQFP packages, under bias | | 135 | ° C |

**Table 15. MAX 7000A Device DC Operating Conditions** *Note (6)*

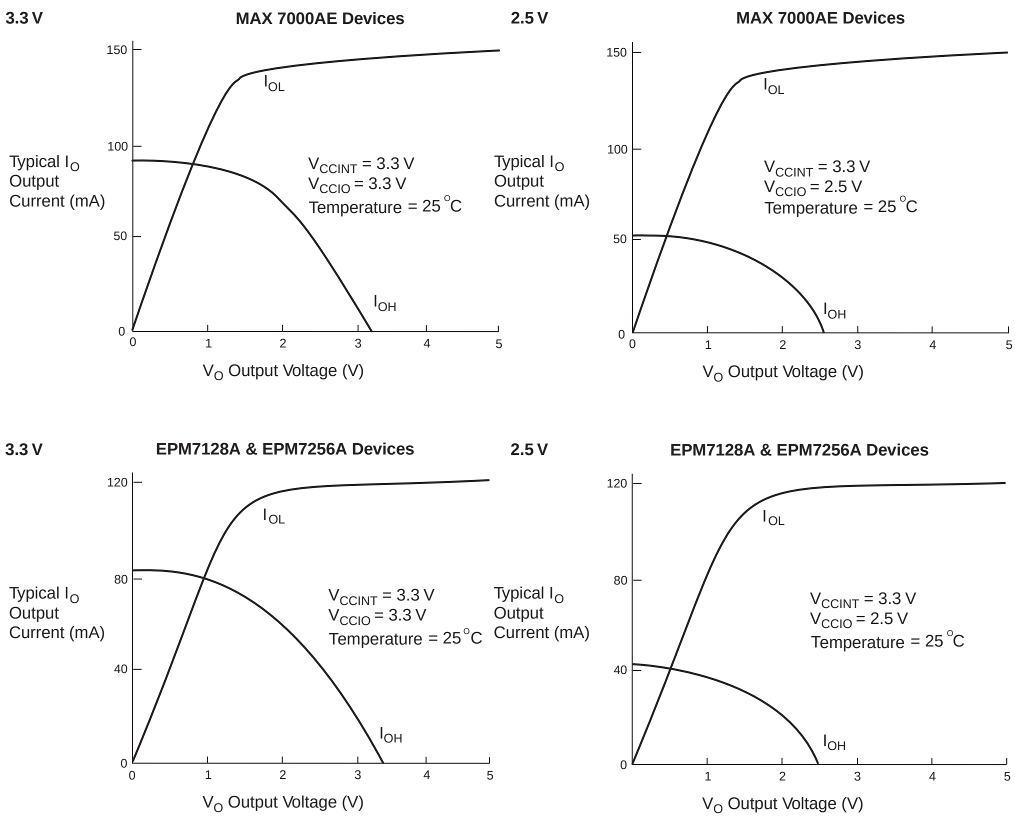
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7 | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | 0.8 | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(7)* | 2.4 | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(7)* | $V_{CCIO}$ – 0.2 | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –100 μA DC, $V_{CCIO}$ = 2.30 V *(7)* | 2.1 | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(7)* | 2.0 | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(7)* | 1.7 | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 8 mA DC, $V_{CCIO}$ = 3.00 V *(8)* | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(8)* | | 0.2 | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 100 μA DC, $V_{CCIO}$ = 2.30 V *(8)* | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(8)* | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(8)* | | 0.7 | V |
| $I_I$ | Input leakage current | $V_I$ = –0.5 to 5.5 V *(9)* | –10 | 10 | μA |
| $I_{OZ}$ | Tri-state output off-state current | $V_I$ = –0.5 to 5.5 V *(9)* | –10 | 10 | μA |
| $R_{ISP}$ | Value of I/O pin pull-up resistor during in-system programming or during power-up | $V_{CCIO}$ = 3.0 to 3.6 V *(10)* | 20 | 50 | kΩ |
| | | $V_{CCIO}$ = 2.3 to 2.7 V *(10)* | 30 | 80 | kΩ |
| | | $V_{CCIO}$ = 2.3 to 3.6 V *(11)* | 20 | 74 | kΩ |

**Table 16. MAX 7000A Device Capacitance** *Note (12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

Figure 10 shows the typical output drive characteristics of MAX 7000A devices.

*Figure 10. Output Drive Characteristics of MAX 7000A Devices*




# Timing Model

MAX 7000A device timing can be analyzed with the Altera software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 11. MAX 7000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

*Table 18. EPM7032AE Internal Timing Parameters (Part 1 of 2) Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -4 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.7 | | 1.2 | | 1.5 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.7 | | 1.2 | | 1.5 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.3 | | 2.8 | | 3.4 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.9 | | 3.1 | | 4.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.5 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.5 | | 2.5 | | 3.3 | ns |
| $t_{LAC}$ | Logic control array delay | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.8 | | 1.3 | | 1.8 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 1.3 | | 1.8 | | 2.3 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.8 | | 6.3 | | 6.8 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 1.3 | | 2.0 | | 2.8 | | ns |
| $t_H$ | Register hold time | | 0.6 | | 1.0 | | 1.3 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.0 | | 1.5 | | 1.5 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.5 | | 1.5 | | 1.5 | | ns |
| $t_{RD}$ | Register delay | | | 0.7 | | 1.2 | | 1.5 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.6 | | 1.0 | | 1.3 | ns |

| *Table 20. EPM7064AE Internal Timing Parameters (Part 1 of 2)* *Note (1)* | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Speed Grade** | | | | | | **Unit** |
| | | | **-4** | | **-7** | | **-10** | | |
| | | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.6 | | 1.1 | | 1.4 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.6 | | 1.1 | | 1.4 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.5 | | 3.0 | | 3.7 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.8 | | 3.0 | | 3.9 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.7 | | 0.9 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.5 | | 2.5 | | 3.2 | ns |
| $t_{LAC}$ | Logic control array delay | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.8 | | 1.3 | | 1.8 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 1.3 | | 1.8 | | 2.3 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.8 | | 6.3 | | 6.8 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 1.3 | | 2.0 | | 2.9 | | ns |
| $t_H$ | Register hold time | | 0.6 | | 1.0 | | 1.3 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.0 | | 1.5 | | 1.5 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.5 | | 1.5 | | 1.5 | | ns |
| $t_{RD}$ | Register delay | | | 0.7 | | 1.2 | | 1.6 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.6 | | 0.9 | | 1.3 | ns |
| $t_{IC}$ | Array clock delay | | | 1.2 | | 1.9 | | 2.5 | ns |

| Table 20. EPM7064AE Internal Timing Parameters (Part 2 of 2) Note (1) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
| | | | -4 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{EN}$ | Register enable time | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.0 | | 1.5 | | 2.2 | ns |
| $t_{PRE}$ | Register preset time | | | 1.3 | | 2.1 | | 2.9 | ns |
| $t_{CLR}$ | Register clear time | | | 1.3 | | 2.1 | | 2.9 | ns |
| $t_{PIA}$ | PIA delay | (2) | | 1.0 | | 1.7 | | 2.3 | ns |
| $t_{LPA}$ | Low-power adder | (6) | | 3.5 | | 4.0 | | 5.0 | ns |

| *Table 26. EPM7512AE Internal Timing Parameters (Part 1 of 2) Note (1)* | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Speed Grade** | | | | | | **Unit** |
| | | | **-7** | | **-10** | | **-12** | | |
| | | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.7 | | 0.9 | | 1.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.7 | | 0.9 | | 1.0 | ns |
| $t_{FIN}$ | Fast input delay | | | 3.1 | | 3.6 | | 4.1 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 2.7 | | 3.5 | | 4.4 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.2 | | 2.8 | | 3.5 | ns |
| $t_{LAC}$ | Logic control array delay | | | 1.0 | | 1.3 | | 1.7 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 1.0 | | 1.5 | | 1.7 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 1.5 | | 2.0 | | 2.2 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 6.0 | | 6.5 | | 6.7 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 5.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(5)* | | 4.5 | | 5.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 9.0 | | 10.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 5.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 2.1 | | 3.0 | | 3.5 | | ns |
| $t_{H}$ | Register hold time | | 0.6 | | 0.8 | | 1.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.6 | | 1.6 | | 1.6 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.4 | | 1.4 | | 1.4 | | ns |
| $t_{RD}$ | Register delay | | | 1.3 | | 1.7 | | 2.1 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.6 | | 0.8 | | 1.0 | ns |

*Table 28. EPM7128A Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -12 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RD}$ | Register delay | | | 1.7 | | 2.1 | | 2.8 | | 3.3 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.7 | | 2.1 | | 2.8 | | 3.3 | ns |
| $t_{IC}$ | Array clock delay | | | 2.4 | | 3.0 | | 4.1 | | 4.9 | ns |
| $t_{EN}$ | Register enable time | | | 2.4 | | 3.0 | | 4.1 | | 4.9 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.0 | | 1.2 | | 1.7 | | 2.0 | ns |
| $t_{PRE}$ | Register preset time | | | 3.1 | | 3.9 | | 5.2 | | 6.2 | ns |
| $t_{CLR}$ | Register clear time | | | 3.1 | | 3.9 | | 5.2 | | 6.2 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 0.9 | | 1.1 | | 1.5 | | 1.8 | ns |
| $t_{LPA}$ | Low-power adder | *(6)* | | 11.0 | | 10.0 | | 10.0 | | 10.0 | ns |

The parameters in this equation are:

| | | |
|---|---|---|
| $MC_{TON}$ | = | Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**) |
| $MC_{DEV}$ | = | Number of macrocells in the device |
| $MC_{USED}$ | = | Total number of macrocells in the design, as reported in the Report File |
| $\mathbf{f_{MAX}}$ | = | Highest clock frequency to the device |
| $\mathbf{tog_{LC}}$ | = | Average percentage of logic cells toggling at each clock (typically 12.5%) |
| A, B, C | = | Constants, shown in Table 31 |

**Table 31. MAX 7000A $I_{CC}$ Equation Constants**

| Device | A | B | C |
|---|---|---|---|
| EPM7032AE | 0.71 | 0.30 | 0.014 |
| EPM7064AE | 0.71 | 0.30 | 0.014 |
| EPM7128A | 0.71 | 0.30 | 0.014 |
| EPM7128AE | 0.71 | 0.30 | 0.014 |
| EPM7256A | 0.71 | 0.30 | 0.014 |
| EPM7256AE | 0.71 | 0.30 | 0.014 |
| EPM7512AE | 0.71 | 0.30 | 0.014 |

This calculation provides an $I_{CC}$ estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual $I_{CC}$ should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 13 shows the typical supply current versus frequency for MAX 7000A devices.

*Figure 13. $I_{CC}$ vs. Frequency for MAX 7000A Devices (Part 1 of 2)*

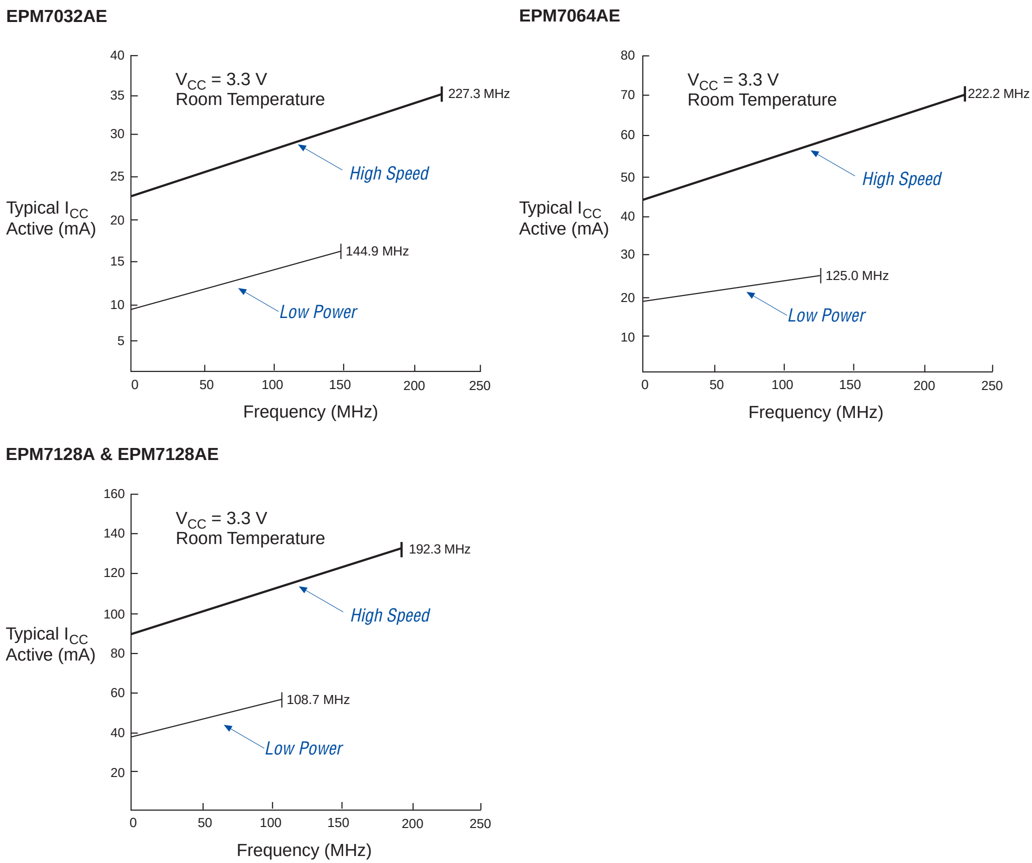
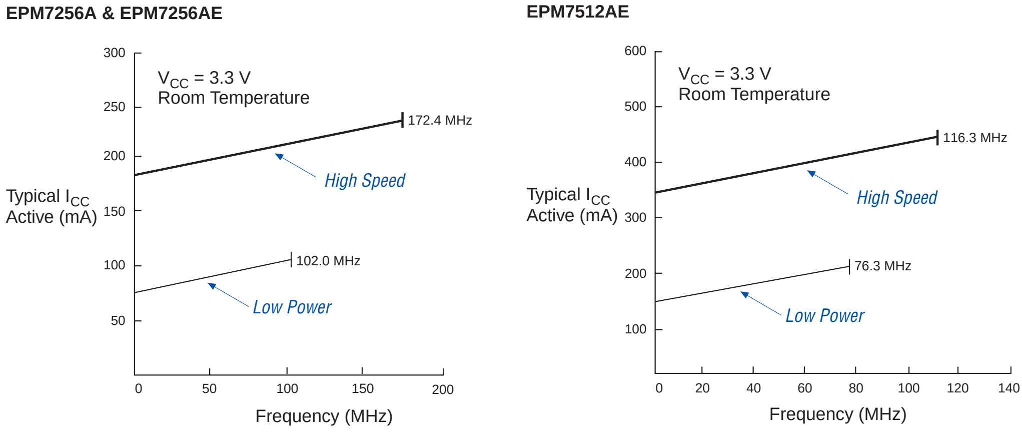


*Figure 13. $I_{CC}$ vs. Frequency for MAX 7000A Devices (Part 2 of 2)*




## Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the ***Altera Digital Library*** for pin-out information.

Figures 14 through 23 show the package pin-out diagrams for MAX 7000A devices.

*Figure 14. 44-Pin PLCC/TQFP Package Pin-Out Diagram*

*Package outlines not drawn to scale.*

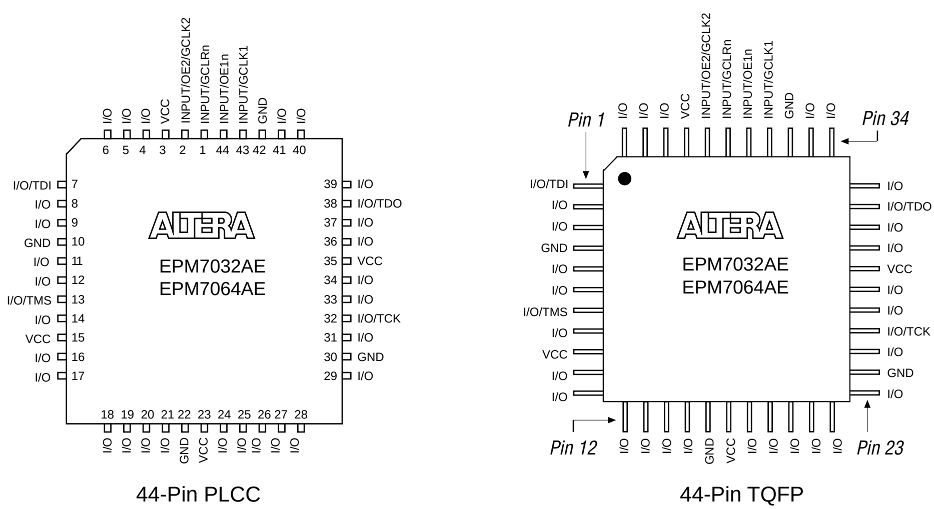


*Figure 19. 144-Pin TQFP Package Pin-Out Diagram*

*Package outline not drawn to scale.*

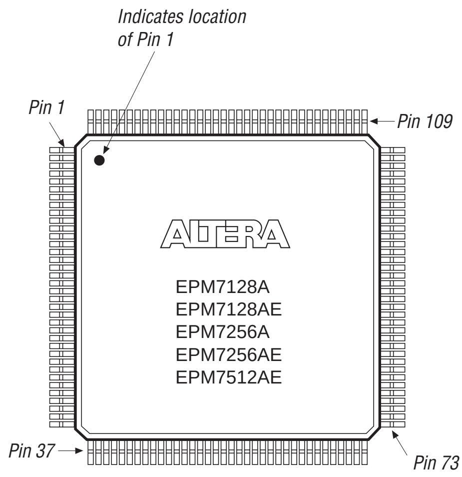



*Figure 20. 169-Pin Ultra FineLine BGA Package Pin-Out Diagram*

*Package outline not drawn to scale.*

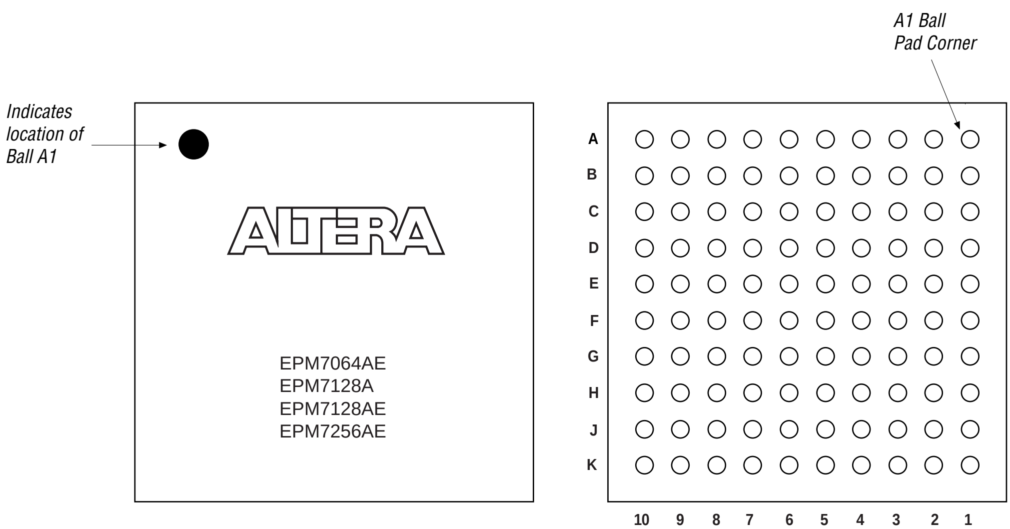


***Figure 23. 256-Pin FineLine BGA Package Pin-Out Diagram***

*Package outline not drawn to scale.*


# Revision History

The information contained in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5 supersedes information published in previous versions.

## Version 4.5

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.5:

- Updated text in the "Power Sequencing & Hot-Socketing" section.

## Version 4.4

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.4:

- Added Tables 5 through 7.
- Added "Programming Sequence" on page 17 and "Programming Times" on page 18.

## Version 4.3

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.3:

- Added extended temperature devices to document
- Updated Table 14.

## Version 4.2

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.2:

- Removed *Note (1)* from Table 2.
- Removed *Note (4)* from Tables 3 and 4.

## Version 4.1

The following changes were made in the *MAX 7000A Programmable Logic Device Data Sheet* version 4.1:

- Updated leakage current information in Table 15.
- Updated *Note (9)* of Table 15.
- Updated *Note (1)* of Tables 17 through 30.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com