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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	88
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12xf512mlm

Table 1-1. Package and Memory Options of MC9S12XF-Family Members

Device	Package	Flash	RAM	EEEPROM
9S12XF512	144 LQFP	512K	32K	4K
	112 LQFP			
	64 LQFP			
9S12XF384	144 LQFP	384K	24K	4K
	112 LQFP			
	64 QFP			
9S12XF256	144 LQFP	256K	20K	2K
	112 LQFP			
	64 QFP			
9S12XF128	144 LQFP	128K	16K	2K
	112 LQFP			
	64 QFP			

2.4.3.3 Stop Mode

All clocks are stopped in STOP mode, dependent of the setting of the PCE, PRE and PSTP bit. The oscillator is disabled in STOP mode unless the PSTP bit is set. If the PRE or PCE bits are set, the RTI or COP continues to run in Pseudo Stop Mode. In addition to disabling system and core clocks the S12XECRG requests other functional units of the MCU (e.g. voltage-regulator) to enter their individual power saving modes (if available).

If the PLLSEL bit is still set when entering Stop Mode, the S12XECRG will switch the system and core clocks to OSCCLK by clearing the PLLSEL bit. Then the S12XECRG disables the IPLL, disables the core clock and finally disables the remaining system clocks.

If Pseudo Stop Mode is entered from Self-Clock Mode the S12XECRG will continue to check the clock quality until clock check is successful. In this case the IPLL and the voltage regulator (VREG) will remain enabled. If Full Stop Mode (PSTP = 0) is entered from Self-Clock Mode the ongoing clock quality check will be stopped. A complete timeout window check will be started when Stop Mode is left again.

There are two ways to restart the MCU from Stop Mode:

1. Any reset
2. Any interrupt

If the MCU is woken-up from Full Stop Mode by an interrupt and the fast wake-up feature is enabled (FSTWKP=1 and SCME=1), the system will immediately (no clock quality check) resume operation in Self-Clock Mode (see Section 2.4.1.4, “Clock Quality Checker”). The SCMIF flag will not be set for this special case. The system will remain in Self-Clock Mode with oscillator disabled until FSTWKP bit is cleared. The clearing of FSTWKP will start the oscillator and the clock quality check. If the clock quality check is successful, the S12XECRG will switch all system clocks to oscillator clock. The SCMIF flag will be set. See application examples in Figure 2-19 and Figure 2-20.

Because the IPLL has been powered-down during Stop Mode the PLLSEL bit is cleared and the MCU runs on OSCCLK after leaving Stop-Mode. The software must manually set the PLLSEL bit again, in order to switch system and core clocks to the PLLCLK.

NOTE

In Full Stop Mode or Self-Clock Mode caused by the fast wake-up feature the clock monitor and the oscillator are disabled.

information will be recorded until the specific ECC fault flag has been cleared. In the event of simultaneous ECC faults, the priority for fault recording is:

1. Double bit fault over single bit fault
2. CPU over XGATE

Offset Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	ECCR[15:8]							
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-20. Flash ECC Error Results High Register (FECCRHI)

Offset Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	ECCR[7:0]							
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-21. Flash ECC Error Results Low Register (FECCRLO)

All FECCR bits are readable but not writable.

Table 8-27. FECCR Index Settings

ECCRIX[2:0]	FECCR Register Content		
	Bits [15:8]	**Bit[7]**	**Bits[6:0]**
000	Parity bits read from Flash block	CPU or XGATE source identity	Global address [22:16]
001	Global address [15:0]		
010	Data 0 [15:0]		
011	Data 1 [15:0] (P-Flash only)		
100	Data 2 [15:0] (P-Flash only)		
101	Data 3 [15:0] (P-Flash only)		
110	Not used, returns 0x0000 when read		
111	Not used, returns 0x0000 when read		

10.4 Functional Description

10.4.1 Flash Command Operations

Flash command operations are used to modify Flash memory contents or configure module resources for EEE operation.

The next sections describe:

- How to write the FCLKDIV register that is used to generate a time base (FCLK) derived from OSCCLK for Flash program and erase command operations
- The command write sequence used to set Flash command parameters and launch execution
- Valid Flash commands available for execution

10.4.1.1 Writing the FCLKDIV Register

Prior to issuing any Flash program or erase command after a reset, the user is required to write the FCLKDIV register to divide OSCCLK down to a target FCLK of 1 MHz. Table 10-9 shows recommended values for the FDIV field based on OSCCLK frequency.

NOTE

Programming or erasing the Flash memory cannot be performed if the bus clock runs at less than 1 MHz. Setting FDIV too high can destroy the Flash memory due to overstress. Setting FDIV too low can result in incomplete programming or erasure of the Flash memory cells.

When the FCLKDIV register is written, the FDIVLD bit is set automatically. If the FDIVLD bit is 0, the FCLKDIV register has not been written since the last reset. If the FCLKDIV register has not been written, any Flash program or erase command loaded during a command write sequence will not execute and the ACCERR bit in the FSTAT register will set.

10.4.1.2 Command Write Sequence

The Memory Controller will launch all valid Flash commands entered using a command write sequence.

Before launching a command, the ACCERR and FPVIOL bits in the FSTAT register must be clear (see Section 10.3.2.7) and the CCIF flag should be tested to determine the status of the current command write sequence. If CCIF is 0, the previous command write sequence is still active, a new command write sequence cannot be started, and all writes to the FCCOB register are ignored.

CAUTION

Writes to any Flash register must be avoided while a Flash command is active (CCIF=0) to prevent corruption of Flash register contents and Memory Controller behavior.

Table 10-32. D-Flash Commands

FCMD	Command	Function on D-Flash Memory
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all D-Flash (and P-Flash) blocks and verifying that all D-Flash (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the D-Flash block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the D-Flash block (special modes only).
0x0F	Full Partition D-Flash	Erase the D-Flash block and partition an area of the D-Flash block for user access.
0x10	Erase Verify D-Flash Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program D-Flash	Program up to four words in the D-Flash block.
0x12	Erase D-Flash Sector	Erase all bytes in a sector of the D-Flash block.
0x13	Enable EEPROM Emulation	Enable EEPROM emulation where writes to the buffer RAM EEE partition will be copied to the D-Flash EEE partition.
0x14	Disable EEPROM Emulation	Suspend all current erase and program activity related to EEPROM emulation but leave current EEE tags set.
0x15	EEPROM Emulation Query	Returns EEE partition and status variables.
0x20	Partition D-Flash	Partition an area of the D-Flash block for user access.

10.4.2 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation will return invalid data. If the SFDIF or DFDIF flags were not previously set when the invalid read operation occurred, both the SFDIF and DFDIF flags will be set and the FECCR registers will be loaded with the global address used in the invalid read operation with the data and parity fields set to all 0.

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 10.3.2.7).

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	VCOFRQ[1:0]		SYNDIV[5:0]					
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-3. CGMIPLL Synthesizer Register (CGMSYNR)

Read: Anytime

Write: Anytime

Writing the CGMSYNR register clears the LOCK status bit.

$$f_{VCO} = 2 \times f_{OSC} \times \frac{(SYNDIV + 1)}{(REFDIV + 1)}$$

$$f_{CGMIPLL} = f_{VCO} \quad \text{(IF DIV2=0)}$$

$$f_{CGMIPLL} = \frac{f_{VCO}}{2} \quad \text{(IF DIV2=1)}$$

NOTE

f_{VCO} must be within the specified VCO frequency lock range. $f_{CGMIPLL}$ must not exceed the specified maximum.

The VCOFRQ[1:0] bit are used to configure the VCO gain for optimal stability and lock time. For correct IPLL operation the VCOFRQ[1:0] bits have to be selected according to the actual target VCOCLK frequency as shown in Table 12-1. Setting the VCOFRQ[1:0] bits wrong can result in a non functional IPLL (no locking and/or insufficient stability).

Table 12-1. VCO Clock Frequency Selection

VCOCLK Frequency Ranges	VCOFRQ[1:0]
32MHz <= f_{VCO}<= 48MHz	00
48MHz < f_{VCO}<= 80MHz	01
Reserved	10
80MHz < f_{VCO} <= 120MHz	11

12.3.2.2 CGMIPLL Reference Divider Register (CGMREFDV)

The REFDV register provides a finer granularity for the IPLL multiplier steps.

ORH — Logical OR Immediate 8 bit Constant (High Byte) — ORH

Operation

RD.H | IMM8 ⇒ RD.H

Performs a bit wise logical OR between the high byte of register RD and an immediate 8 bit constant and stores the result in the destination register RD.H. The low byte of RD is not affected.

CCR Effects

N	Z	V	C
Δ	Δ	0	—

N: Set if bit 15 of the result is set; cleared otherwise.
Z: Set if the 8 bit result is $00; cleared otherwise.
V: 0; cleared.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code							Cycles
ORH RD, #IMM8	IMM8	1	0	1	0	1	RD	IMM8	P

15.1.2.3 Low-Power Modes

The BDM can be used until all bus masters (e.g., CPU or XGATE or others depending on which masters are available on the SOC) are in stop mode. When CPU is in a low power mode (wait or stop mode) all BDM firmware commands as well as the hardware BACKGROUND command can not be used respectively are ignored. In this case the CPU can not enter BDM active mode, and only hardware read and write commands are available. Also the CPU can not enter a low power mode during BDM active mode.

If all bus masters are in stop mode, the BDM clocks are stopped as well. When BDM clocks are disabled and one of the bus masters exits from stop mode the BDM clocks will restart and BDM will have a soft reset (clearing the instruction register, any command in progress and disable the ACK function). The BDM is now ready to receive a new command.

15.1.3 Block Diagram

A block diagram of the BDM is shown in Figure 15-1.

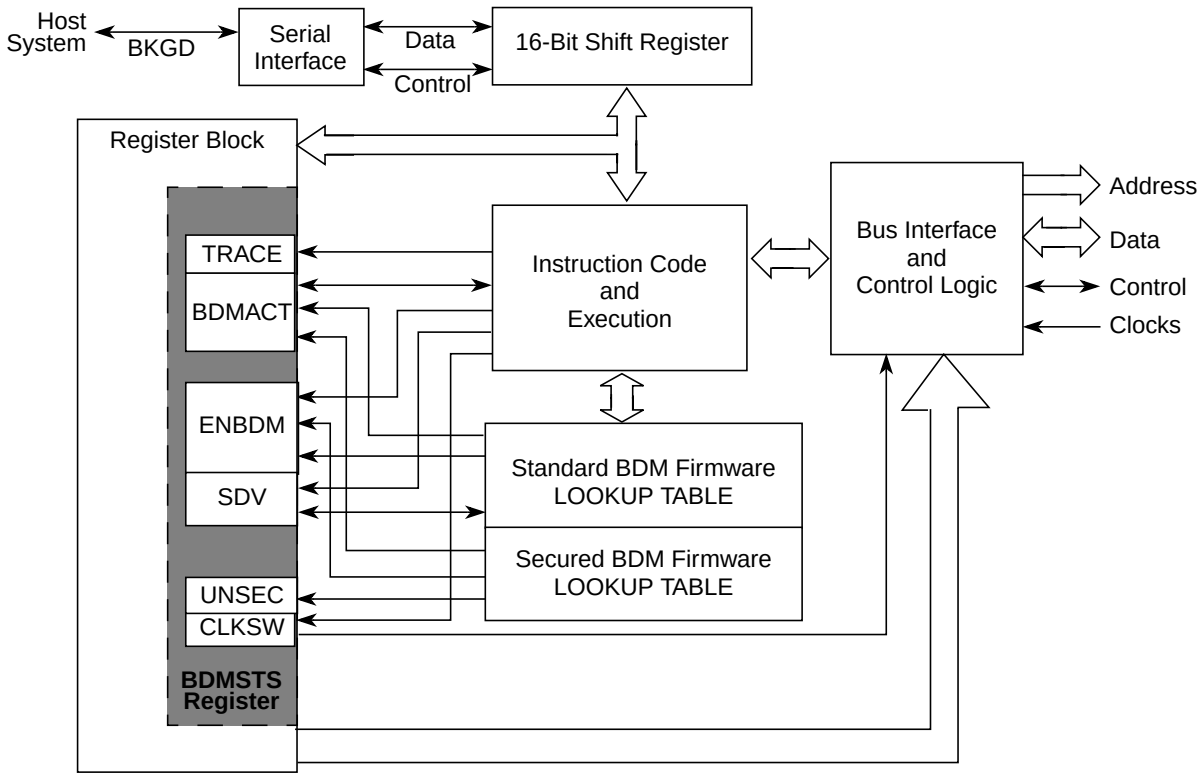

Figure 15-1. BDM Block Diagram

15.2 External Signal Description

A single-wire interface pin called the background debug interface (BKGD) pin is used to communicate with the BDM system. During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the background debug mode.

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x7FFF07	BDMCCRH	R	0	0	0	0	0	CCR10	CCR9	CCR8
		W								
0x7FFF08	BDMGPR	R	BGAE	BGP6	BGP5	BGP4	BGP3	BGP2	BGP1	BGP0
		W								
0x7FFF09	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x7FFF0A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x7FFF0B	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented, Reserved; = Implemented (do not alter)

X = Indeterminate; 0 = Always read zero

Figure 15-2. BDM Register Summary (continued)

15.3.2.1 BDM Status Register (BDMSTS)

Register Global Address 0x7FFF01

	7	6	5	4	3	2	1	0
R	ENBDM	BDMACT	0	SDV	TRACE	CLKSW	UNSEC	0
W								
Reset								
Special Single-Chip Mode	0(1)	1	0	0	0	0	0(3)	0
Emulation Modes (if modes available)	1	0	0	0	0	1(2)	0	0
All Other Modes	0	0	0	0	0	0	0	0

= Unimplemented, Reserved; = Implemented (do not alter)

0 = Always read zero

1. ENBDM is read as 1 by a debugging environment in special single chip mode when the device is not secured or secured but fully erased (non-volatile memory). This is because the ENBDM bit is set by the standard firmware before a BDM command can be fully transmitted and executed.
2. CLKSW is read as 1 by a debugging environment in emulation modes when the device is not secured and read as 0 when secured if emulation modes available.
3. UNSEC is read as 1 by a debugging environment in special single chip mode when the device is secured and fully erased, else it is 0 and can only be read if not secure (see also bit description).

Figure 15-3. BDM Status Register (BDMSTS)

17.3.1.6 MPU Descriptor Register 0 (MPUDESC0)

Address: Module Base + 0x0006

	7	6	5	4	3	2	1	0
R W	MSTR0	MSTR1	MSTR2	MSTR3	LOW_ADDR[22:19]			
Reset	1[1]	1	1	1[2]	0[3]	0[3]	0[3]	0[3]

1. initialized as set for descriptor 0 only, cleared for all others
2. initialized as set for descriptor 0 only, if respective master is implemented on the device
3. These bits are intialized to the lower boundary of the MPU address range by a system reset. Depending on defined descriptor granularity and MPU address range some of these bits may not be writeable.

Figure 17-8. MPU Descriptor Register 0 (MPUDESC0)

Read: Anytime

Write: Anytime

Table 17-8. MPUDESC0 Field Descriptions

Field	Description
7 MSTR0	**Master 0 select bit** — If this bit is set the descriptor is valid for bus master 0 (CPU in supervisor state).
6 MSTR1	**Master 1 select bit** — If this bit is set the descriptor is valid for bus master 1 (CPU in user state). This bit can only be set if the CPU supports user state.
5 MSTR2	**Master 2 select bit** — If this bit is set the descriptor is valid for bus master 2 (XGATE). This bit can only be set if there is an XGATE implemented on the SoC.
4 MSTR3	**Master 3 select bit** — If this bit is set the descriptor is valid for bus master 3 (FlexRay).[1]
3–0 LOW_ADDR [22:19]	**Memory range lower boundary address bits** — The LOW_ADDR[22:19] bits represent bits [22:19] of the global memory address that is used as the lower boundary for the described memory range. These bits are intialized to the lower boundary of the MPU address range by a system reset.

1. Please refer Refernce Guide for information about the availability and function of Master 3 (see 1.9 MPU Configuration).

A descriptor can be configured as valid for more than one bus-master at the same time by setting multiple Master select bits to one. Setting all Master select bits of a descriptor to zero disables the descriptor. Bits for non-implemented masters cannot be written to and always read zero.

17.3.1.7 MPU Descriptor Register 1 (MPUDESC1)

Address: Module Base + 0x0007

	7	6	5	4	3	2	1	0
R W	LOW_ADDR[18:11]							
Reset	0(1)	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

1. These bits are intialized to the lower boundary of the MPU address range by a system reset. Depending on defined descriptor granularity and MPU address range some of these bits may not be writeable.

Figure 17-9. MPU Descriptor Register 1 (MPUDESC1)

Read: Anytime

Write: Anytime

Table 17-9. MPUDESC1 Field Descriptions

Field	Description
7–0 LOW_ADDR[18:11]	**Memory range lower boundary address bits** — The LOW_ADDR[18:11] bits represent bits [18:11] of the global memory address that is used as the lower boundary for the described memory range.hese bits are intialized to the lower boundary of the MPU address range by a system reset.

17.3.1.8 MPU Descriptor Register 2 (MPUDESC2)

Address: Module Base + 0x0008

	7	6	5	4	3	2	1	0
R W	LOW_ADDR[10:3]							
Reset	0(1)	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

1. These bits are intialized to the lower boundary of the MPU address range by a system reset. Depending on defined descriptor granularity and MPU address range some of these bits may not be writeable.

Figure 17-10. MPU Descriptor Register 2 (MPUDESC2)

Read: Anytime

Write: Anytime

Table 17-10. MPUDESC2 Field Descriptions

Field	Description
7–0 LOW_ADDR[10:3]	**Memory range lower boundary address bits** — The LOW_ADDR[10:3] bits represent bits [10:3] of the global memory address that is used as the lower boundary for the described memory range. These bits are intialized to the lower boundary of the MPU address range by a system reset.

Most I/O pins can be configured by register bits to select data direction and drive strength, to enable and select pull-up or pull-down devices.

NOTE

The implementation of the S12XF-family Port Integration Module is device dependent. Therefore some functions are not available on certain derivatives or 112-pin and 64-pin package options.

19.1.2 Features

A full-featured S12XF-family Port Integration Module includes these distinctive registers:

- Data and data direction registers for Ports A, B, C, D, E, K, T, S, M, P, H, J, and AD when used as general-purpose I/O
- Control registers to enable/disable pull-device and select pull-ups/pull-downs on Ports T, S, M, P, H, and J on per-pin basis
- Control registers to enable/disable pull-up devices on Port AD on per-pin basis
- Single control register to enable/disable pull-ups on Ports A, B, C, D, E, and K on per-port basis and on BKGD pin
- Control registers to enable/disable reduced output drive on Ports T, S, M, P, H, J, and AD on per-pin basis
- Single control register to enable/disable reduced output drive on Ports A, B, C, D, E, and K on per-port basis
- Control registers to enable/disable open-drain (wired-or) mode on Ports S and M
- Control register to configure $\overline{\text{IRQ}}$ pin operation
- Free-running clock outputs

A standard port pin has the following minimum features:

- Input/output selection
- 5V output drive with two selectable drive strengths
- 5V digital and analog input
- Input with selectable pull-up or pull-down device

Optional features supported on dedicated pins:

- Open drain for wired-or connections
- Reduced input threshold to support low voltage applications

19.2 External Signal Description

This section lists and describes the signals that do connect off-chip.

Table 19-2 shows all the pins and their functions that are controlled by the S12XFPIMV2. *Refer to the SoC Guide for the availability of the individual pins in the different package options.*

Table 19-10. DDRC Register Field Descriptions

Field	Description
7-0 DDRC	Port C Data Direction— This register controls the data direction of pins 7 through 0. The external bus function controls the data direction for the associated pins. In this case the data direction bits will not change. When operating a pin as a general purpose I/O, the associated data direction bit determines whether it is an input or output. 1 Associated pin is configured as output. 0 Associated pin is configured as high-impedance input.

19.3.10 Port D Data Direction Register (DDRD)

Address 0x0007 (PRR) Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
Reset	0	0	0	0	0	0	0	0

Figure 19-8. Port D Data Direction Register (DDRD)

1. Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.
   Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

Table 19-11. DDRD Register Field Descriptions

Field	Description
7-0 DDRD	**Port D Data Direction**— This register controls the data direction of pins 7 through 0. When used with the external bus this function controls the data direction for the associated pins. In this case the data direction bits will not change. When operating a pin as a general purpose I/O, the associated data direction bit determines whether it is an input or output. 1 Associated pin is configured as output. 0 Associated pin is configured as high-impedance input.

1. Read: Anytime.
   Write:Never, writes to this register have no effect.

Table 19-21. PTIT Register Field Descriptions

Field	Description
7-0 PTIT	**Port T input data**— This register always reads back the buffered state of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

19.3.23 Port T Data Direction Register (DDRT)

Address 0x0242 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset	0	0	0	0	0	0	0	0

Figure 19-21. Port T Data Direction Register (DDRT)

1. Read: Anytime.
   Write: Anytime.

Table 19-22. DDRT Register Field Descriptions

Field	Description
7-0 DDRT	**Port T data direction**— This register controls the data direction of pins 7 through 0. The ECT forces the I/O state to be an output for each timer port associated with an enabled output compare. In this case the data direction bits will not change. The data direction bits revert to controlling the I/O direction of a pin when the associated timer output compare is disabled. The timer Input Capture always monitors the state of the pin. 1 Associated pin is configured as output. 0 Associated pin is configured as high-impedance input.

NOTE

Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTT or PTIT registers, when changing the DDRT register.

19.3.74 Port AD Reduced Drive Register 1 (RDR1AD)

Address 0x0275 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	RDR1AD15	RDR1AD14	RDR1AD13	RDR1AD12	RDR1AD11	RDR1AD10	RDR1AD9	RDR1AD8
Reset	0	0	0	0	0	0	0	0

Figure 19-72. Port AD Reduced Drive Register 1 (RDR1AD)

1. Read: Anytime.
   Write: Anytime.

Table 19-63. RDR1AD Register Field Descriptions

Field	Description
7-0 RDR1AD	**Port AD reduced drive**—Select reduced drive for Port AD outputs This register configures the drive strength of Port AD output pins 7 through 0 as either full or reduced. If a pin is used as input this bit has no effect. 1 Reduced drive selected (1/6 of the full drive strength). 0 Full drive strength enabled.

19.3.75 Port AD Pull Up Enable Register 0 (PER0AD)

Address 0x0276 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PER0AD15	PER0AD14	PER0AD13	PER0AD12	PER0AD11	PER0AD10	PER0AD9	PER0AD8
Reset	0	0	0	0	0	0	0	0

Figure 19-73. Port AD Pull Device Up Register 0 (PER0AD)

1. Read: Anytime.
   Write: Anytime.

Table 19-64. PER0AD Register Field Descriptions

Field	Description
7-0 PER0AD	**Port AD pull device enable**—Enable pull devices on input pins These bits configure whether a pull device is activated, if the associated pin is used as an input. This bit has no effect if the pin is used as an output. Out of reset no pull device is enabled. 1 Pull device enabled. 0 Pull device disabled.

Table 21-12. CANRIER Register Field Descriptions

Field	Description
7 WUPIE[1]	**Wake-Up Interrupt Enable** 0 No interrupt request is generated from this event. 1 A wake-up event causes a Wake-Up interrupt request.
6 CSCIE	**CAN Status Change Interrupt Enable** 0 No interrupt request is generated from this event. 1 A CAN Status Change event causes an error interrupt request.
5-4 RSTATE[1:0]	**Receiver Status Change Enable** — These RSTAT enable bits control the sensitivity level in which receiver state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level the RSTAT flags continue to indicate the actual receiver state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by receiver state changes. 01 Generate CSCIF interrupt only if the receiver enters or leaves "bus-off" state. Discard other receiver state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the receiver enters or leaves "RxErr" or "bus-off"[2] state. Discard other receiver state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
3-2 TSTATE[1:0]	**Transmitter Status Change Enable** — These TSTAT enable bits control the sensitivity level in which transmitter state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level, the TSTAT flags continue to indicate the actual transmitter state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by transmitter state changes. 01 Generate CSCIF interrupt only if the transmitter enters or leaves "bus-off" state. Discard other transmitter state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the transmitter enters or leaves "TxErr" or "bus-off" state. Discard other transmitter state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
1 OVRIE	**Overrun Interrupt Enable** 0 No interrupt request is generated from this event. 1 An overrun event causes an error interrupt request.
0 RXFIE	**Receiver Full Interrupt Enable** 0 No interrupt request is generated from this event. 1 A receive buffer full (successful message reception) event causes a receiver interrupt request.

1. WUPIE and WUPE (see Section 21.3.2.1, "MSCAN Control Register 0 (CANCTL0)") must both be enabled if the recovery mechanism from stop or wait is required.
2. Bus-off state is only defined for transmitters by the CAN standard (see Bosch CAN 2.0A/B protocol specification). Because the only possible state change for the transmitter from bus-off to TxOK also forces the receiver to skip its current state to RxOK, the coding of the RXSTAT[1:0] flags define an additional bus-off state for the receiver (see Section 21.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)").

21.3.2.7 MSCAN Transmitter Flag Register (CANTFLG)

The transmit buffer empty flags each have an associated interrupt enable bit in the CANTIER register.

NOTE

The CANTBSEL register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK=1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 21-17. CANTBSEL Register Field Descriptions

Field	Description
2-0 TX[2:0]	**Transmit Buffer Select** — The lowest numbered bit places the respective transmit buffer in the CANTXFG register space (e.g., TX1 = 1 and TX0 = 1 selects transmit buffer TX0; TX1 = 1 and TX0 = 0 selects transmit buffer TX1). Read and write accesses to the selected transmit buffer will be blocked, if the corresponding TXEx bit is cleared and the buffer is scheduled for transmission (see Section 21.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)"). 0 The associated message buffer is deselected 1 The associated message buffer is selected, if lowest numbered bit

The following gives a short programming example of the usage of the CANTBSEL register:

To get the next available transmit buffer, application software must read the CANTFLG register and write this value back into the CANTBSEL register. In this example Tx buffers TX1 and TX2 are available. The value read from CANTFLG is therefore 0b0000_0110. When writing this value back to CANTBSEL, the Tx buffer TX1 is selected in the CANTXFG because the lowest numbered bit set to 1 is at bit position 1. Reading back this value out of CANTBSEL results in 0b0000_0010, because only the lowest numbered bit position set to 1 is presented. This mechanism eases the application software's selection of the next available Tx buffer.

- LDAA CANTFLG; value read is 0b0000_0110
- STAA CANTBSEL; value written is 0b0000_0110
- LDAA CANTBSEL; value read is 0b0000_0010

If all transmit message buffers are deselected, no accesses are allowed to the CANTXFG registers.

21.3.2.12 MSCAN Identifier Acceptance Control Register (CANIDAC)

The CANIDAC register is used for identifier acceptance control as described below.

Module Base + 0x000B — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 21-15. MSCAN Identifier Acceptance Control Register (CANIDAC)

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1), except bits IDHITx, which are read-only

24.3.2.9 ATD Status Register 2 (ATDSTAT2)

This read-only register contains the Conversion Complete Flags CCF[15:0].

Module Base + 0x000A

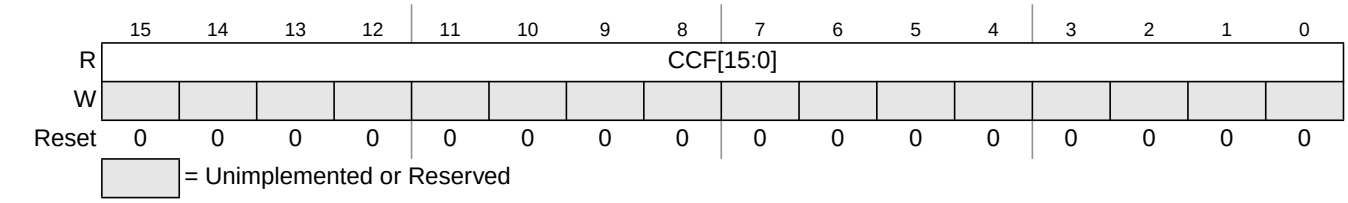

Figure 24-11. ATD Status Register 2 (ATDSTAT2)

Read: Anytime

Write: Anytime, no effect

Table 24-18. ATDSTAT2 Field Descriptions

Field	Description
15–0 CCF[15:0]	**Conversion Complete Flag *n* (*n*= 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0)** — A conversion complete flag is set at the end of each conversion in a sequence. The flags are associated with the conversion position in a sequence (and also the result register number). Therefore in non-fifo mode, CCF[8] is set when the ninth conversion in a sequence is complete and the result is available in result register ATDDR8; CCF[9] is set when the tenth conversion in a sequence is complete and the result is available in ATDDR9, and so forth. If automatic compare of conversion results is enabled (CMPE[*n*]=1 in ATDCMPE), the conversion complete flag is only set if comparison with ATDDR*n* is true and if ACMPIE=1 a compare interrupt will be requested. In this case, as the ATDDR*n* result register is used to hold the compare value, the result will not be stored there at the end of the conversion but is lost. A flag CCF[*n*] is cleared when one of the following occurs: A) Write to ATDCTL5 (a new conversion sequence is started) B) If AFFC=0, write “1” to CCF[*n*] C) If AFFC=1 and CMPE[*n*]=0, read of result register ATDDR*n* D) If AFFC=1 and CMPE[*n*]=1, write to result register ATDDR*n* In case of a concurrent set and clear on CCF[*n*]: The clearing by method A) will overwrite the set. The clearing by methods B) or C) or D) will be overwritten by the set. 0 Conversion number *n* not completed or successfully compared 1 If (CMPE[*n*]=0): Conversion number *n* has completed. Result is ready in ATDDR*n*. If (CMPE[*n*]=1): Compare for conversion result number *n* with compare value in ATDDR*n*, using compare operator CMPGT[*n*] is true. (No result available in ATDDR*n*)

26.2.3 IOC5 — Input Capture and Output Compare Channel 5

This pin serves as input capture or output compare for channel 5.

26.2.4 IOC4 — Input Capture and Output Compare Channel 4

This pin serves as input capture or output compare for channel 4.

26.2.5 IOC3 — Input Capture and Output Compare Channel 3

This pin serves as input capture or output compare for channel 3.

26.2.6 IOC2 — Input Capture and Output Compare Channel 2

This pin serves as input capture or output compare for channel 2.

26.2.7 IOC1 — Input Capture and Output Compare Channel 1

This pin serves as input capture or output compare for channel 1.

26.2.8 IOC0 — Input Capture and Output Compare Channel 0

This pin serves as input capture or output compare for channel 0.

NOTE

For the description of interrupts see Section 26.4.3, “Interrupts”.

26.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

26.3.1 Module Memory Map

The memory map for the ECT module is given below in the Table 26-2. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the ECT module and the address offset for each register.

26.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Table A-7. 5-V I/O Characteristics

Conditions are 4.5 V < V_{DD35} < 5.5 V temperature from –40°C to +150°C, unless otherwise noted I/O Characteristics for all I/O pins except EXTAL, XTAL,TEST and supply pins.							
16	D	Port H, J, P interrupt input pulse passed ($\overline{STOP}$)	t_{PULSE}	4	—	—	tcyc
17	D	$\overline{IRQ}$ pulse width, edge-sensitive mode ($\overline{STOP}$)	PW_{IRQ}	1	—	—	tcyc
18	D	$\overline{XIRQ}$ pulse width with X-bit set (STOP)	PW_{XIRQ}	4	—	—	tosc

1. Maximum leakage current occurs at maximum operating temperature.
2. Refer to Section A.1.4, “Current Injection” for more details
3. Parameter only applies in stop or pseudo stop mode.