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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, FlexRay, I ² C, LINbus, SPI
Peripherals	DMA, I ² S, POR, WDT
Number of I/O	-
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 36x10b, 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	100-MAPBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5744bk1cmh2r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Debug functionality
 - e200z2 core:NDI per IEEE-ISTO 5001-2008 Class3+
 - e200z4 core: NDI per IEEE-ISTO 5001-2008 Class 3+
- Timer
 - 16 Periodic Interrupt Timers (PITs)
 - Two System Timer Modules (STM)
 - Three Software Watchdog Timers (SWT)
 - 64 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels
- Device/board boundary Scan testing supported with Joint Test Action Group (JTAG) of IEEE 1149.1 and IEEE 1149.7 (CJTAG)
- Security
 - Hardware Security Module (HSMv2)
 - Password and Device Security (PASS) supporting advanced censorship and life-cycle management
 - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Functional Safety
 - ISO26262 ASIL-B compliance
- Multiple operating modes
 - Includes enhanced low power operation

3.2 Ordering Information

Example	Code	PC 57	4	6	С	Ş	К0	М	MJ	6	R
·	Qualification Status								1	1	1
	Power Architecture										
	Automotive Platform										
	Core Version										
Flas	sh Size (core dependent)										
	Product										
	Optional fields										
	Fab and mask indicator										
	Temperature spec.										
	Package Code]		
	CPU Frequency										
R = Ta	pe & Reel (blank if Tray)										
	Due due 6 Manual au		-				D -	- 1	0		
Qualification Status	Product version	Fab and i	nask v Sab	versic	on indi	icator	Pa	CKage		ED	
S = Automotive qualified	B = Single core	#(0.1 etc.)) = Ver	sion o	f the		M.	J = 170 J = 250	6 MAPB	GA	
	C = Dual core	maskset.	like rev	v. 0=0	N65H		M	N = 32	4 MAPE	GA	
PC = Power Architecture		maeneeu,					Μ	H = 10	OMAPB	GA	
Automotive Platform		Temperat	ure sp	bec.			СР	U Fre	quency		
57 = Power Architecture in 55nm	Omtion of tiolds	C = -40.C	to +85	5.C Ta			2 =	- 74 0	nerates	unto	120 MHz
	Optional fields	V = -40.C	to +10)5.C T	a		6-	74 01	nerates	unto	160 MHz
Core Version	Blank = No optional feature	M = -40.C	to +12	25.0	a		0 -		sciales	upto	100 1012
4 = e200z4 Core version (highest	S = HSM (Security Module)										
cores)	F = CAN FD										
,	B = HSM + CAN FD						Sh	ipping	Metho	d	
Flash Memory Size	R = 512K RAM						H =	= lape	and ree		
4 = 1.5 MB	T = HSM + 512K RAM						Dia		lay		
5 = 2 MB	G* = CAN FD + 512K RAM										
6 = 3 MB	H* = HSM + CAN FD + 512K RAM										
	[•] G and H for 5746 B/C only										
Note: Not all part number con	nbinations are available as produ	ction produ	ıct								
		enon prout									

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in Table 5 for specific conditions

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Symbol	Parameter	Conditions ¹	Min	Max	Unit
$\begin{matrix} V_{DD_HV_A}, V_{DD_HV_B}, \\ V_{DD_HV_C}^{2,3} \end{matrix}$	3.3 V - 5. 5V input/output supply voltage		-0.3	6.0	V
V _{DD_HV_FLA} ^{4, 5}	3.3 V flash supply voltage (when supplying from an external source in bypass mode)		-0.3	3.63	V
V _{DD_LP_DEC} ⁶	Decoupling pin for low power regulators ⁷		-0.3	1.32	V
V _{DD_HV_ADC1_REF} ⁸	3.3 V / 5.0 V ADC1 high reference voltage		-0.3	6	V
V _{DD_HV_ADC0}	3.3 V to 5.5V ADC supply voltage	—	-0.3	6.0	V
V _{DD_HV_ADC1}					
V _{SS_HV_ADC0}	3.3V to 5.5V ADC supply ground	—	-0.1	0.1	V
V _{SS_HV_ADC1}					
V _{DD_LV} ^{9, 10, 10, 11, 11, 12}	Core logic supply voltage		-0.3	1.32	V
V _{INA}	Voltage on analog pin with respect to ground (V _{SS_HV})	_	-0.3	Min (V _{DD_HV_x} , V _{DD_HV_ADCx} , V _{DD_ADCx_REF}) +0.3	V
V _{IN}	Voltage on any digital pin with respect to ground (V _{SS_HV})	Relative to V _{DD_HV_A} , V _{DD_HV_B} , V _{DD_HV_C}	-0.3	V _{DD_HV_x} + 0.3	V
I _{INJPAD}	Injected input current on any pin during overload condition	Always	-5	5	mA
I _{INJSUM}	Absolute sum of all injected input currents during overload condition		-50	50	mA
T _{ramp}	Supply ramp rate		0.5 V / min	100V/ms	—
T _A ¹³	Ambient temperature		-40	125	°C
T _{STG}	Storage temperature	_	-55	165	°C

Table 5.	Absolute	maximum	ratings
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- 1. All voltages are referred to VSS_HV unless otherwise specified
- 2. VDD_HV_B and VDD_HV_C are common together on the 176 LQFP-EP package.
- Allowed V_{DD_HV_x} = 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J= 150 °C, remaining time at or below 5.5 V.
- 4. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
- 5. VDD_HV_FLA must be disconnected from ANY power sources when VDD_HV_A = 5V
- 6. This pin should be decoupled with low ESR 1 μ F capacitor.
- 7. Not available for input voltage, only for decoupling internal regulators
- 8. 10-bit ADC does not have dedicated reference and its reference is bonded to 10-bit ADC supply(VDD_HV_ADC0) inside the package.
- Allowed 1.45 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C, remaining time as defined in footnotes 10 and 11.
- 10. Allowed 1.38 1.45 V- for 10 hours cumulative time at maximum T_J = 150 °C, remaining time as defined in footnote 11.
- 11. 1.32 1.38 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.326 V at maximum T_J = 150 °C.
- 12. If HVD on core supply (V_{HVD LV x}) is enabled, it will generate a reset when supply goes above threshold.
- 13. $T_J=150^{\circ}C$. Assumes $T_A=125^{\circ}C$
 - Assumes maximum θJA for 2s2p board. See Thermal attributes





Figure 2. Voltage regulator capacitance connection

NOTE

On BGA, VSS_LV and VSS_HV have been joined on substrate and renamed as VSS.

Table 8.	Voltage regulator	electrical	specifications
	U U		-

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{fp_reg} 1	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2 ²	3	μF
	Combined ESR of external capacitor	_	0.001	_	0.03	Ohm
C _{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	μF
	Combined ESR of external capacitor	_	0.001	—	0.1	Ohm
C _{be_fpreg} ³	Capacitor in parallel to base-	BCP68 and BCP56		3.3		nF
	emitter	MJD31		4.7		

Table continues on the next page ...

General

Symbol	Parameter	Conditions ¹	Min	Тур	Max	Unit
IDD_HV_ADC_REF ^{10,}	ADC REF Operating current	T _a = 125 °C ⁵		200	400	μA
11, 11		2 ADCs operating at 80 MHz				
		$V_{DD_{HV}ADC_{REF}} = 5.5 V$				
		T _a = 105 °C	_	200	_	
		2 ADCs operating at 80 MHz				
		$V_{DD_HV_ADC_REF} = 5.5 V$				
		T _a = 85 °C	_	200	_	
		2 ADCs operating at 80 MHz				
		$V_{DD_{HV}ADC_{REF}} = 5.5 V$				
		T _a = 25 °C	_	200	_	
		2 ADCs operating at 80 MHz				
		$V_{DD_{HV}ADC_{REF}} = 3.6 V$				
I _{DD_HV_ADCx} ¹¹	ADC HV Operating current	T _a = 125 °C ⁵	-	1.2	2	mA
		ADC operating at 80 MHz				
		$V_{DD_HV_ADC} = 5.5 V$				
		T _a = 25 °C	—	1	2	
		ADC operating at 80 MHz				
		$V_{DD_HV_ADC} = 3.6 V$				
IDD_HV_FLASH ¹²	Flash Operating current during read	T _a = 125 °C ⁵	—	40	45	mA
	access	3.3 V supplies				
		160 MHz frequency				
		T _a = 105 °C	—	40	45	
		3.3 V supplies				
		160 MHz frequency				
		T _a = 85 °C	—	40	45	
		3.3 V supplies				
		160 MHz frequency				

Table 10. Current consumption characteristics (continued)

- 1. The content of the Conditions column identifies the components that draw the specific current.
- Single e200Z4 core cache disabled @80 MHz, no FlexRay, no ENET, 2 x CAN, 8 LINFlexD, 2 SPI, ADC0 and 1 used constantly, no HSM, Memory: 2M flash, 128K RAM RUN mode, Clocks: FIRC on, XOSC, PLL on, SIRC on for TOD, no 32KHz crystal (TOD runs off SIRC).
- 3. Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C. In case of internal ballast mode, it is expected that the external ballast is not mounted and BAL_SELECT_INT pin is tied to VDD_HV_A supply on board. Internal ballast can be used for all use cases with current consumption upto 150mA
- 4. The power consumption does not consider the dynamic current of I/Os
- 5. Tj=150°C. Assumes Ta=125°C
 - Assumes maximum θJA of 2s2p board. SeeThermal attributes
- e200Z4 core, 160MHz, cache enabled; e200Z2 core, 80MHz, no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 256K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
- e200Z4 core, 120MHz, cache enabled; e200Z2 core, 60MHz; no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 128K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal

General

Symbol	Parameter	Conditions ¹	Min	Тур	Max	Unit
STANDBY2	STANDBY with	T _a = 25 °C	_	75	_	μA
	128K RAM	T _a = 85 °C	—	155	730	
		T _a = 105 °C	—	255	1350	
		$T_a = 125 \ ^{\circ}C^{2}$	—	396	2600	
STANDBY3	STANDBY with	$T_a = 25 \text{ °C}$	—	80	_	μA
	256K RAM	T _a = 85 °C	—	180	800	
		T _a = 105 °C	—	290	1425	
		$T_{a} = 125 \ ^{\circ}C^{2}$	—	465	2900	
STANDBY3	FIRC ON	T _a = 25 °C	—	500	—	μA

Table 12. STANDBY Current consumption characteristics (continued)

1. The content of the Conditions column identifies the components that draw the specific current.

 Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts \times (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Symbol	Parameter	Conditions ¹	Class	Max value ²	Unit
V _{ESD(HBM)}	Electrostatic discharge	T _A = 25 °C	H1C	2000	V
	(Human Body Model)	conforming to AEC- Q100-002			
V _{ESD(CDM)}	Electrostatic discharge	T _A = 25 °C	C3A	500	V
	(Charged Device Model)	conforming to AEC- Q100-011		750 (corners)	

Table 13. ESD ratings

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2. Data based on characterization results, not tested in production.

Peripheral operating requirements and behaviours

Symbol	Parameter Conditions			Value		Unit
			Min	Тур	Max	1
V _{HYS}	CMOS Input Buffer hysterisis	—	300	—	—	mV
V _{DD_POR}	Minimum supply for strong pull-down activation	—	_	-	1.2	V
I _{OL_R}	Strong pull-down current ^{1, 1}	Device under power-on reset	0.2	—	-	mA
		$V_{DD_HV_A} = V_{DD_POR}$				
		$V_{OL} = 0.35^* V_{DD_HV_A}$				
		Device under power-on reset	11	—	-	mA
		$V_{DD_HV_A} = V_{DD_POR}$				
		$V_{OL} = 0.35^* V_{DD_HV_IO}$				
W _{FRST}	RESET input filtered pulse	—	—	—	500	ns
W _{NFRST}	RESET input not filtered pulse		2000	_	_	ns
ll _{WPU} l	Weak pull-up current absolute value	RESET pin V _{IN} = V _{DD}	23	_	82	μA

 Table 18.
 Functional reset pad electrical specifications (continued)

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter		Unit		
		Min	Тур	Max	1
W _{FPORST}	PORST input filtered pulse	_	_	200	ns
W _{NFPORST}	PORST input not filtered pulse	1000	_	—	ns
V _{IH}	Input high level	0.65 x V _{DD_HV_A}	_	—	V
V _{IL}	Input low level		_	0.35 x V _{DD_HV_A}	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
R _{AD} ⁶	Internal resistance of analog source	—	_	_	825	Ω
INL	Integral non-linearity (precise channel)	—	-2	_	2	LSB
INL	Integral non-linearity (standard channel)	—	-3	—	3	LSB
DNL	Differential non-linearity	—	-1	—	1	LSB
OFS	Offset error	—	-6	—	6	LSB
GNE	Gain error	—	-4	—	4	LSB
ADC Analog Pad	Max leakage (precision channel)	150 °C	_		250	nA
(pad going to one	Max leakage (standard channel)	150 °C	—	—	2500	nA
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Max leakage (standard channel)	105 °C _{TA}	—	5	250	nA
	Max positive/negative injection		-5		5	mA
TUEprecision channels	Total unadjusted error for precision	Without current injection	-6	+/-4	6	LSB
	channels	With current injection ^{7, 7}		+/-5		LSB
TUE _{standard/extended}	Total unadjusted error for standard/	Without current injection	-8	+/-6	8	LSB
channels	extended channels	With current injection ⁷		+/-8		LSB
t _{recovery}	STOP mode to Run mode recovery time				< 1	μs

Table 20. ADC conversion characteristics (for 12-bit) (continued)

- Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
- 2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal
 resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the
 sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample
 clock t_{sample} depend on programming.
- This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
- 5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
- 6. See Figure 6.
- 7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
fск	f _{CK} ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK ² frequency.)		15.2	80	80	MHz
f _s	Sampling frequency	_	—	—	1.00	MHz
t _{sample} Sample time ³		80 MHz@ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
t _{conv}	Conversion time ⁴	80 MHz	550	—	—	ns
t _{total_conv}	Total Conversion time tsample + tconv (for standard channels)	80 MHz	1			μs
	Total Conversion time tsample + tconv (for extended channels)		1.5	_		
C _S ⁵	ADC input sampling capacitance	—	_	3	5	pF
C _{P1} ⁵	ADC input pin capacitance 1	—	_	—	5	pF
C _{P2} ⁵	ADC input pin capacitance 2	—		—	0.8	pF
R _{SW1} ⁵	Internal resistance of analog	V_{REF} range = 4.5 to 5.5 V	_	—	0.3	kΩ
	source	V_{REF} range = 3.15 to 3.6 V	_	—	875	Ω
R _{AD} ⁵	Internal resistance of analog source	_	—	_	825	Ω
INL	Integral non-linearity	—	-2	—	2	LSB
DNL	Differential non-linearity	—	-1	—	1	LSB
OFS	Offset error	—	-4	—	4	LSB
GNE	Gain error	—	-4	—	4	LSB
ADC Analog Pad	Max leakage (standard channel)	150 °C		—	2500	nA
(pad going to one	Max positive/negative injection		-5	—	5	mA
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Max leakage (standard channel)	105 °C _{TA}		5	250	nA
TUE _{standard/extended}	Total unadjusted error for standard	Without current injection	-4	+/-3	4	LSB
channels	channels	With current injection ⁶		+/-4		LSB
t _{recovery}	STOP mode to Run mode recovery time				< 1	μs

 Table 21. ADC conversion characteristics (for 10-bit) (continued)

- Active ADC Input, VinA < [min(ADC_ADV, IO_Supply_A,B,C)]. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO_supply_A, B, C and ADC_Supply.
- 2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal
 resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the
 sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample
 clock t_{sample} depend on programming.
- 4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
- 5. See Figure 65
- 6. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

6.1.2 Analog Comparator (CMP) electrical specifications Table 22. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
I _{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	_	—	250	μA
I _{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	_	5	11	μA
V _{AIN}	Analog input voltage	V_{SS}	_	V _{IN1_CMP_RE} F	V
V _{AIO}	Analog input offset voltage ^{1, 1}	-47	_	47	mV
V _H	Analog comparator hysteresis ^{2, 2}	_	1	25	mV
	• CR0[HYSTCTR] = 00	_	20	50	mV
	• CR0[HYSTCTR] = 01	_	40	70	mV
	• CR0[HYSTCTR] = 10	_	60	105	mV
	• CR0[HYSTCTR] = 11			100	
t _{DHS}	Propagation Delay, High Speed Mode (Full Swing) ^{1,} 3, 3	_	_	250	ns
t _{DLS}	Propagation Delay, Low power Mode (Full Swing) ^{1, 3}	_	5	21	μs
	Analog comparator initialization delay, High speed mode ^{4, 4}	_	4		μs
	Analog comparator initialization delay, Low speed mode ⁴	_	100		μs
I _{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	_	6	9	μA
	5V Reference Voltage		10	16	μΑ
INL	6-bit DAC integral non-linearity	-0.5		0.5	LSB ⁵
DNL	6-bit DAC differential non-linearity	-0.8		0.8	LSB

1. Measured with hysteresis mode of 00

2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD_{-HV_{-}A}}$ -0.6V

3. Full swing = VIH, VIL

4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.

5. 1 LSB = $V_{reference}/64$

Type of jitter	Jitter due to Supply Noise (ps) J _{SN} ¹	Jitter due to Fractional Mode (ps) J _{SDM} ²	Jitter due to Fractional Mode J _{SSCG} (ps) ³	1 Sigma Random Jitter J _{RJ} (ps) ⁴	Total Period Jitter (ps)
Long Term Jitter (Integer Mode)				40	+/-(N x J _{RJ})
Long Term jitter (Fractional Mode)				100	+/-(N x J _{RJ})

Table 28. Jitter calculation (continued)

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on VDD_LV and VSS_LV.

2. This jitter component is added when the PLL is working in the fractional mode.

3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.

4. The value of N is dependent on the accuracy requirement of the application. See Table 29

Table 29. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27
4	6.30 × 1e-03
5	5.63 × 1e-05
6	2.00 × 1e-07
7	2.82 × 1e-10

6.3 Memory interfaces

6.3.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.

6.4 Communication interfaces

6.4.1 DSPI timing

Table 35. DSPI electrical specifications

No	Symbol	Parameter	Conditions	High Speed Mode		low Spe	ed mode	Unit
				Min	Мах	Min	Max	1
1	t _{SCK}	DSPI cycle	Master (MTFE = 0)	25	_	50		ns
		time	Slave (MTFE = 0)	40	_	60	_	1
2	t _{csc}	PCS to SCK delay	_	16	_	_	_	ns
3	t _{ASC}	After SCK delay	_	16	_	_	_	ns
4	t _{SDC}	SCK duty cycle		t _{SCK} /2 - 10	t _{SCK} /2 + 10	_	_	ns
5	t _A	Slave access time	SS active to SOUT valid		40	—	_	ns
6	t _{DIS}	Slave SOUT disable time	_{SS} inactive to SOUT High-Z or invalid		10	_	-	ns
7	t _{PCSC}	PCSx to PCSS time	_	13	_	_	-	ns
8	t _{PASC}	PCSS to PCSx time	_	13	_	_	_	ns
9	t _{SUI}	Data setup	Master (MTFE = 0)	NA	—	20	—	ns
		time for	Slave	2	—	2	_	1
		inputo	Master (MTFE = 1, CPHA = 0)	15	_	8 ^{1, 1}	_	
			Master (MTFE = 1, CPHA = 1)	15	_	20	_	
10	t _{HI}	Data hold	Master (MTFE = 0)	NA	—	-5	_	ns
		time for	Slave	4	—	4	_	
		inputo	Master (MTFE = 1, CPHA = 0)	0	_	11 ¹	_	
			Master (MTFE = 1, CPHA = 1)	0	_	-5	-	
11	t _{SUO}	Data valid	Master (MTFE = 0)	_	NA	_	4	ns
		(after SCK	Slave	_	15	—	23	1
		cuge)	Master (MTFE = 1, CPHA = 0)		4	_	16 ¹	
			Master (MTFE = 1, CPHA = 1)	—	4	—	4	1

Table continues on the next page...



Figure 10. DSPI classic SPI timing — slave, CPHA = 0



Figure 11. DSPI classic SPI timing — slave, CPHA = 1

FlexRay electrical specifications

no	Parameter	Va	Value			
		Min	Мах			
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period		
S3	SAI_BCLK cycle time	80	-	BCLK period		
S4	SAI_BCLK pulse width high/low	45%	55%	ns		
S5	SAI_BCLK to SAI_FS output valid	-	15	ns		
S6	SAI_BCLK to SAI_FS output invalid	0	-	ns		
S7	SAI_BCLK to SAI_TXD valid	-	15	ns		
S8	SAI_BCLK to SAI_TXD invalid	0	-	ns		
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	28	-	ns		
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	-	ns		

Table 43. Master mode SAI Timing (continued)





Table 44.	Slave	mode	SAI	Timing
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No	Parameter	Value		Unit
		Min	Мах	
	Operating Voltage	2.7	3.6	V
S11	SAI_BCLK cycle time (input)	80	-	ns
S12	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	-	ns
S14	SAI_FS input hold after SAI_BCLK	2	-	ns

Table continues on the next page...





Figure 27. JTAG boundary scan timing

6.5.2 Nexus timing

Table 46. Nexus debug port timing 1

No.	Symbol	Parameter	Condition	Min	Max	Unit
			S			
1	t _{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t _{MDC}	MCKO Duty Cycle	—	40	60	%
3	t _{MDOV}	MCKO Low to MDO, MSEO, EVTO Data Valid ²	—	-0.1	0.25	tMCYC
4	t _{EVTIPW}	EVTI Pulse Width	—	4	—	tTCYC
5	t _{EVTOPW}	EVTO Pulse Width	—	1	—	tMCYC
6	t _{TCYC}	TCK Cycle Time ³	—	62.5	—	ns
7	t _{TDC}	TCK Duty Cycle	—	40	60	%
8	t _{NTDIS} , t _{NTMSS}	TDI, TMS Data Setup Time	_	8	_	ns

Table continues on the next page...

Table 46. Nexus debug port timing ¹ (continued)

No.	Symbol	Parameter	Condition s	Min	Max	Unit
9	t _{NTDIH} , t _{NTMSH}	TDI, TMS Data Hold Time	_	5	_	ns
10	t _{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.

- 2. For all Nexus modes except DDR mode, MDO, MSEO, and EVTO data is held valid until next MCKO low cycle.
- 3. The system clock frequency needs to be four times faster than the TCK frequency.



Figure 28. Nexus output timing



Figure 29. Nexus EVTI Input Pulse Width

Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Four-layer (2s2p)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	17.8	°C/W	1, 3
_	R _{θJB}	Thermal resistance, junction to board	10.9	°C/W	44
_	R _{θJC}	Thermal resistance, junction to case	8.4	°C/W	55
_	Ψ _{JT}	Thermal resistance, junction to package top	0.5	°C/W	66
_	Ψ _{JB}	Thermal characterization parameter, junction to package bottom	0.3	°C/W	77

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal.
- 4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
- 7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	31.0	°C/W	11, 22
Four-layer (2s2p)	R _{0JA}	Thermal resistance, junction to ambient (natural convection)	24.3	°C/W	1,2,33
Single-layer (1s)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	23.5	°C/W	1, 3
Four-layer (2s2p)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	20.1	°C/W	1,3

Table continues on the next page...

Board type	Symbol	Description	100 MAPBGA	Unit	Notes
_	R _{θJB}	Thermal resistance, junction to board	10.8	°C/W	44
_	R _{θJC}	Thermal resistance, junction to case	8.2	°C/W	55
	Ψ _{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	66
_	Ψ _{JB}	Thermal characterization parameter, junction to package bottom outside center (natural convection)	7.8	°C/W	77

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal
- 4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
- 7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

Package	NXP Document Number
100 MAPBGA	98ASA00802D

Table continues on the next page...

Pinouts

Package	NXP Document Number
176-pin LQFP-EP	98ASA00698D
256 MAPBGA	98ASA00346D
324 MAPBGA	98ASA10582D

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

10.1 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1.1 Reset sequence duration

Table 49 specifies the reset sequence duration for the five different reset sequences described in Reset sequence description.

No.	Symbol	Parameter	T _{Reset}		Unit	
			Min	Тур 1, 1	Max	
1	T _{DRB}	Destructive Reset Sequence, BIST enabled	6.2	7.3	-	ms
2	T _{DR}	Destructive Reset Sequence, BIST disabled	110	182	-	us
3	T _{ERLB}	External Reset Sequence Long, Unsecure Boot	6.2	7.3	-	ms
4	T _{FRL}	Functional Reset Sequence Long, Unsecure Boot	110	182	-	us
5	T _{FRS}	Functional Reset Sequence Short, Unsecure Boot	7	9	-	us

Table 49. RESET sequences

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

Table 51. Revision History (continue

Rev. No.	Date	Substantial Changes		
Rev 4	9 March 2016	 In section, Voltage regulator electrical characteristics In table, Voltage regulator electrical specifications: Updated the footnote on V_{DD-HV_BALLAST} 		
Rev 5	27 February 2017	 In Family Comparison section: Updated the "MPC5746C Family Comparison" table. added "NVM Memory Map 1", "NVM Memory Map 2", and "RAM Memory Map" tables. 		
		 Updated the product version, flash memory size and optional fields information in Ordering Information section. 		
		 In Recommended Operating Conditions section, removed the note related to additional crossover current. 		
		 VDD_HV_C row added in "Voltage regulator electrical specifications" table in Voltage regulator electrical characteristics section. 		
		 In Voltage Monitor Electrical Characteristics section, updated the "Trimmed" Fall and Rise specs of VHVD_LV_cold parameter in "Voltage Monitor Electrical Characteristics" table. 		
		 In AC Electrical Specifications: 3.3 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. In DC Electrical Specifications: 3.3 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" and updated "Vol min and max" values in the table. In AC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. In AC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. In DC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" and updated "Vol min and max" values in the table. 		
		 In "Flash memory AC timing specifications" table in Flash memory AC timing specifications section: Updated the "t_{psus}" typ value from 7 us to 9.4 us. Updated the "t_{psus}" max value from 9.1 us to 11.5 us. 		
		Added "Continuous SCK Timing" table in DSPI timing section.		
		 Added "ADC pad leakage" at 105°C TA conditions in "ADC conversion characteristics (for 12-bit)" table in ADC electrical specifications section. 		
		 In "STANDBY Current consumption characteristics" table in Supply current characteristics section: Updated the Typ and max values of IDD Standby current. Added IDD Standby3 current spec for FIRC ON. 		
		 Removed IVDDHV and IVDDLV specs in 16 MHz RC Oscillator electrical specifications section. 		
		 Added Reset Sequence section, with Reset Sequence Duration, BAF execution duration section, and Reset Sequence Distribution as its sub-sections. 		

Table continues on the next page ...