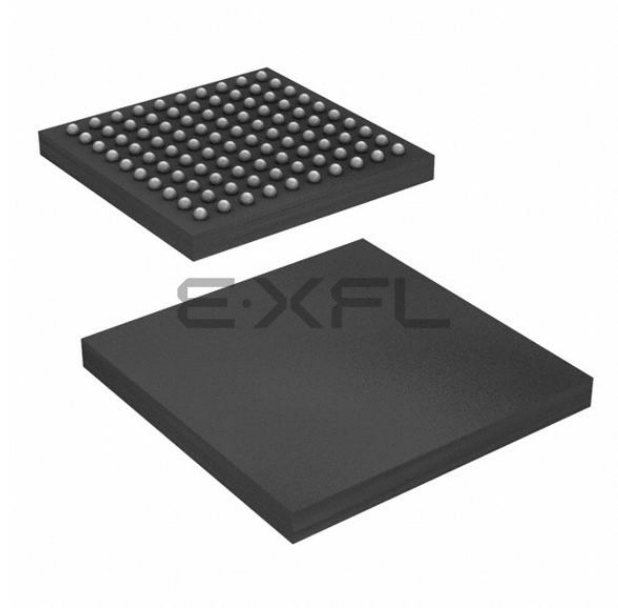

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, I²S, POR, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 36x10b, 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	100-MAPBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5745bbk1ammh6

NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest number or address (e.g., FlexCAN0) and end at highest available number or address (e.g., MPC574xB/C have 6 CAN, ending with FlexCAN5).

Table 1. MPC5746C Family Comparison[1]

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C
CPUs	e200z4	e200z4	e200z4	e200z4 e200z2	e200z4 e200z2	e200z4 e200z2
FPU	e200z4	e200z4	e200z4	e200z4	e200z4	e200z4
Maximum Operating Frequency[2]	160MHz (Z4)	160MHz (Z4)	160MHz (Z4)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)
Flash memory	2 MB	1.5 MB	3 MB	1.5 MB	2 MB	3 MB
EEPROM support	Emulated up to 64K			Emulated up to 64K		
RAM	256 KB	192 KB	384 KB (Optional 512KB)[3, 3]	192 KB	256 KB	384 KB (Optional 512KB)[3]
ECC	End to End					
SMPU	16 entry					
DMA	32 channels					
10-bit ADC	36 Standard channels 32 External channels					
12-bit ADC	15 Precision channels 16 Standard channels					
Analog Comparator	3					
BCTU	1					
SWT	1, SWT[0][4]			2[4]		
STM	1, STM[0]			2		
PIT-RTI	16 channels PIT 1 channels RTI					
RTC/API	1					
Total Timer I/O[5]	64 channels 16-bits					
LINFlexD	1 Master and Slave (LINFlexD[0], 11 Master (LINFlexD[1:11])			1 Master and Slave (LINFlexD[0], 15 Master (LINFlexD[1:15])		
FlexCAN	6 with optional CAN FD support (FlexCAN[0:5])			8 with optional CAN FD support (FlexCAN[0:7])		
DSPI/SPI	4 x DSPI 4 x SPI					

Table continues on the next page...

Table 2. MPC5746C Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW partition	MPC5744	MPC5745	MPC5746
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	not available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	7	not available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	7	not available	not available	available
0x011C0000	0x011FFFFF	256 KB code Flash block 7	7	not available	not available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	not available	not available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	not available	not available	not available

Table 3. MPC5746C Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW partition	MPC5744B MPC5745B MPC5746B	MPC5744C MPC5745C MPC5746C
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	not available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	not available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	not available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	not available	available

Table 4. MPC5746C Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40000000	0x40001FFF	8 KB	SRAM0	available	available	available
0x40002000	0x4000FFFF	56 KB	SRAM1	available	available	available
0x40010000	0x4001FFFF	64 KB	SRAM2	available	available	available
0x40020000	0x4002FFFF	64 KB	SRAM3	available	available	available

Table continues on the next page...

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 5. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$[2, 3]	3.3 V - 5. 5V input/output supply voltage	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$[4, 5]	3.3 V flash supply voltage (when supplying from an external source in bypass mode)	—	–0.3	3.63	V
$V_{DD\_LP\_DEC}$[6]	Decoupling pin for low power regulators[7]	—	–0.3	1.32	V
$V_{DD\_HV\_ADC1\_REF}$[8]	3.3 V / 5.0 V ADC1 high reference voltage	—	–0.3	6	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	3.3 V to 5.5V ADC supply voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	3.3V to 5.5V ADC supply ground	—	–0.1	0.1	V
V_{DD_LV}[9, 10, 10, 11, 11, 12]	Core logic supply voltage	—	–0.3	1.32	V
V_{INA}	Voltage on analog pin with respect to ground (V_{SS_HV})	—	–0.3	Min ($V_{DD\_HV\_x}$, $V_{DD\_HV\_ADCx}$, $V_{DD\_ADCx\_REF}$) +0.3	V
V_{IN}	Voltage on any digital pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$	–0.3	$V_{DD\_HV\_x}$ + 0.3	V
I_{INJPAD}	Injected input current on any pin during overload condition	Always	–5	5	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{ramp}	Supply ramp rate	—	0.5 V / min	100V/ms	—
T_A[13]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	–55	165	°C

1. All voltages are referred to VSS_HV unless otherwise specified
2. VDD_HV_B and VDD_HV_C are common together on the 176 LQFP-EP package.
3. Allowed $V_{DD\_HV\_x}$ = 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J= 150 °C, remaining time at or below 5.5 V.
4. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
5. VDD_HV_FLA must be disconnected from ANY power sources when VDD_HV_A = 5V
6. This pin should be decoupled with low ESR 1 µF capacitor.
7. Not available for input voltage, only for decoupling internal regulators
8. 10-bit ADC does not have dedicated reference and its reference is bonded to 10-bit ADC supply(VDD_HV_ADC0) inside the package.
9. Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C, remaining time as defined in footnotes 10 and 11.
10. Allowed 1.38 – 1.45 V– for 10 hours cumulative time at maximum T_J = 150 °C, remaining time as defined in footnote 11.
11. 1.32 – 1.38 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.326 V at maximum T_J = 150 °C.
12. If HVD on core supply ($V_{HVD\_LV\_x}$) is enabled, it will generate a reset when supply goes above threshold.
13. T_J=150°C. Assumes T_A=125°C
    - Assumes maximum θJA for 2s2p board. See Thermal attributes

Table 9. Voltage monitor electrical characteristics (continued)

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt[2, 2]	Reset Type	Min	Typ	Max	V
$V_{LVD\_LV\_PD2\_cold}$	LV supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.1400	1.1550	1.1750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.1600	1.1750	1.1950	V

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.
3. There is no voltage monitoring on the $V_{DD\_HV\_ADC0}$, $V_{DD\_HV\_ADC1}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ I/O segments. For applications requiring monitoring of these segments, either connect these to $V_{DD\_HV\_A}$ at the PCB level or monitor externally.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 10. Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_BODY\_1}$ [2, 3]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4, 4] T_a = 125°C [5, 5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 80MHz	—	—	147	mA
		T_a = 105°C	—	—	142	mA
		T_a = 85 °C	—	—	137	mA

Table continues on the next page...

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_BODY\_2}$ 6	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125°C[5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	—	246	mA
		T_a = 105°C	—	—	235	mA
		T_a = 85°C	—	—	210	mA
$I_{DD\_BODY\_3}$ 7	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125 °C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	181	mA
		T_a = 105 °C	—	—	176	mA
		T_a = 85°C	—	—	171	mA
$I_{DD\_BODY\_4}$[8]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125 °C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	264	mA
		T_a = 105 °C	—	—	176	mA
		T_a = 85 °C	—	—	171	mA
I_{DD_STOP}	STOP mode Operating current	T_a = 125 °C[9] V_{DD_LV} = 1.25 V	—	—	49	mA
		T_a = 105 °C V_{DD_LV} = 1.25 V	—	10.6	—	
		T_a = 85 °C V_{DD_LV} = 1.25 V	—	8.1	—	
		T_a = 25 °C V_{DD_LV} = 1.25 V	—	4.6	—	

Table continues on the next page...

8. e200Z4 core, 160MHz, cache enabled; e200Z4 core, 80MHz; HSM fully operational (Z0 core @80MHz) FlexRay, 5x CAN, 5x LINFlexD, 2x SPI, 1x ADC used constantly, 1xeMIOS (5 ch), Memory: 3M flash, 384K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
9. Assuming Ta=Tj, as the device is in Stop mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes.
10. Internal structures hold the input voltage less than $V_{DD\_HV\_ADC\_REF}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
11. This value is the total current for two ADCs.Each ADC might consume upto 2mA at max.
12. This assumes the default configuration of flash controller register. For more details, refer to Flash memory program and erase specifications

Table 11. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
LPU_RUN	with 256K RAM	T_a = 25 °C SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF	—	10	—	mA
		T_a = 85 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	10.5	—	
		T_a = 105 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	11	—	
		T_a = 125 °C[2, 2] SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	—	26	
LPU_STOP	with 256K RAM	T_a = 25 °C	—	0.18	—	mA
		T_a = 85 °C	—	0.60	—	
		T_a = 105 °C	—	1.00	—	
		T_a = 125 °C [2]	—	—	10.6	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

Table 12. STANDBY Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
STANDBY0	STANDBY with 8K RAM	T_a = 25 °C	—	71	—	µA
		T_a = 85 °C	—	125	700	
		T_a = 105 °C	—	195	1225	
		T_a = 125 °C [2, 2]	—	314	2100	
STANDBY1	STANDBY with 64K RAM	T_a = 25 °C	—	72	—	µA
		T_a = 85 °C	—	140	715	
		T_a = 105 °C	—	225	1275	
		T_a = 125 °C [2]	—	358	2250	

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Table 12. STANDBY Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
STANDBY2	STANDBY with 128K RAM	T_a = 25 °C	—	75	—	µA
		T_a = 85 °C	—	155	730	
		T_a = 105 °C	—	255	1350	
		T_a = 125 °C [2]	—	396	2600	
STANDBY3	STANDBY with 256K RAM	T_a = 25 °C	—	80	—	µA
		T_a = 85 °C	—	180	800	
		T_a = 105 °C	—	290	1425	
		T_a = 125 °C [2]	—	465	2900	
STANDBY3	FIRC ON	T_a = 25 °C	—	500	—	µA

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 13. ESD ratings

Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 14. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry[2]	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01[3]
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00[3]
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input)[4]		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.
3. Slew rate control modes
4. Input slope = 2ns

NOTE

The specification given above is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The specification given above is measured between 20% / 80%.

5.2 DC electrical specifications @ 3.3V Range

Table 15. DC electrical specifications @ 3.3V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	Pad_I_HV Input Buffer High Voltage	0.72*VDD_HV_x	VDD_HV_x + 0.3	V
Vil (pad_i_hv)	Pad_I_HV Input Buffer Low Voltage	VDD_HV_x - 0.3	0.45*VDD_HV_x	V
Vhys (pad_i_hv)	Pad_I_HV Input Buffer Hysteresis	0.11*VDD_HV_x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.67*VDD_HV_x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VDD_HV_x - 0.3	0.35*VDD_HV_x	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.57 * VDD_HV_x[1, 1]	VDD_HV_x[1] + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VDD_HV_x - 0.3	0.4 * VDD_HV_x[1]	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x[1]		V
Pull_IIH (pad_i_hv)	Weak Pullup Current[2, 2] Low	15		µA
Pull_IIH (pad_i_hv)	Weak Pullup Current[3, 3] High		55	µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[3] Low	28		µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[2] High		85	µA
Pull_Ioh	Weak Pullup Current[4]	15	50	µA
Pull_Iol	Weak Pulldown Current[5]	15	50	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[6]	0.8 *VDD_HV_x[1]	—	V
Vol	Output Low Voltage[7] Output Low Voltage[8]	—	0.2 *VDD_HV_x[1] 0.1 *VDD_HV_x	V
Ioh_f	Full drive Ioh[9, 9] (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.3 AC specifications @ 5 V Range

Table 16. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		4.5/4.5		1.3/1.2	25	11
		6/6		2.5/2	50	
		13/13		9/9	200	
		5.25/5.25		3/2	25	10
		9/8		5/4	50	
		22/22		18/16	200	
		27/27		13/13	50	01[2, 2]
		40/40		24/24	200	
		40/40		24/24	50	00[2]
		65/65		40/40	200	
pad_i_hv/ pad_sr_hv (input)		1.5/1.5		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V

Table continues on the next page...

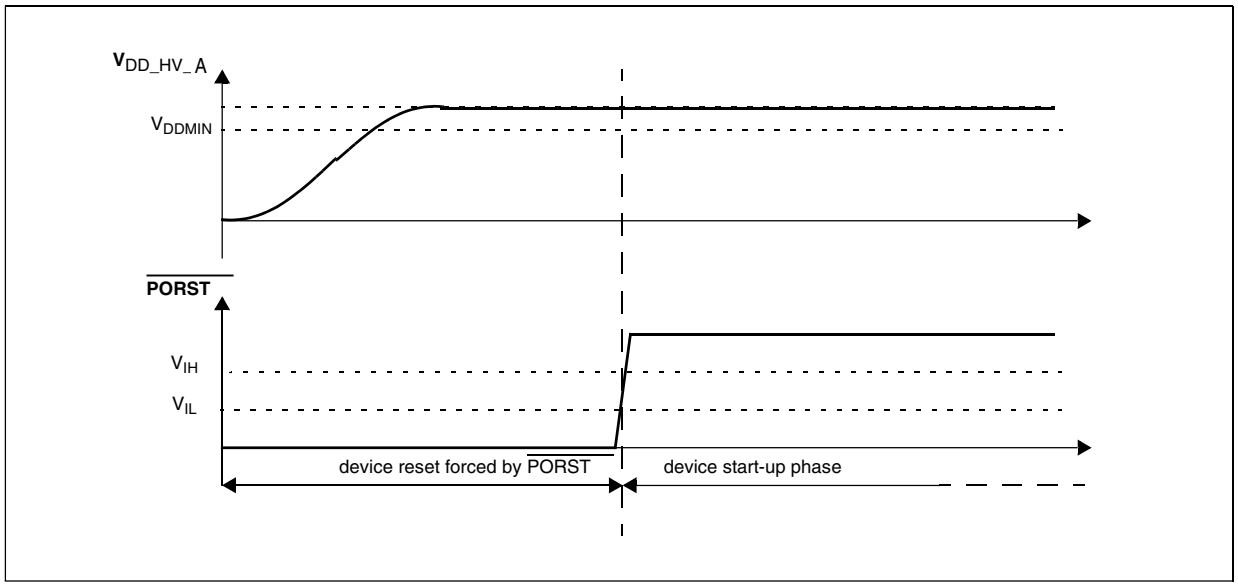

Figure 3. Start-up reset requirements

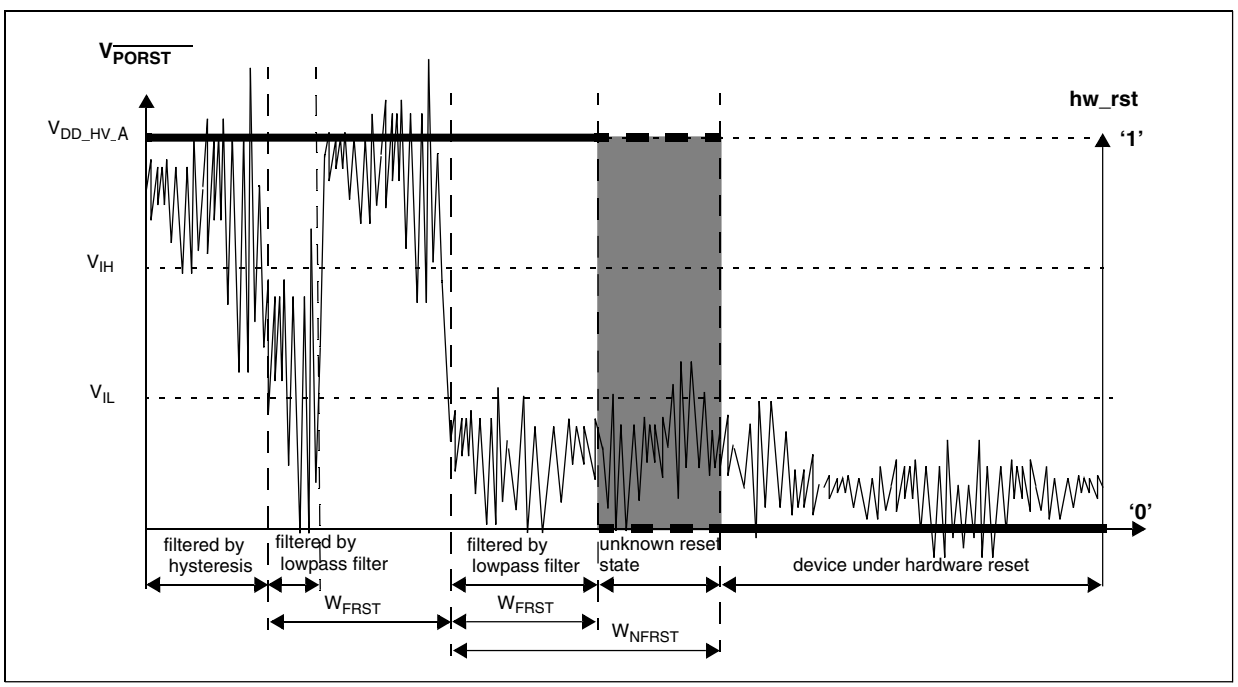

Figure 4. Noise filtering on reset signal

Table 18. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	CMOS Input Buffer High Voltage	—	$0.65*V_{DD\_HV\_x}$	—	$V_{DD\_HV\_x}$ +0.3	V
V_{IL}	CMOS Input Buffer Low Voltage	—	$V_{DD\_HV\_x}$-0.3	—	$0.35*V_{DD\_HV\_x}$	V

Table continues on the next page...

6.1.1.1 Input equivalent circuit and ADC conversion characteristics

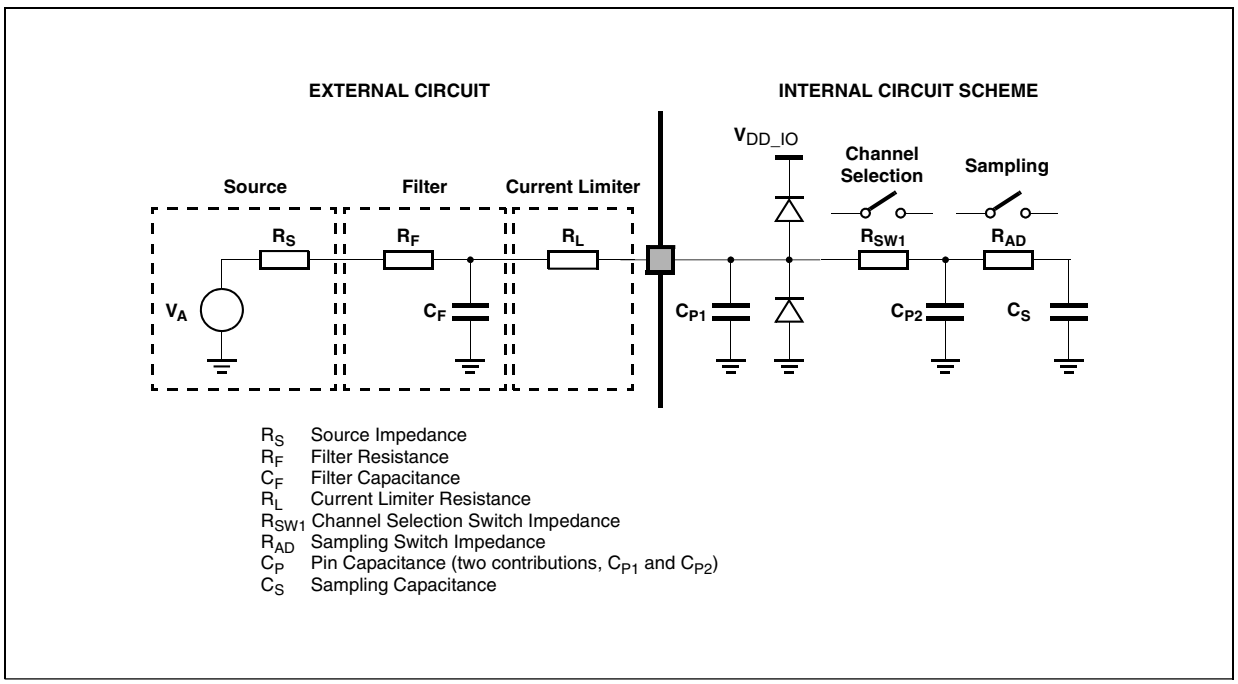

Figure 6. Input equivalent circuit

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

Table 20. ADC conversion characteristics (for 12-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	250	—	—	ns
t_{conv}	Conversion time[4]	80 MHz	700	—	—	ns
t_{total_conv}	Total Conversion time t_{sample} + t_{conv} (for standard and extended channels)	80 MHz	1.5[5]	—	—	µs
	Total Conversion time t_{sample} + t_{conv} (for precision channels)		1	—	—	
C_S[6, 6]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[6]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[6]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω

Table continues on the next page...

Table 20. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
R_{AD}[6]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity (precise channel)	—	–2	—	2	LSB
INL	Integral non-linearity (standard channel)	—	–3	—	3	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (precision channel)	150 °C	—	—	250	nA
	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C $_{TA}$	—	5	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{precision\ channels}$	Total unadjusted error for precision channels	Without current injection	–6	+/-4	6	LSB
		With current injection[7, 7]		+/-5		LSB
$TUE_{standard/extended\ channels}$	Total unadjusted error for standard/ extended channels	Without current injection	–8	+/-6	8	LSB
		With current injection[7]		+/-8		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	µs

1. Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 6.
7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

Table 21. ADC conversion characteristics (for 10-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{conv}	Conversion time[4]	80 MHz	550	—	—	ns
t_{total_conv}	Total Conversion time tsample + tconv (for standard channels)	80 MHz	1	—	—	µs
	Total Conversion time tsample + tconv (for extended channels)		1.5	—	—	
C_S[5]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[5]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[5]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[5]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD}[5]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max positive/negative injection		–5	—	5	mA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
$TUE_{standard/extended\ channels}$	Total unadjusted error for standard channels	Without current injection	–4	+/-3	4	LSB
		With current injection[6]		+/-4		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	µs

1. Active ADC Input, VinA < [min(ADC_ADV, IO_Supply_A,B,C)]. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO_supply_A, B, C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See Figure 65
6. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

6.2.4 128 KHz Internal RC oscillator Electrical specifications

Table 26. 128 KHz Internal RC oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{oscu}[1]	Oscillator frequency	Calibrated	119	128	136.5	KHz
	Temperature dependence				600	ppm/C
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	µA
		Clock stopped			200	nA

1. Vdd=1.2 V, 1.32V, T_a=-40 C, 125 C

6.2.5 PLL electrical specifications

Table 27. PLL electrical specifications

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 28	ps	NON SSCG mode
TIE			See Table 28		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	µs	Calibration mode

Table 28. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN}[1]	Jitter due to Fractional Mode (ps) J_{SDM}[2]	Jitter due to Fractional Mode J_{SSCG} (ps) [3]	1 Sigma Random Jitter J_{RJ} (ps) [4]	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	+/-(J_{SN}+J_{SDM}+J_{SSCG}+N[4] ×J_{RJ})

Table continues on the next page...

Table 31. Flash memory Array Integrity and Margin Read specifications (continued)

Symbol	Characteristic	Min	Typical	Max[1, 1]	Units[2, 2]
$t_{ai256kseq}$	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

6.3.3 Flash memory module life specifications

Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1, 1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2, 2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

6.3.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = –40 oC / 150 oC.

6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 41. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

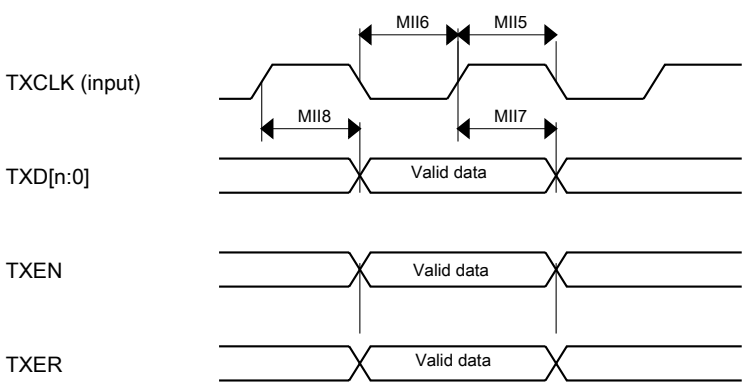

Figure 21. RMII/MII transmit signal timing diagram

Thermal attributes

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
—	$R_{\theta JC}$	Thermal resistance, junction to case	7.9	°C/W	55
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	66
—	$R_{\theta JB\_CSB}$	Thermal characterization parameter, junction to package bottom outside center (natural convection)	9.0	°C/W	77

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	100 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50.9	°C/W	1, 21,2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	27.0	°C/W	1,2,33
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	38.0	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	22.2	°C/W	1,3

Table continues on the next page...

10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

Table 50. BAF execution duration

BAF execution duration	Min	Typ	Max	Unit
BAF execution time (boot header at first location)	—	200	—	µs
BAF execution time (boot header at last location)	—	—	320	µs

10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

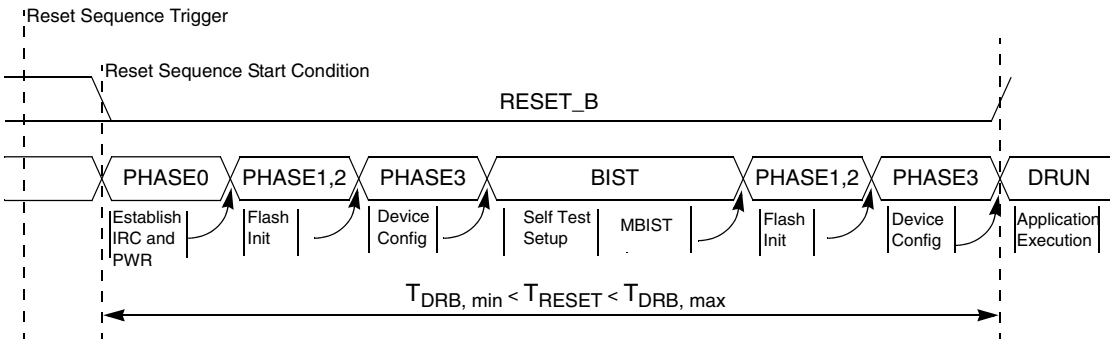

Figure 32. Destructive reset sequence, BIST enabled

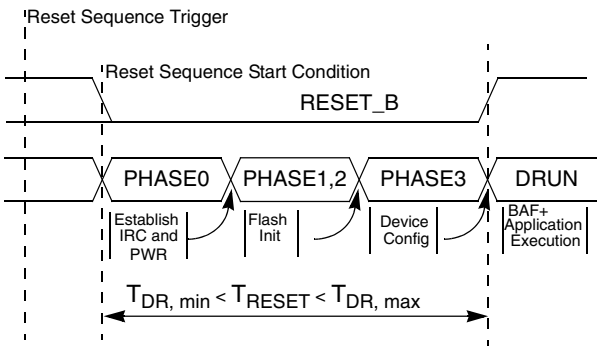

Figure 33. Destructive reset sequence, BIST disabled

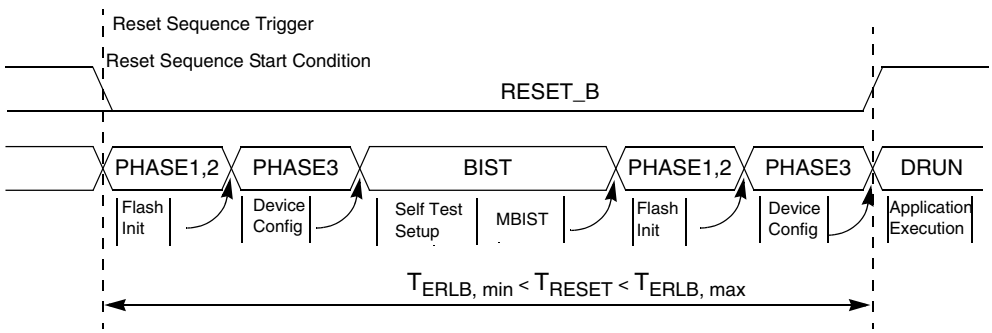

Figure 34. External reset sequence long, BIST enabled

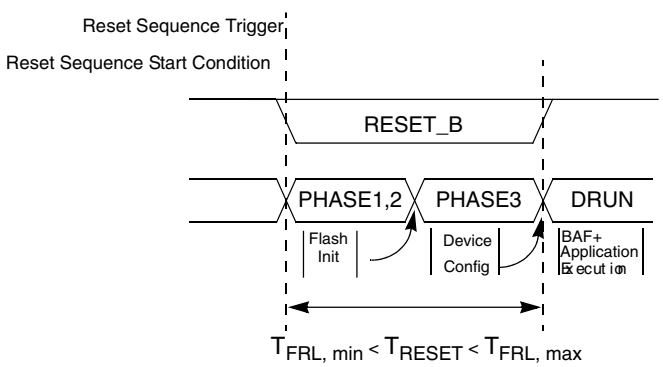

Figure 35. Functional reset sequence long