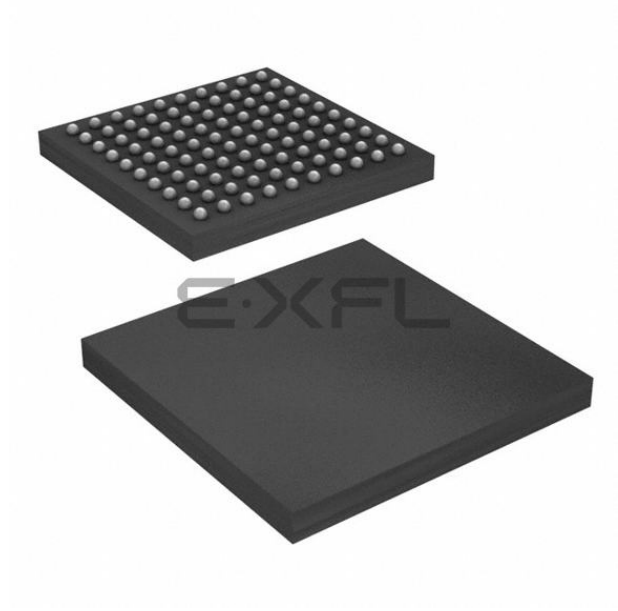

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Peripherals	DMA, I²S, POR, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 36x10b, 16x12b
Oscillator Type	Internal
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Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	100-MAPBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5745bk1vmh2

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

NOTE

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)

Symbol	Parameter	Conditions[1]	Min[2]	Max	Unit
$V_{DD\_HV\_A}$ $V_{DD\_HV\_B}$ $V_{DD\_HV\_C}$	HV IO supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_FLA}$[3]	HV flash supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_ADC1\_REF}$	HV ADC1 high reference voltage	—	3.0	5.5	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	HV ADC supply voltage	—	max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05	3.6	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV}[4, 5]	Core supply voltage	—	1.2	1.32	V
$V_{IN1\_CMP\_REF}$[6, 7]	Analog Comparator DAC reference voltage	—	3.15	3.6	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA

Table continues on the next page...

4. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. VIN1_CMP_REF ≤ VDD_HV_A
6. This supply is shorted VDD_HV_A on lower packages.
7. T_J=150°C. Assumes T_A=125°C
    - Assumes maximum θJA of 2s2p board. See Thermal attributes

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
    - Control of external NPN ballast transistor
    - Generating core supply using internal ballast transistor
    - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector (LVD_FLASH) for 3.3 V flash supply (VDD_HV_FLA)
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

1. BCP56, MCP68 and MJD31are guaranteed ballasts.

4.4 Voltage monitor electrical characteristics

Table 9. Voltage monitor electrical characteristics

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt[2, 2]	Reset Type	Min	Typ	Max	V
V_{POR_LV}	LV supply power on reset detector	Fall	Untrimmed	Yes	No	Destructive	0.930	0.979	1.028	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				0.980	1.029	1.078	V
			Trimmed				-	-	-	V
$V_{HVD\_LV\_cold}$	LV supply high voltage monitoring, detecting at device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.325	1.345	1.375	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.345	1.365	1.395	V
$V_{LVD\_LV\_PD2\_hot}$	LV supply low voltage monitoring, detecting on the PD2 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1250	1.1425	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1450	1.1625	1.1800	V
$V_{LVD\_LV\_PD1\_hot\ (BGFP)}$	LV supply low voltage monitoring, detecting on the PD1 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.140	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
$V_{LVD\_LV\_PD0\_hot\ (BGFP)}$	LV supply low voltage monitoring, detecting on the PD0 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
V_{POR_HV}	HV supply power on reset detector	Fall	Untrimmed	Yes	No	Destructive	2.7000	2.8500	3.0000	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				2.7500	2.9000	3.0500	V
			Trimmed				-	-	-	V
$V_{LVD\_IO\_A\_LO}$[3, 3]	HV IO_A supply low voltage monitoring - low range	Fall	Untrimmed	Yes	No	Destructive	2.7500	2.9230	3.0950	V
			Trimmed				2.9780	3.0390	3.1000	V
		Rise	Untrimmed				2.7800	2.9530	3.1250	V
			Trimmed				3.0080	3.0690	3.1300	V
$V_{LVD\_IO\_A\_HI}$[3]	HV IO_A supply low voltage monitoring - high range	Fall	Trimmed	No	Yes	Destructive	Disabled at Start			
							4.0600	4.151	4.2400	V
		Rise	Trimmed				Disabled at Start			
							4.1150	4.2010	4.3000	V

Table continues on the next page...

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_HV\_ADC\_REF}$[10, 11, 11]	ADC REF Operating current	T_a = 125 °C[5] 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 5.5 V	—	200	400	µA
		T_a = 105 °C 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 5.5 V	—	200	—	
		T_a = 85 °C 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 5.5 V	—	200	—	
		T_a = 25 °C 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 3.6 V	—	200	—	
$I_{DD\_HV\_ADCx}$[11]	ADC HV Operating current	T_a = 125 °C[5] ADC operating at 80 MHz $V_{DD\_HV\_ADC}$ = 5.5 V	—	1.2	2	mA
		T_a = 25 °C ADC operating at 80 MHz $V_{DD\_HV\_ADC}$ = 3.6 V	—	1	2	
$I_{DD\_HV\_FLASH}$[12]	Flash Operating current during read access	T_a = 125 °C[5] 3.3 V supplies 160 MHz frequency	—	40	45	mA
		T_a = 105 °C 3.3 V supplies 160 MHz frequency	—	40	45	
		T_a = 85 °C 3.3 V supplies 160 MHz frequency	—	40	45	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Single e200Z4 core cache disabled @80 MHz, no FlexRay, no ENET, 2 x CAN, 8 LINFlexD, 2 SPI, ADC0 and 1 used constantly, no HSM, Memory: 2M flash, 128K RAM RUN mode, Clocks: FIRC on, XOSC, PLL on, SIRC on for TOD, no 32KHz crystal (TOD runs off SIRC).
3. Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C. In case of internal ballast mode, it is expected that the external ballast is not mounted and BAL_SELECT_INT pin is tied to VDD_HV_A supply on board. Internal ballast can be used for all use cases with current consumption upto 150mA
4. The power consumption does not consider the dynamic current of I/Os
5. Tj=150°C. Assumes Ta=125°C
   - Assumes maximum θJA of 2s2p board. SeeThermal attributes
6. e200Z4 core, 160MHz, cache enabled; e200Z2 core , 80MHz, no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 256K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
7. e200Z4 core, 120MHz, cache enabled; e200Z2 core, 60MHz; no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 128K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal

8. e200Z4 core, 160MHz, cache enabled; e200Z4 core, 80MHz; HSM fully operational (Z0 core @80MHz) FlexRay, 5x CAN, 5x LINFlexD, 2x SPI, 1x ADC used constantly, 1xeMIOS (5 ch), Memory: 3M flash, 384K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
9. Assuming Ta=Tj, as the device is in Stop mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes.
10. Internal structures hold the input voltage less than $V_{DD\_HV\_ADC\_REF}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
11. This value is the total current for two ADCs.Each ADC might consume upto 2mA at max.
12. This assumes the default configuration of flash controller register. For more details, refer to Flash memory program and erase specifications

Table 11. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
LPU_RUN	with 256K RAM	T_a = 25 °C SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF	—	10	—	mA
		T_a = 85 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	10.5	—	
		T_a = 105 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	11	—	
		T_a = 125 °C[2, 2] SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	—	26	
LPU_STOP	with 256K RAM	T_a = 25 °C	—	0.18	—	mA
		T_a = 85 °C	—	0.60	—	
		T_a = 105 °C	—	1.00	—	
		T_a = 125 °C [2]	—	—	10.6	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

Table 12. STANDBY Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
STANDBY0	STANDBY with 8K RAM	T_a = 25 °C	—	71	—	µA
		T_a = 85 °C	—	125	700	
		T_a = 105 °C	—	195	1225	
		T_a = 125 °C [2, 2]	—	314	2100	
STANDBY1	STANDBY with 64K RAM	T_a = 25 °C	—	72	—	µA
		T_a = 85 °C	—	140	715	
		T_a = 105 °C	—	225	1275	
		T_a = 125 °C [2]	—	358	2250	

Table continues on the next page...

Table 12. STANDBY Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
STANDBY2	STANDBY with 128K RAM	T_a = 25 °C	—	75	—	µA
		T_a = 85 °C	—	155	730	
		T_a = 105 °C	—	255	1350	
		T_a = 125 °C [2]	—	396	2600	
STANDBY3	STANDBY with 256K RAM	T_a = 25 °C	—	80	—	µA
		T_a = 85 °C	—	180	800	
		T_a = 105 °C	—	290	1425	
		T_a = 125 °C [2]	—	465	2900	
STANDBY3	FIRC ON	T_a = 25 °C	—	500	—	µA

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 13. ESD ratings

Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

Table 18. Functional reset pad electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{HYS}	CMOS Input Buffer hysterisis	—	300	—	—	mV
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current [1, 1]	Device under power-on reset $V_{DD\_HV\_A}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD\_HV\_A}$	0.2	—	—	mA
		Device under power-on reset $V_{DD\_HV\_A}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD\_HV\_IO}$	11	—	—	mA
W_{FRST}	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	$\overline{\text{RESET}}$ input not filtered pulse	—	2000	—	—	ns
$\|I_{WPU}\|$	Weak pull-up current absolute value	RESET pin V_{IN} = V_{DD}	23	—	82	µA

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{\text{PORST}}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{\text{PORST}}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	0.65 x $V_{DD\_HV\_A}$	—	—	V
V_{IL}	Input low level	—	—	0.35 x $V_{DD\_HV\_A}$	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

6.1.1.1 Input equivalent circuit and ADC conversion characteristics

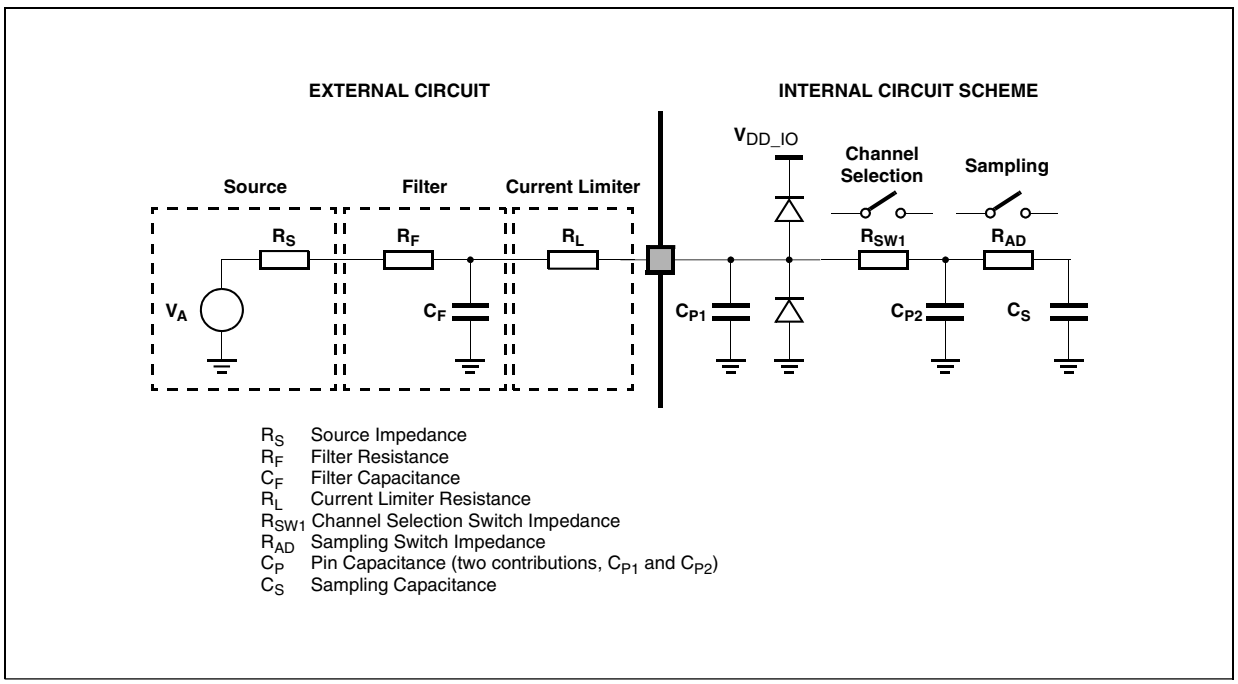

Figure 6. Input equivalent circuit

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

Table 20. ADC conversion characteristics (for 12-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	250	—	—	ns
t_{conv}	Conversion time[4]	80 MHz	700	—	—	ns
t_{total_conv}	Total Conversion time t_{sample} + t_{conv} (for standard and extended channels)	80 MHz	1.5[5]	—	—	µs
	Total Conversion time t_{sample} + t_{conv} (for precision channels)		1	—	—	
C_S[6, 6]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[6]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[6]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω

Table continues on the next page...

6.1.2 Analog Comparator (CMP) electrical specifications

Table 22. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	µA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1\_CMP\_REF}$	V
V_{AIO}	Analog input offset voltage [1, 1]	-47	—	47	mV
V_H	Analog comparator hysteresis [2, 2]	—	1	25	mV
	• CR0[HYSTCTR] = 00	—	20	50	mV
	• CR0[HYSTCTR] = 01	—	40	70	mV
	• CR0[HYSTCTR] = 10	—	60	105	mV
	• CR0[HYSTCTR] = 11				
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) [1, 3, 3]	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) [1, 3]	—	5	21	µs
	Analog comparator initialization delay, High speed mode[4, 4]	—	4		µs
	Analog comparator initialization delay, Low speed mode [4]	—	100		µs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[5]
DNL	6-bit DAC differential non-linearity	–0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD\_HV\_A}$-0.6V
3. Full swing = VIH, VIL
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

Table 35. DSPI electrical specifications (continued)

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	NA	—	–2	—	ns
			Slave	4	—	6	—	
			Master (MTFE = 1, CPHA = 0)	-2	—	10[1]	—	
			Master (MTFE = 1, CPHA = 1)	–2	—	–2	—	

1. SMPL_PTR should be set to 1

NOTE

Restriction For High Speed modes

- DSPI2, DSPI3, SPI1 and SPI2 will support 40MHz Master mode SCK
- DSPI2, DSPI3, SPI1 and SPI2 will support 25MHz Slave SCK frequency
- Only one {SIN,SOUT and SCK} group per DSPI/SPI will support high frequency mode
- For Master mode MTFE will be 1 for high speed mode
- For high speed slaves, their master have to be in MTFE=1 mode or should be able to support 15ns tSUO delay

NOTE

For numbers shown in the following figures, see Table 35

Table 36. Continuous SCK timing

Spec	Characteristics	Pad Drive/Load	Value	
			Min	Max
tSCK	SCK cycle timing	strong/50 pF	100 ns	-
-	PCS valid after SCK	strong/50 pF	-	15 ns
-	PCS valid after SCK	strong/50 pF	-4 ns	-

Table 37. DSPI high speed mode I/Os

DSPI	High speed SCK	High speed SIN	High speed SOUT
DSPI2	GPIO[78]	GPIO[76]	GPIO[77]
DSPI3	GPIO[100]	GPIO[101]	GPIO[98]
SPI1	GPIO[173]	GPIO[175]	GPIO[176]
SPI2	GPIO[79]	GPIO[110]	GPIO[111]

Table 44. Slave mode SAI Timing (continued)

No	Parameter	Value		Unit
		Min	Max	
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

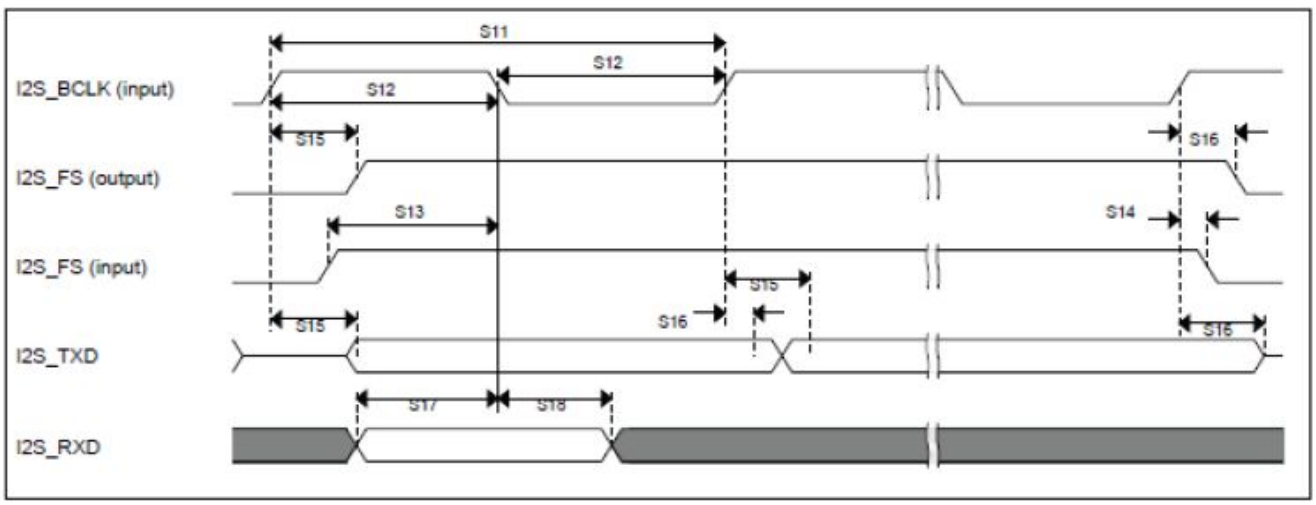

Figure 24. Slave mode SAI Timing

6.5 Debug specifications

6.5.1 JTAG interface timing

Table 45. JTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time [2, 2]	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20[3, 3]	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600[4, 4]	ns

Table continues on the next page...

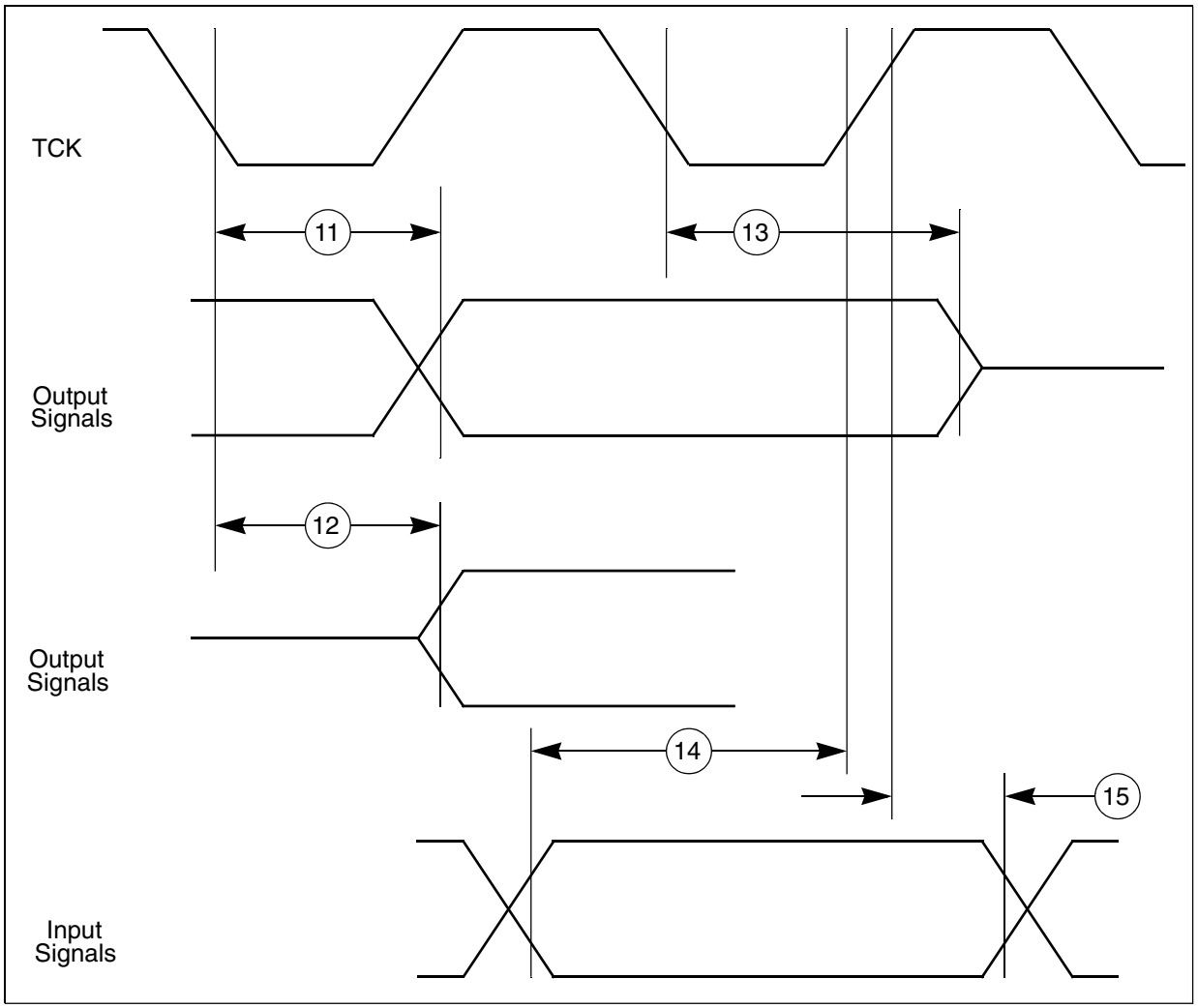

Figure 27. JTAG boundary scan timing

6.5.2 Nexus timing

Table 46. Nexus debug port timing [1]

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	tMCYC
4	t_{EVTIPW}	$\overline{\text{EVTI}}$ Pulse Width	—	4	—	tTCYC
5	t_{EVTOPW}	$\overline{\text{EVTO}}$ Pulse Width	—	1	—	tMCYC
6	t_{TCYC}	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	TDI, TMS Data Setup Time	—	8	—	ns

Table continues on the next page...

Table 46. Nexus debug port timing [1] (continued)

No.	Symbol	Parameter	Conditions	Min	Max	Unit
9	t_{NTDIH}, t_{NTMSH}	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

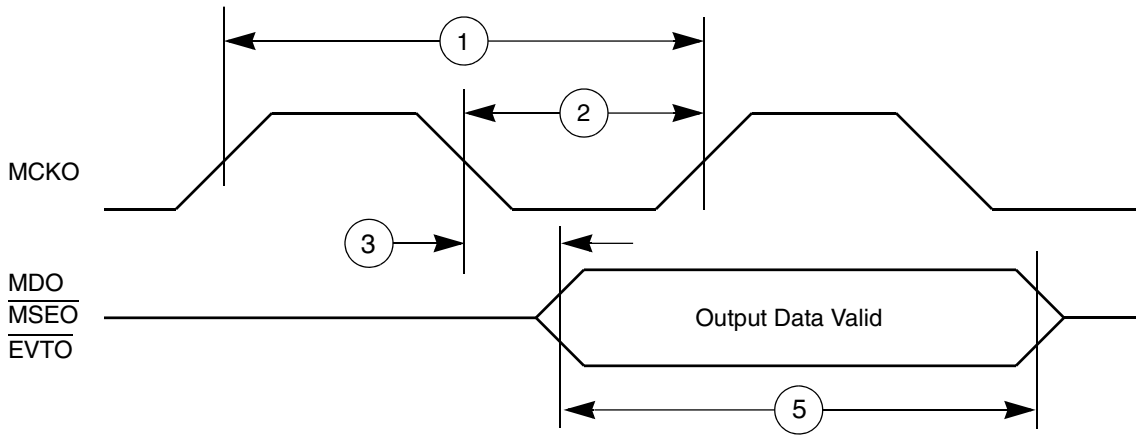

Figure 28. Nexus output timing

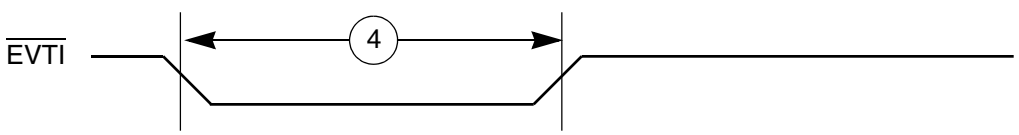

Figure 29. Nexus EVTI Input Pulse Width

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	16.8	°C/W	44
—	$R_{\theta JC}$	Thermal resistance, junction to case	7.4	°C/W	55
—	Ψ_{JT}	Thermal characterization parameter, junction to package top natural convection	0.2	°C/W	66
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom natural convection	7.3	°C/W	77

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	42.6	°C/W	11, 22
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	26.0	°C/W	1,2,33
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	31.0	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	21.3	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	12.8	°C/W	44

Table continues on the next page...

Board type	Symbol	Description	100 MAPBGA	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.8	°C/W	44
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.2	°C/W	55
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	66
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center (natural convection)	7.8	°C/W	77

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

Package	NXP Document Number
100 MAPBGA	98ASA00802D

Table continues on the next page...

10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

Table 50. BAF execution duration

BAF execution duration	Min	Typ	Max	Unit
BAF execution time (boot header at first location)	—	200	—	µs
BAF execution time (boot header at last location)	—	—	320	µs

10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

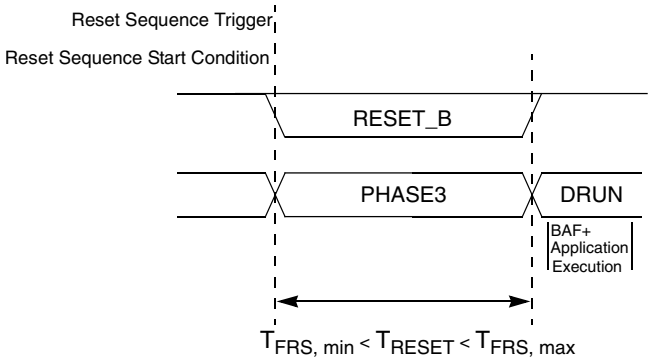

Figure 36. Functional reset sequence short

The reset sequences shown in Figure 35 and Figure 36 are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

11.1 Revision History

The following table provides a revision history for this document.

Table 51. Revision History

Rev. No.	Date	Substantial Changes
Rev 1	14 March 2013	Initial Release

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In section, Thermal attributes
		  • Added table for 100 MAPBGA
		
		• In section Obtaining package dimensions
		  • Updated package details for 100 MAPBGA

		• Editoral updates throughtout including correction of various module names.

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev 5.1	22 May 2017	• Removed the Introduction section from Section 4 "General". • In AC Specifications@3.3V section, removed note related to Cz results and added two notes. • In AC Specifications@5V section, added two notes. • In ADC Electrical Specifications section, added spec value of "ADC Analog Pad" at Max leakage (standard channel)@ 105 C T_A in "ADC conversion characteristics (for 10-bit)" table. • In PLL Electrical Specifications section, updated the first footnote of "Jitter calculation" table. • In Analog Comparator Electrical Specifications section, updated the TDLS (propagation delay, low power mode) max value in "Comparator and 6-bit DAC electrical specifications" table to 21 us. • In Recommended Operating Conditions section, updated the footnote link to T_A in "Recommended operating conditions (V DD_HV_x = 5V)" table.