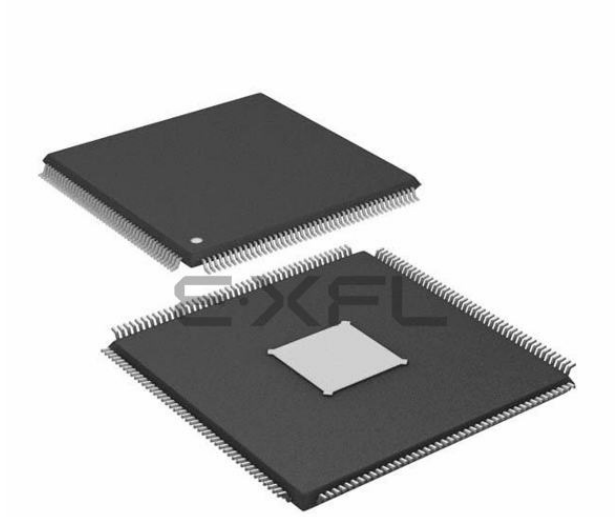

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz, 160MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, I²S, POR, WDT
Number of I/O	129
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 36x10b, 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5745cfk1amku6

4. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. VIN1_CMP_REF ≤ VDD_HV_A
6. This supply is shorted VDD_HV_A on lower packages.
7. T_J=150°C. Assumes T_A=125°C
    - Assumes maximum θJA of 2s2p board. See Thermal attributes

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
    - Control of external NPN ballast transistor
    - Generating core supply using internal ballast transistor
    - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector (LVD_FLASH) for 3.3 V flash supply (VDD_HV_FLA)
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

1. BCP56, MCP68 and MJD31are guaranteed ballasts.

5. 1. For VDD_HV_x, 1µf on each side of the chip
      a. 0.1 µf close to each VDD/VSS pin pair.
      b. 10 µf near for each power supply source
      c. For VDD_LV, 0.1uf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter.
   2. For VDD_LV, 0.1uf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter
6. Only applicable to ADC1
7. In external ballast configuration the following must be ensured during power-up and power-down (Note: If $V_{DD\_HV\_BALLAST}$ is supplied from the same source as VDD_HV_A this condition is implicitly met):
   - During power-up, $V_{DD\_HV\_BALLAST}$ must have met the min spec of 2.25V before VDD_HV_A reaches the POR_HV_RISE min of 2.75V.
   - During power-down, $V_{DD\_HV\_BALLAST}$ must not drop below the min spec of 2.25V until VDD_HV_A is below POR_HV_FALL min of 2.7V.

NOTE

For a typical configuration using an external ballast transistor with separate supply for VDD_HV_A and the ballast collector, a bulk storage capacitor (as defined in Table 8) is required on VDD_HV_A close to the device pins to ensure a stable supply voltage.

Extra care must be taken if the VDD_HV_A supply is also being used to power the external ballast transistor or the device is running in internal regulation mode. In these modes, the inrush current on device Power Up or on exit from Low Power Modes is significant and may case the VDD_HV_A voltage to drop resulting in an LVD reset event. To avoid this, the board layout should be optimized to reduce common trace resistance or additional capacitance at the ballast transistor collector (or VDD_HV_A pins in the case of internal regulation mode) is required. NXP recommends that customers simulate the external voltage supply circuitry.

In all circumstances, the voltage on VDD_HV_A must be maintained within the specified operating range (see Recommended operating conditions) to prevent LVD events.

Table 9. Voltage monitor electrical characteristics (continued)

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt[2, 2]	Reset Type	Min	Typ	Max	V
$V_{LVD\_LV\_PD2\_cold}$	LV supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.1400	1.1550	1.1750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.1600	1.1750	1.1950	V

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.
3. There is no voltage monitoring on the $V_{DD\_HV\_ADC0}$, $V_{DD\_HV\_ADC1}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ I/O segments. For applications requiring monitoring of these segments, either connect these to $V_{DD\_HV\_A}$ at the PCB level or monitor externally.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 10. Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_BODY\_1}$ [2, 3]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4, 4] T_a = 125°C [5, 5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 80MHz	—	—	147	mA
		T_a = 105°C	—	—	142	mA
		T_a = 85 °C	—	—	137	mA

Table continues on the next page...

Table 12. STANDBY Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
STANDBY2	STANDBY with 128K RAM	T_a = 25 °C	—	75	—	µA
		T_a = 85 °C	—	155	730	
		T_a = 105 °C	—	255	1350	
		T_a = 125 °C [2]	—	396	2600	
STANDBY3	STANDBY with 256K RAM	T_a = 25 °C	—	80	—	µA
		T_a = 85 °C	—	180	800	
		T_a = 105 °C	—	290	1425	
		T_a = 125 °C [2]	—	465	2900	
STANDBY3	FIRC ON	T_a = 25 °C	—	500	—	µA

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 13. ESD ratings

Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

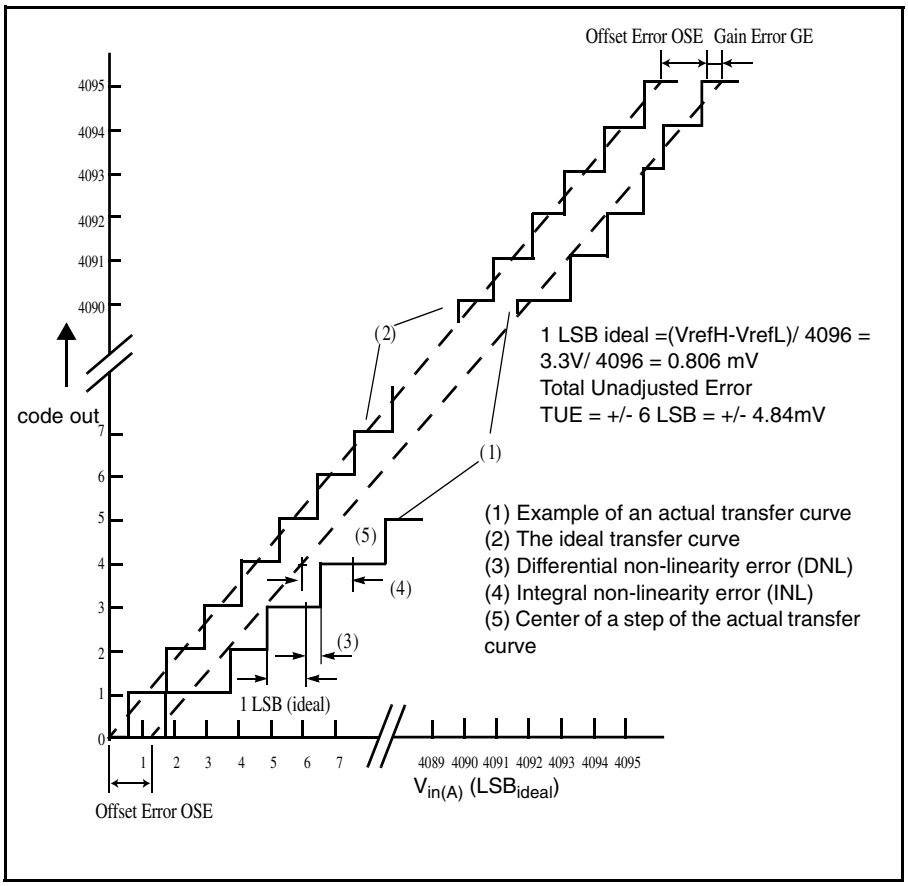

Figure 5. ADC characteristics and error definitions

6.1.2 Analog Comparator (CMP) electrical specifications

Table 22. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	µA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1\_CMP\_REF}$	V
V_{AIO}	Analog input offset voltage [1, 1]	-47	—	47	mV
V_H	Analog comparator hysteresis [2, 2]	—	1	25	mV
	• CR0[HYSTCTR] = 00	—	20	50	mV
	• CR0[HYSTCTR] = 01	—	40	70	mV
	• CR0[HYSTCTR] = 10	—	60	105	mV
	• CR0[HYSTCTR] = 11				
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) [1, 3, 3]	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) [1, 3]	—	5	21	µs
	Analog comparator initialization delay, High speed mode[4, 4]	—	4		µs
	Analog comparator initialization delay, Low speed mode [4]	—	100		µs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[5]
DNL	6-bit DAC differential non-linearity	–0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD\_HV\_A}$-0.6V
3. Full swing = VIH, VIL
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

Table 23. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
	Oscillator Analog Circuit supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		
		LCP	8 MHz		141		uA
			16 MHz		252		
			40 MHz		518		
V_{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3	1.95			V
V_{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3			1.25	V

1. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board.
2. Typ value for oscillator supply 3.3 V@27 °C

6.2.2 32 kHz Oscillator electrical specifications

Table 24. 32 kHz oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{osc_lo}	Oscillator crystal or resonator frequency		32		40	KHz
t_{cst}	Crystal Start-up Time[1, 2]				2	s

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 16 MHz RC Oscillator electrical specifications

Table 25. 16 MHz RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F_{Target}	IRC target frequency	—	—	16	—	MHz
PTA	IRC frequency variation after trimming	—	-5	—	5	%
$T_{startup}$	Startup time	—		—	1.5	us
T_{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T_{LTJIT}	Long term jitter		—	—	0.2	%

Table 30. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1, 1]	Units[2, 2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—

Table continues on the next page...

6.4 Communication interfaces

6.4.1 DSPI timing

Table 35. DSPI electrical specifications

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
1	t_{SCK}	DSPI cycle time	Master (MTFE = 0)	25	—	50	—	ns
			Slave (MTFE = 0)	40	—	60	—	
2	t_{CSC}	PCS to SCK delay	—	16	—	—	—	ns
3	t_{ASC}	After SCK delay	—	16	—	—	—	ns
4	t_{SDC}	SCK duty cycle	—	$t_{SCK}/2$ - 10	$t_{SCK}/2$ + 10	—	—	ns
5	t_A	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	—	—	ns
6	t_{DIS}	Slave SOUT disable time	$_{SS}$ inactive to SOUT High-Z or invalid	—	10	—	—	ns
7	t_{PCSC}	PCSx to $\overline{PCSS}$ time	—	13	—	—	—	ns
8	t_{PASC}	$\overline{PCSS}$ to PCSx time	—	13	—	—	—	ns
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	NA	—	20	—	ns
			Slave	2	—	2	—	
			Master (MTFE = 1, CPHA = 0)	15	—	8[1, 1]	—	
			Master (MTFE = 1, CPHA = 1)	15	—	20	—	
10	t_{HI}	Data hold time for inputs	Master (MTFE = 0)	NA	—	–5	—	ns
			Slave	4	—	4	—	
			Master (MTFE = 1, CPHA = 0)	0	—	11[1]	—	
			Master (MTFE = 1, CPHA = 1)	0	—	-5	—	
11	t_{SUO}	Data valid (after SCK edge)	Master (MTFE = 0)	—	NA	—	4	ns
			Slave	—	15	—	23	
			Master (MTFE = 1, CPHA = 0)	—	4	—	16[1]	
			Master (MTFE = 1, CPHA = 1)	—	4	—	4	

Table continues on the next page...

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

6.4.2.2 TxEN

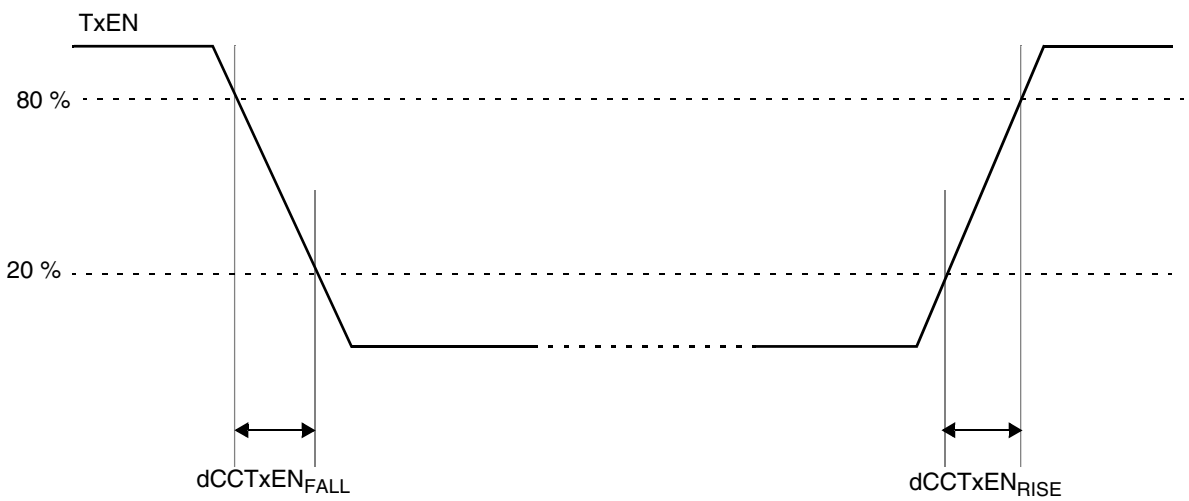

Figure 17. TxEN signal

Table 38. TxEN output characteristics[1]

Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxEN pin load maximum 25 pF

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = –40 oC / 150 oC.

6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 41. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

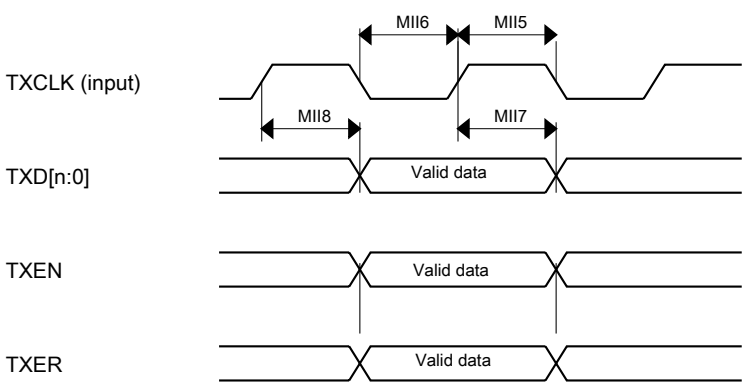

Figure 21. RMII/MII transmit signal timing diagram

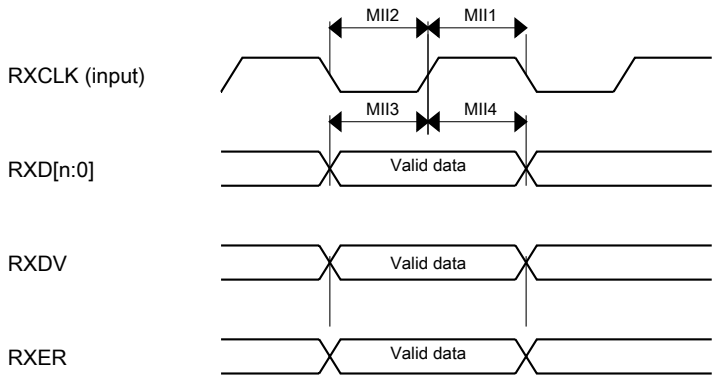

Figure 22. RMII/MII receive signal timing diagram

6.4.3.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 42. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

6.4.4 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 43. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns

Table continues on the next page...

Table 45. JTAG pin AC electrical characteristics [1] (continued)

#	Symbol	Characteristic	Min	Max	Unit
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

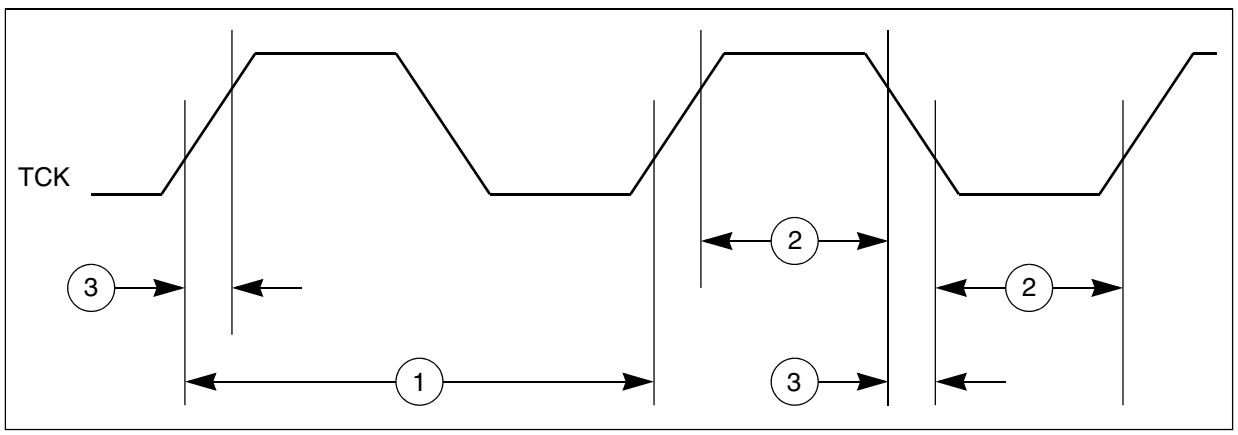

Figure 25. JTAG test clock input timing

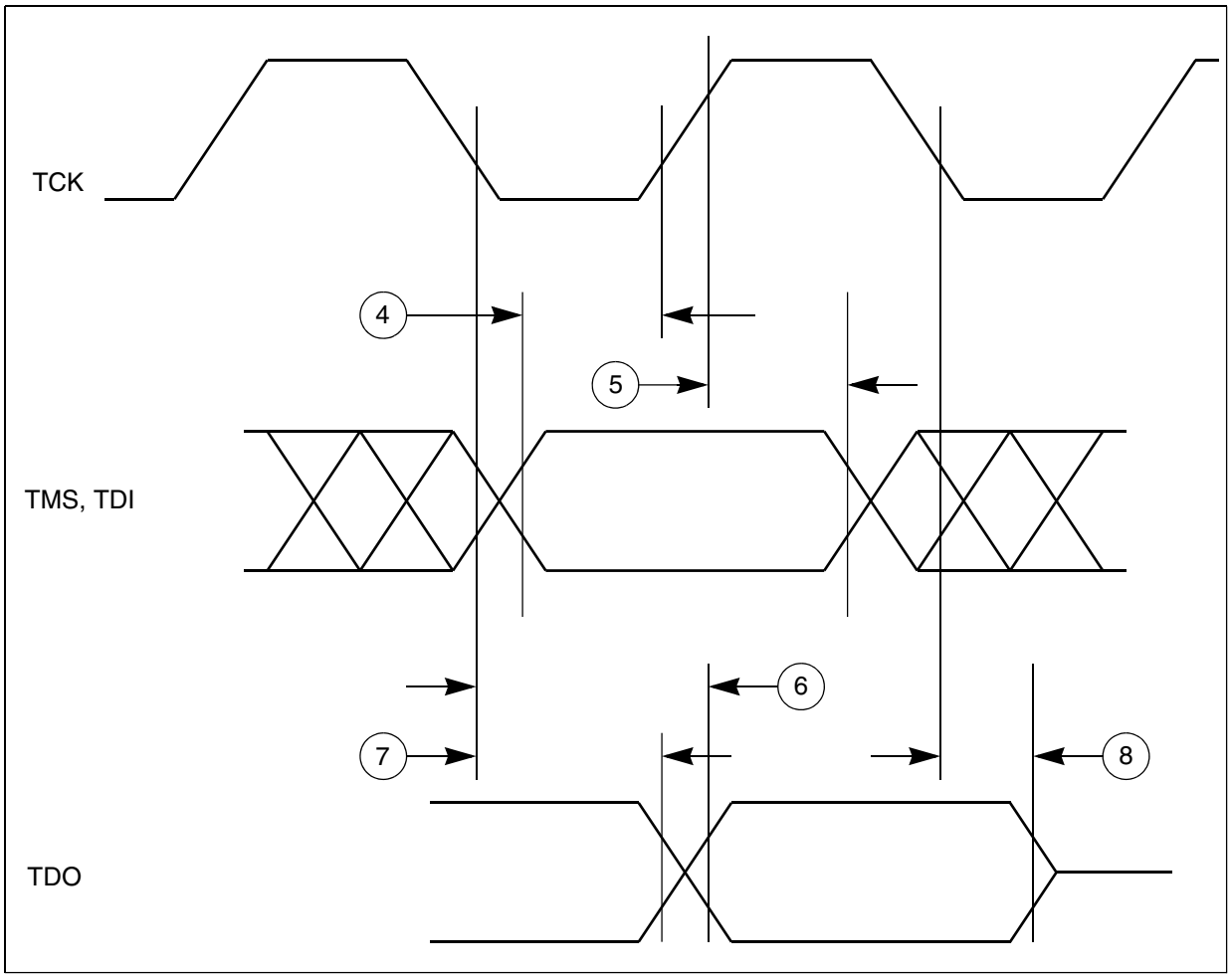

Figure 26. JTAG test access port timing

Table 46. Nexus debug port timing [1] (continued)

No.	Symbol	Parameter	Conditions	Min	Max	Unit
9	t_{NTDIH}, t_{NTMSH}	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

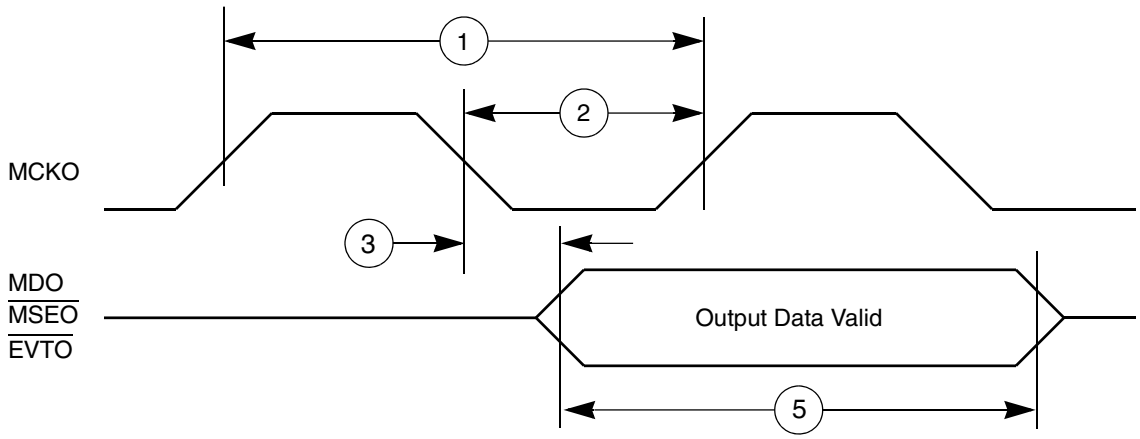

Figure 28. Nexus output timing

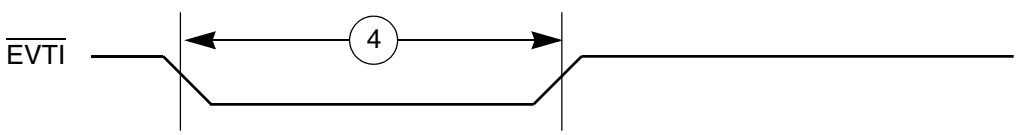

Figure 29. Nexus EVTI Input Pulse Width

Thermal attributes

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
—	$R_{\theta JC}$	Thermal resistance, junction to case	7.9	°C/W	55
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	66
—	$R_{\theta JB\_CSB}$	Thermal characterization parameter, junction to package bottom outside center (natural convection)	9.0	°C/W	77

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	100 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50.9	°C/W	1, 21,2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	27.0	°C/W	1,2,33
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	38.0	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	22.2	°C/W	1,3

Table continues on the next page...

Package	NXP Document Number
176-pin LQFP-EP	98ASA00698D
256 MAPBGA	98ASA00346D
324 MAPBGA	98ASA10582D

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

10.1 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1.1 Reset sequence duration

Table 49 specifies the reset sequence duration for the five different reset sequences described in Reset sequence description.

Table 49. RESET sequences

No.	Symbol	Parameter	T_{Reset}			Unit
			Min	Typ [1, 1]	Max	
1	T_{DRB}	Destructive Reset Sequence, BIST enabled	6.2	7.3	-	ms
2	T_{DR}	Destructive Reset Sequence, BIST disabled	110	182	-	us
3	T_{ERLB}	External Reset Sequence Long, Unsecure Boot	6.2	7.3	-	ms
4	T_{FRL}	Functional Reset Sequence Long, Unsecure Boot	110	182	-	us
5	T_{FRS}	Functional Reset Sequence Short, Unsecure Boot	7	9	-	us

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In section: Reset pad electrical characteristics
		  • Revised table, Reset electrical characteristics
		  • Deleted note, There are some specific ports that supports TTL functionality. These ports are, PB[4], PB[5], PB[6], PB[7], PB[8], PB[9], PD[0], PD[1], PD[2], PD[3], PD[4], PD[5], PD[6], PD[7], PD[8], PD[9], PD[10], and PD[11].
		• In section: PORST electrical specifications
		  • In table: PORST electrical specifications
		  • Updated 'Min' value for $W_{NFPORST}$
		• In section: Peripheral operating requirements and behaviours
		  • Changed section title from Input impedance and ADC accuracy to Input equivalent circuit and ADC conversion characteristics.
		  • Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit)
		  • Removed table, ADC supply configurations.
		• In section: Analogue Comparator (CMP) electrical specifications
		  • In table: Comparator and 6-bit DAC electrical specifications
		  • Updated 'Max' value of I_{DDLS}
		  • Updated 'Min' and 'Max' for V_{AIO} and DNL
		  • Updated 'Descripton' 'Min' 'Max' od V_H
		  • Updated row for t_{DHS}
		  • Added row for t_{DLS}
		  • Removed row for V_{CMPOh} and V_{CMPOl}
		• In section: Clocks and PLL interfaces modules
		  • In table: Main oscillator electrical characteristics
		  • V_{XOSCHS}: Removed values for 4 MHz.
		  • $T_{XOSCHSSU}$: Updated range to 8-40 MHz.
		  • In table: 16 MHz RC Oscillator electrical specifications
		  • Updated 'Max' for $T_{startup}$ and T_{LTJIT}
		  • Removed $F_{Untrimmed}$ row
		  • In table: 128 KHz Internal RC oscillator electrical specifications
		  • Fosc: Removed Uncaliberated 'Condition' and updated 'Min', 'Typ', and 'Max' for Caliberated condition
		  • Fosc: Updated 'Temperature dependence' and 'Supply dependence' Max values
		  • In table: PLL electrical specifications
		  • Removed entries for Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (V_{DD_LV}), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption
		  • Removed 'Typ' value for Duty Cycle at pllclkout
		  • Removed 'Min' value for Lock Time in calibration mode.
		  • In table: Jitter calculation
		  • Added 1 Sigma Random Jitter and Total Period Jitter values for Long Term Jitter (Interger and Fractional Mode) rows.

		• In section Flash read wait state and address pipeline control settings • In Flash Read Wait State and Address Pipeline Control: Updated APC for 40 MHz. • Removed section: On-chip peripherals

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

Rev 3	2 March 2016	• In section, Recommended operating conditions
		  • Added a new Note
		
		• In section, Voltage regulator electrical characteristics
		  • In table, Voltage regulator electrical specifications:
		  • Added a new row for $C_{HV\_VDD\_B}$
		  • Added a footnote on $V_{DD\_HV\_BALLAST}$
		  • Added a new Note at the end of this section
		
		• In section, Voltage monitor electrical characteristics
		  • In table, Voltage monitor electrical characteristics:
		  • Removed "V_{LVD_FLASH}" and "V_{LVD_FLASH} during low power mode using LPBG as reference" rows
		  • Updated Fall and Rise trimmed Minimum values for $V_{HVD\_LV\_cold}$
		
		• In section, Supply current characteristics
		  • In table, Current consumption characteristics:
		  • Updated the footnote mentioned in the Condition column of I_{DD_STOP} row
		  • Updated all TBD values
		  • In table, Low Power Unit (LPU) Current consumption characteristics:
		  • Updated the typical value of LPU_STOP to 0.18 mA
		  • Updated all TBD values
		  • In table, STANDBY Current consumption characteristics:
		  • Updated all TBD values
		
		• In section, AC specifications @ 3.3 V Range
		  • In table, Functional Pad AC Specifications @ 3.3 V Range:
		  • Updated Rise/Fall Edge values
		
		• In section, DC electrical specifications @ 3.3V Range
		  • In table, DC electrical specifications @ 3.3V Range:
		  • Updated Max value for Vol to 0.1 * VDD_HV_x
		
		• In section, AC specifications @ 5 V Range
		  • In table, Functional Pad AC Specifications @ 5 V Range:
		  • Updated Rise/Fall Edge values
		
		• In section, DC electrical specifications @ 5 V Range
		  • In table, DC electrical specifications @ 5 V Range:
		  • Updated Min and Max values for Pull_Ioh and Pull_Iol rows
		  • Updated Max value for Vol to 0.1 * VDD_HV_x
		
		• In section, Reset pad electrical characteristics
		  • In table, Functional reset pad electrical specifications:
		  • Updated parameter column for V_{IH}, V_{IL} and V_{HYS} rows
		  • Updated Min and Max values for V_{IH} and V_{IL} rows
		
		• In section, PORST electrical specifications
		  • In table, PORST electrical specifications:
		  • Updated Unit and Min/Max values for V_{IH} and V_{IL} rows
		
		• In section, Input equivalent circuit and ADC conversion characteristics
		  • In table, ADC conversion characteristics (for 12-bit):
		  • Updated "ADC Analog Pad (pad going to one ADC)" row
		  • In table, ADC conversion characteristics (for 10-bit):
		  • Updated "ADC Analog Pad (pad going to one ADC)" row
		
		• In section, Analog Comparator (CMP) electrical specifications
		  • In table, Comparator and 6-bit DAC electrical specifications:
		  • Updated Min and Max values for V_{AIO} to +47 mV
		  • Updated Max value for t_{DLS} to 21 µs
		
		• In section, Main oscillator electrical characteristics
		  • In table, Main oscillator electrical characteristics:

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev 5.1	22 May 2017	• Removed the Introduction section from Section 4 "General". • In AC Specifications@3.3V section, removed note related to Cz results and added two notes. • In AC Specifications@5V section, added two notes. • In ADC Electrical Specifications section, added spec value of "ADC Analog Pad" at Max leakage (standard channel)@ 105 C T_A in "ADC conversion characteristics (for 10-bit)" table. • In PLL Electrical Specifications section, updated the first footnote of "Jitter calculation" table. • In Analog Comparator Electrical Specifications section, updated the TDLS (propagation delay, low power mode) max value in "Comparator and 6-bit DAC electrical specifications" table to 21 us. • In Recommended Operating Conditions section, updated the footnote link to T_A in "Recommended operating conditions (V DD_HV_x = 5V)" table.