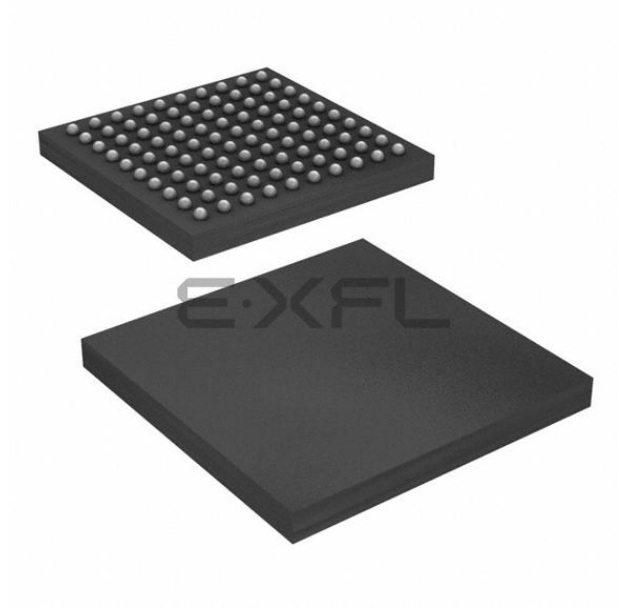

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, I²S, POR, WDT
Number of I/O	-
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 36x10b, 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	100-MAPBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746bfk1avmh6

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NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest number or address (e.g., FlexCAN0) and end at highest available number or address (e.g., MPC574xB/C have 6 CAN, ending with FlexCAN5).

Table 1. MPC5746C Family Comparison[1]

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C
CPUs	e200z4	e200z4	e200z4	e200z4 e200z2	e200z4 e200z2	e200z4 e200z2
FPU	e200z4	e200z4	e200z4	e200z4	e200z4	e200z4
Maximum Operating Frequency[2]	160MHz (Z4)	160MHz (Z4)	160MHz (Z4)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)
Flash memory	2 MB	1.5 MB	3 MB	1.5 MB	2 MB	3 MB
EEPROM support	Emulated up to 64K			Emulated up to 64K		
RAM	256 KB	192 KB	384 KB (Optional 512KB)[3, 3]	192 KB	256 KB	384 KB (Optional 512KB)[3]
ECC	End to End					
SMPU	16 entry					
DMA	32 channels					
10-bit ADC	36 Standard channels 32 External channels					
12-bit ADC	15 Precision channels 16 Standard channels					
Analog Comparator	3					
BCTU	1					
SWT	1, SWT[0][4]			2[4]		
STM	1, STM[0]			2		
PIT-RTI	16 channels PIT 1 channels RTI					
RTC/API	1					
Total Timer I/O[5]	64 channels 16-bits					
LINFlexD	1 Master and Slave (LINFlexD[0], 11 Master (LINFlexD[1:11])			1 Master and Slave (LINFlexD[0], 15 Master (LINFlexD[1:15])		
FlexCAN	6 with optional CAN FD support (FlexCAN[0:5])			8 with optional CAN FD support (FlexCAN[0:7])		
DSPI/SPI	4 x DSPI 4 x SPI					

Table continues on the next page...

Table 4. MPC5746C Family Comparison - RAM Memory Map (continued)

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40030000	0x4003FFFF	64 KB	SRAM4	not available	available	available
0x40040000	0x4004FFFF	64 KB	SRAM5	not available	not available	available
0x40050000	0x4005FFFF	64 KB	SRAM6	not available	not available	available
0x40060000	0x4006FFFF	64 KB	SRAM7	not available	not available	optional
0x40070000	0x4007FFFF	64 KB	SRAM8	not available	not available	optional

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5746C.

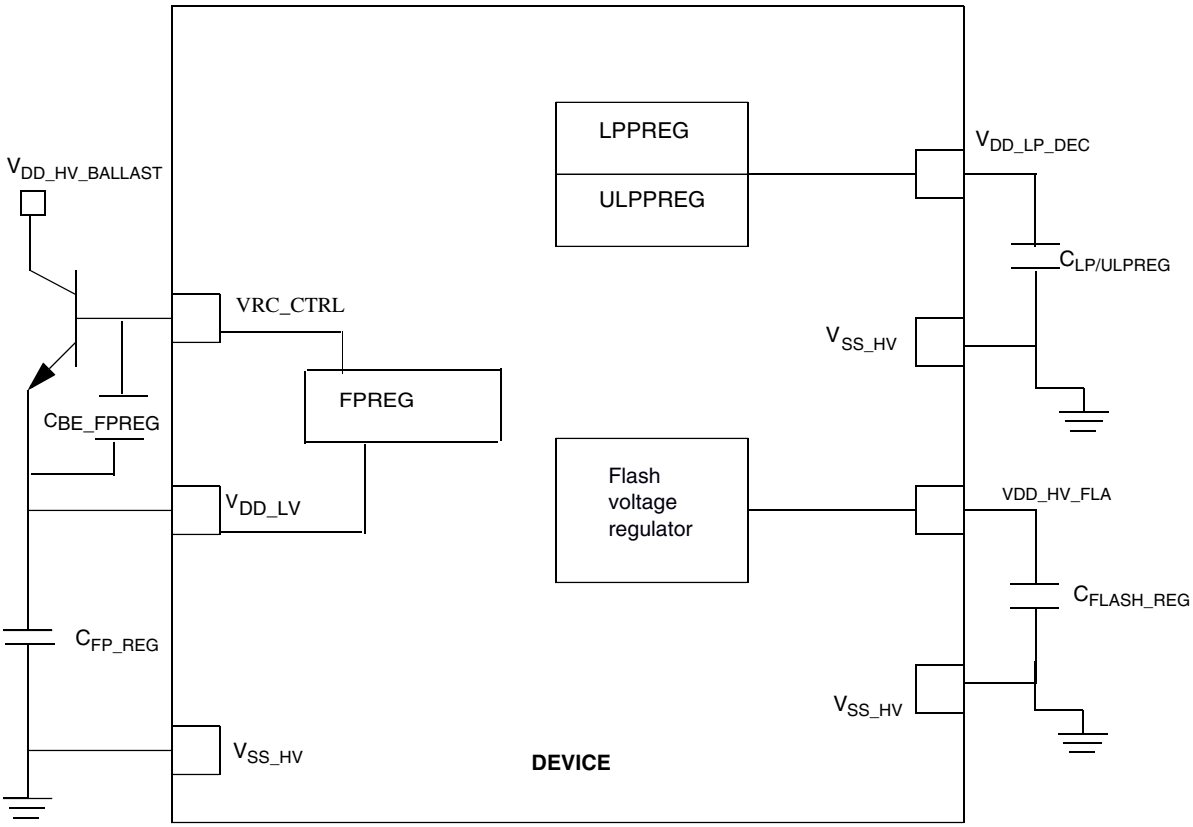


Figure 2. Voltage regulator capacitance connection

NOTE

On BGA, VSS_LV and VSS_HV have been joined on substrate and renamed as VSS.

Table 8. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{fp_reg}[1]	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2[2]	3	µF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
C_{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	µF
	Combined ESR of external capacitor	—	0.001	—	0.1	Ohm
C_{be_fpreg}[3]	Capacitor in parallel to base-emitter	BCP68 and BCP56		3.3		nF
		MJD31		4.7		

Table continues on the next page...

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_BODY\_2}$ 6	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125°C[5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	—	246	mA
		T_a = 105°C	—	—	235	mA
		T_a = 85°C	—	—	210	mA
$I_{DD\_BODY\_3}$ 7	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125 °C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	181	mA
		T_a = 105 °C	—	—	176	mA
		T_a = 85°C	—	—	171	mA
$I_{DD\_BODY\_4}$[8]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125 °C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	264	mA
		T_a = 105 °C	—	—	176	mA
		T_a = 85 °C	—	—	171	mA
I_{DD_STOP}	STOP mode Operating current	T_a = 125 °C[9] V_{DD_LV} = 1.25 V	—	—	49	mA
		T_a = 105 °C V_{DD_LV} = 1.25 V	—	10.6	—	
		T_a = 85 °C V_{DD_LV} = 1.25 V	—	8.1	—	
		T_a = 25 °C V_{DD_LV} = 1.25 V	—	4.6	—	

Table continues on the next page...

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 14. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry[2]	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01[3]
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00[3]
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input)[4]		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.
3. Slew rate control modes
4. Input slope = 2ns

NOTE

The specification given above is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The specification given above is measured between 20% / 80%.

Table 17. DC electrical specifications @ 5 V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Vil (pad_i_hv)	pad_i_hv Input Buffer Low Voltage	VDD_HV_x - 0.3	0.45*VDD_HV_x	V
Vhys (pad_i_hv)	pad_i_hv Input Buffer Hysteresis	0.09*VDD_HV_x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65* VDD_HV_x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VDD_HV_x - 0.3	0.35*VDD_HV_x	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * VDD_HV_x[1, 1]	VDD_HV_x[1] + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VDD_HV_x - 0.3	0.40 * VDD_HV_x[1]	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x[1]		V
Pull_IIH (pad_i_hv)	Weak Pullup Current[2, 2] Low	23		µA
Pull_IIH (pad_i_hv)	Weak Pullup Current[3, 3] High		82	µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[3] Low	40		µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[2] High		130	µA
Pull_Ioh	Weak Pullup Current[4]	30	80	µA
Pull_Iol	Weak Pulldown Current[5]	30	80	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[6]	0.8 * VDD_HV_x[1]	—	V
Vol	Output Low Voltage[7] Output Low Voltage[8]	—	0.2*VDD_HV_x 0.1*VDD_HV_x	V
Ioh_f	Full drive Ioh[9, 9] (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

6.1.1.1 Input equivalent circuit and ADC conversion characteristics

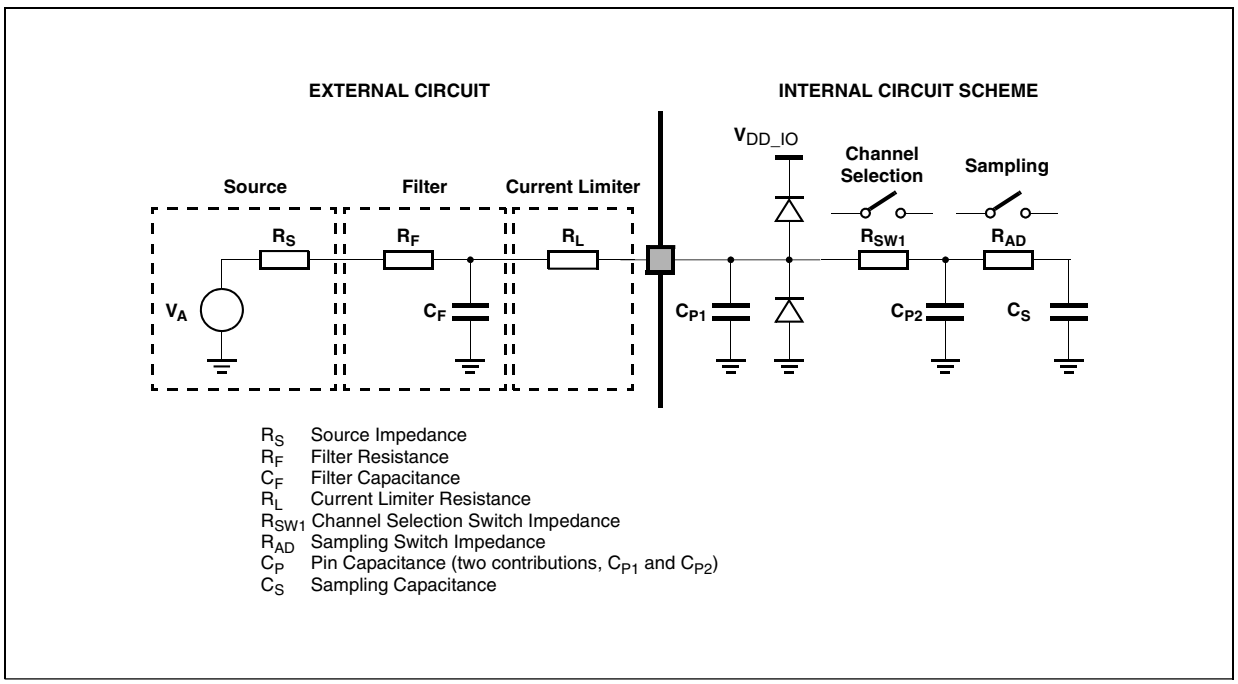


Figure 6. Input equivalent circuit

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

Table 20. ADC conversion characteristics (for 12-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	250	—	—	ns
t_{conv}	Conversion time[4]	80 MHz	700	—	—	ns
t_{total_conv}	Total Conversion time t_{sample} + t_{conv} (for standard and extended channels)	80 MHz	1.5[5]	—	—	µs
	Total Conversion time t_{sample} + t_{conv} (for precision channels)		1	—	—	
C_S[6, 6]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[6]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[6]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω

Table continues on the next page...

Table 20. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
R_{AD}[6]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity (precise channel)	—	–2	—	2	LSB
INL	Integral non-linearity (standard channel)	—	–3	—	3	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (precision channel)	150 °C	—	—	250	nA
	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C $_{TA}$	—	5	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{precision\ channels}$	Total unadjusted error for precision channels	Without current injection	–6	+/-4	6	LSB
		With current injection[7, 7]		+/-5		LSB
$TUE_{standard/extended\ channels}$	Total unadjusted error for standard/ extended channels	Without current injection	–8	+/-6	8	LSB
		With current injection[7]		+/-8		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	µs

1. Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 6.
7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

6.2.4 128 KHz Internal RC oscillator Electrical specifications

Table 26. 128 KHz Internal RC oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{oscu}[1]	Oscillator frequency	Calibrated	119	128	136.5	KHz
	Temperature dependence				600	ppm/C
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	µA
		Clock stopped			200	nA

1. Vdd=1.2 V, 1.32V, T_a=-40 C, 125 C

6.2.5 PLL electrical specifications

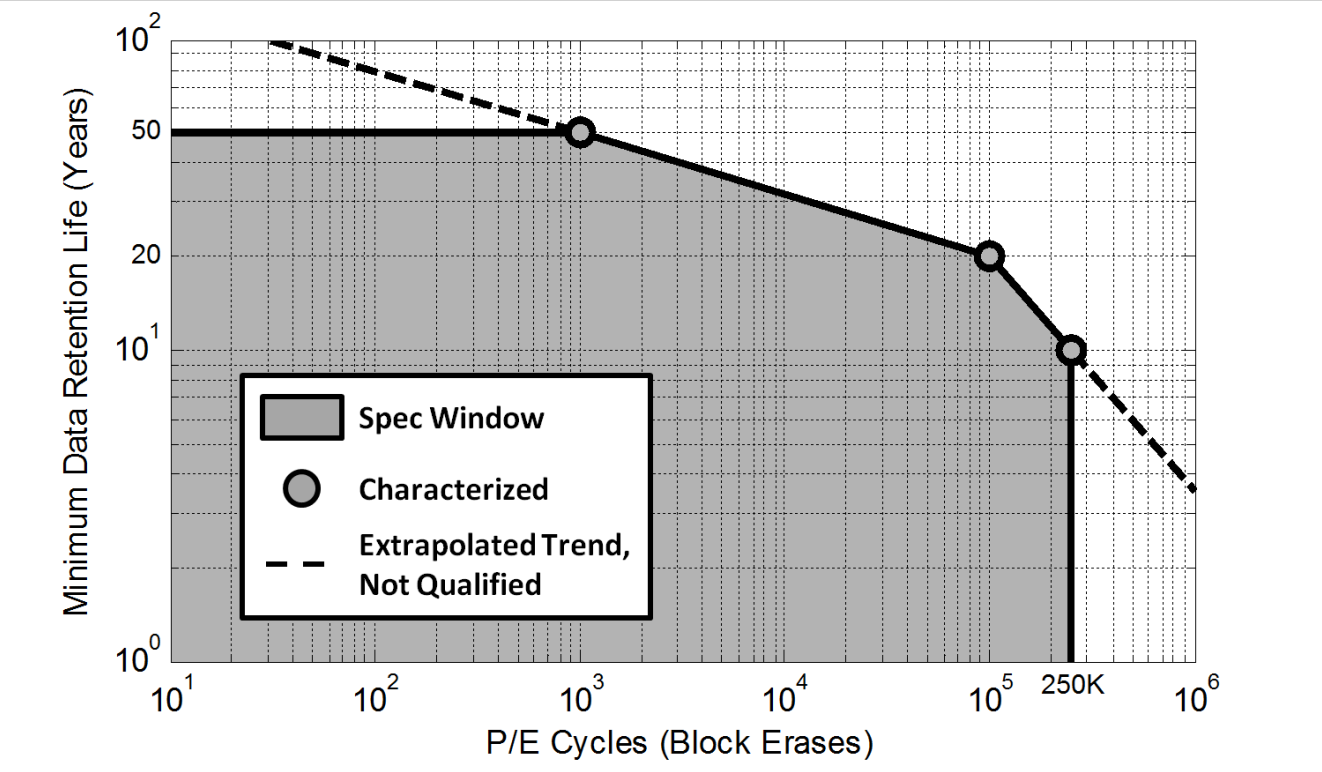
Table 27. PLL electrical specifications

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 28	ps	NON SSCG mode
TIE			See Table 28		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	µs	Calibration mode

Table 28. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN}[1]	Jitter due to Fractional Mode (ps) J_{SDM}[2]	Jitter due to Fractional Mode J_{SSCG} (ps) [3]	1 Sigma Random Jitter J_{RJ} (ps) [4]	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	+/-(J_{SN}+J_{SDM}+J_{SSCG}+N[4] ×J_{RJ})

Table continues on the next page...



6.3.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs

Table continues on the next page...

Table 45. JTAG pin AC electrical characteristics [1] (continued)

#	Symbol	Characteristic	Min	Max	Unit
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

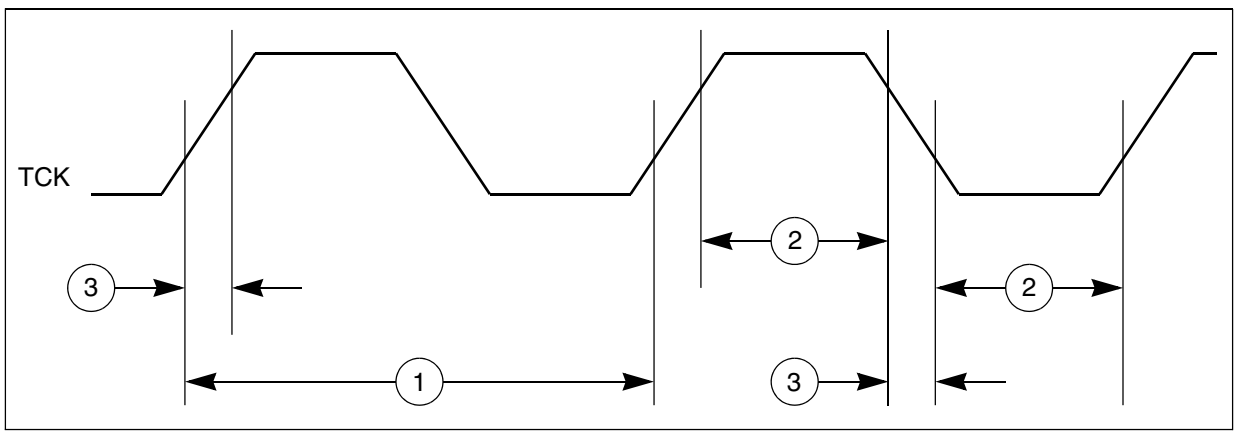


Figure 25. JTAG test clock input timing

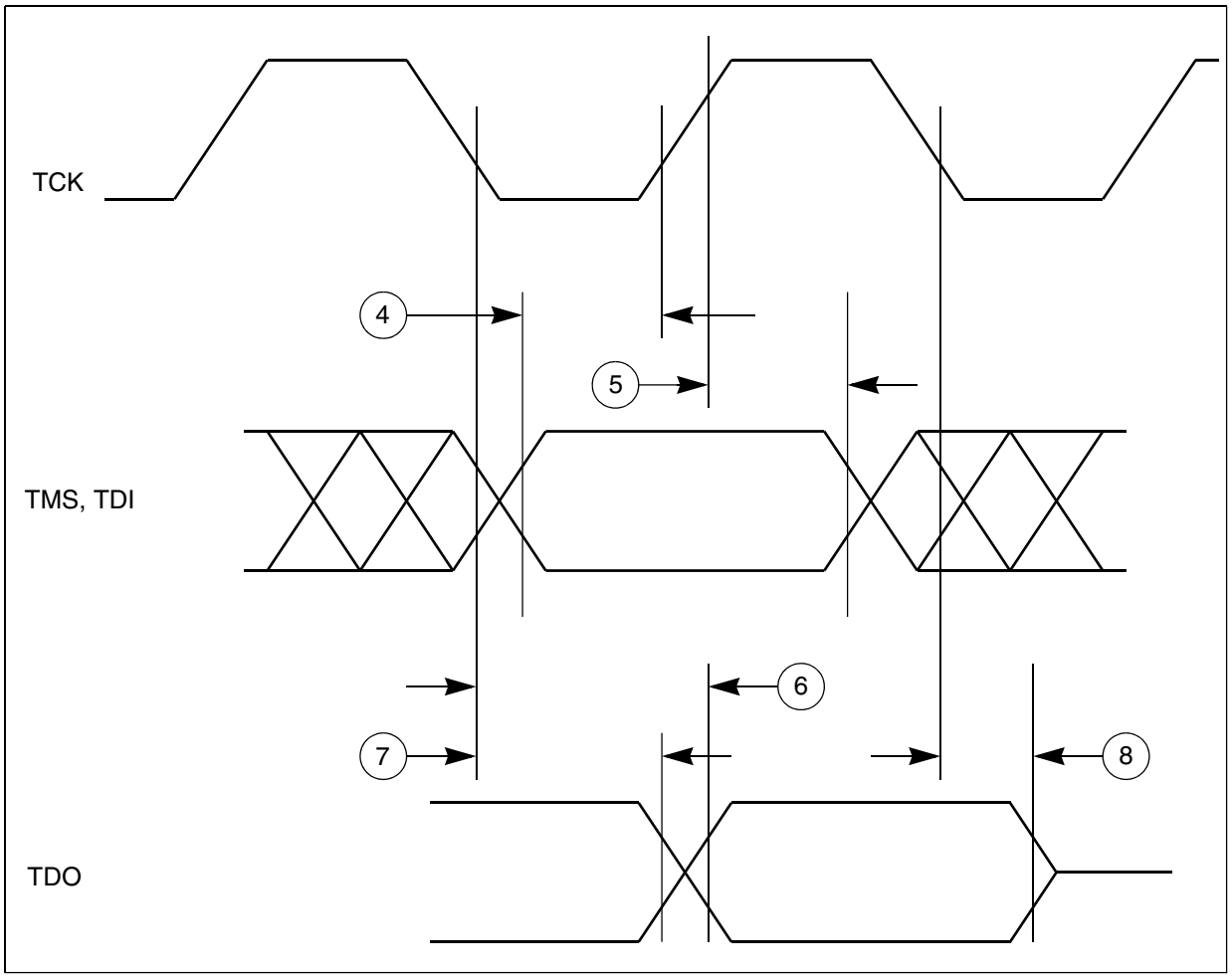


Figure 26. JTAG test access port timing

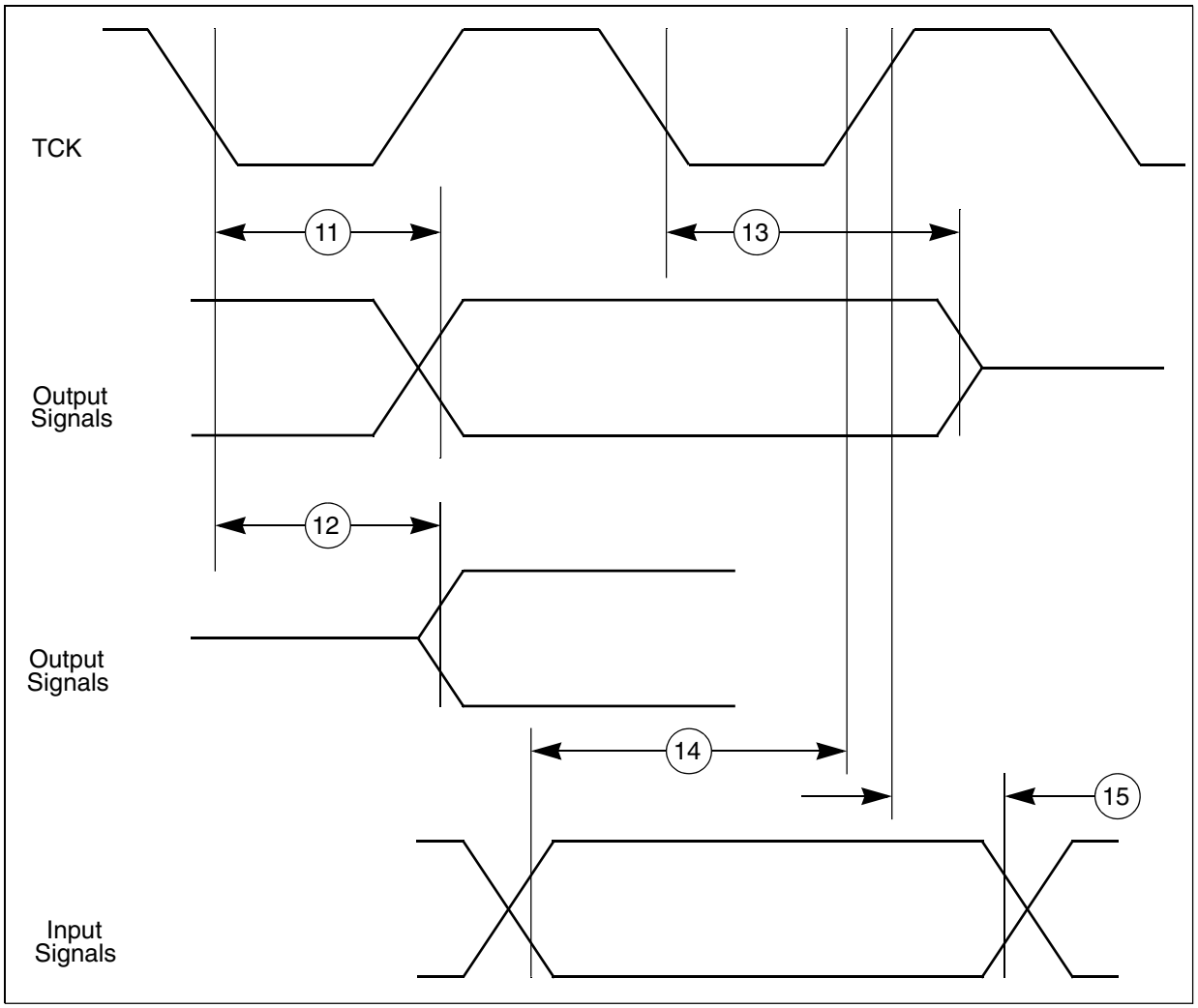


Figure 27. JTAG boundary scan timing

6.5.2 Nexus timing

Table 46. Nexus debug port timing [1]

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	tMCYC
4	t_{EVTIPW}	$\overline{\text{EVTI}}$ Pulse Width	—	4	—	tTCYC
5	t_{EVTOPW}	$\overline{\text{EVTO}}$ Pulse Width	—	1	—	tMCYC
6	t_{TCYC}	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	TDI, TMS Data Setup Time	—	8	—	ns

Table continues on the next page...

6.5.4 External interrupt timing (IRQ pin)

Table 48. External interrupt timing specifications

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time	—	6	—	t_{CYC}

These values applies when IRQ pins are configured for rising edge or falling edge events, but not both.

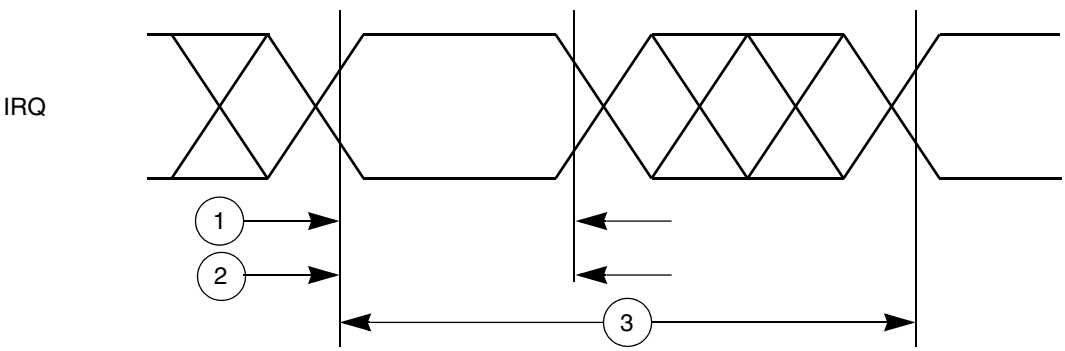


Figure 31. External interrupt timing

7 Thermal attributes

7.1 Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50.7	°C/W	11, 22
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	24.2	°C/W	1, 2, 33
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	38.1	°C/W	1, 3

Table continues on the next page...

10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

Table 50. BAF execution duration

BAF execution duration	Min	Typ	Max	Unit
BAF execution time (boot header at first location)	—	200	—	µs
BAF execution time (boot header at last location)	—	—	320	µs

10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

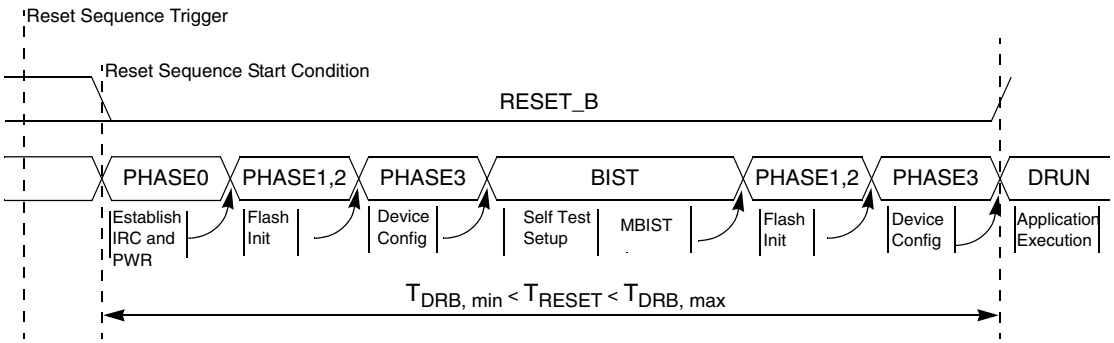


Figure 32. Destructive reset sequence, BIST enabled

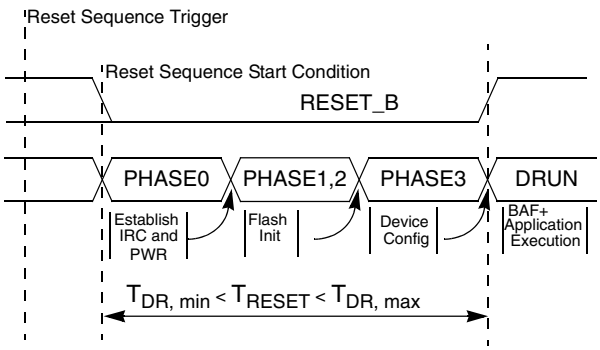


Figure 33. Destructive reset sequence, BIST disabled

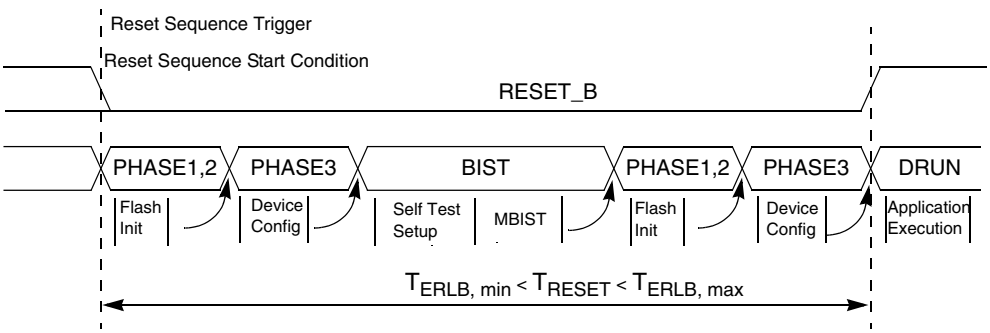


Figure 34. External reset sequence long, BIST enabled

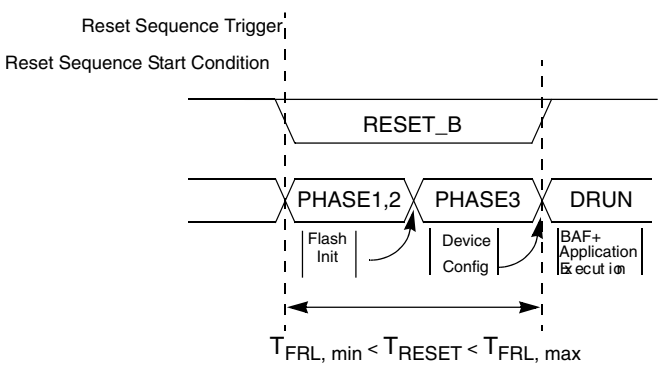


Figure 35. Functional reset sequence long

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In section, Thermal attributes
		  • Added table for 100 MAPBGA
		
		• In section Obtaining package dimensions
		  • Updated package details for 100 MAPBGA

		• Editoral updates throughtout including correction of various module names.

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

Rev 4	9 March 2016	• In section, Voltage regulator electrical characteristics
		  • In table, Voltage regulator electrical specifications:
		  • Updated the footnote on $V_{DD\_HV\_BALLAST}$

Rev 5	27 February 2017	• In Family Comparison section:
		  • Updated the "MPC5746C Family Comparison" table.
		  • added "NVM Memory Map 1", "NVM Memory Map 2", and "RAM Memory Map" tables.
		
		• Updated the product version, flash memory size and optional fields information in Ordering Information section.
		
		• In Recommended Operating Conditions section, removed the note related to additional crossover current.
		
		• VDD_HV_C row added in "Voltage regulator electrical specifications" table in Voltage regulator electrical characteristics section.
		
		• In Voltage Monitor Electrical Characteristics section, updated the "Trimmed" Fall and Rise specs of VHVD_LV_cold parameter in "Voltage Monitor Electrical Characteristics" table.
		
		• In AC Electrical Specifications: 3.3 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” in the table.
		• In DC Electrical Specifications: 3.3 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” and updated "Vol min and max" values in the table.
		• In AC Electrical Specifications: 5 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” in the table.
		• In DC Electrical Specifications: 5 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” and updated "Vol min and max" values in the table.
		
		• In "Flash memory AC timing specifications" table in Flash memory AC timing specifications section:
		  • Updated the "t_{psus}" typ value from 7 us to 9.4 us.
		  • Updated the "t_{psus}" max value from 9.1 us to 11.5 us.
		
		• Added "Continuous SCK Timing" table in DSPI timing section.
		
		• Added "ADC pad leakage" at 105°C TA conditions in "ADC conversion characteristics (for 12-bit)" table in ADC electrical specifications section.
		
		• In "STANDBY Current consumption characteristics" table in Supply current characteristics section:
		  • Updated the Typ and max values of IDD Standby current.
		  • Added IDD Standby3 current spec for FIRC ON.
		
		• Removed IVDDHV and IVDDLV specs in 16 MHz RC Oscillator electrical specifications section.
		
		• Added Reset Sequence section, with Reset Sequence Duration, BAF execution duration section, and Reset Sequence Distribution as its sub-sections.

Table continues on the next page...