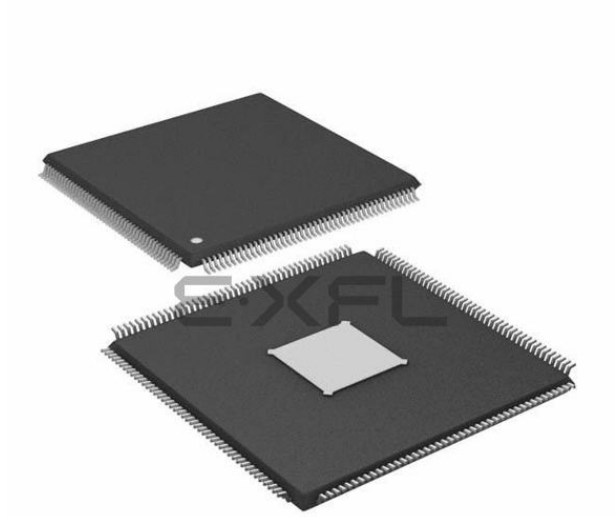

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, Ethernet, FlexRay, I²C, LINbus, SPI |
| Peripherals | DMA, I²S, POR, WDT |
| Number of I/O | 129 |
| Program Memory Size | 3MB (3M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 384K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.15V ~ 5.5V |
| Data Converters | A/D 36x10b, 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP Exposed Pad |
| Supplier Device Package | 176-LQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746bk1amku2 |

- Debug functionality
  - e200z2 core:NDI per IEEE-ISTO 5001-2008 Class3+
  - e200z4 core: NDI per IEEE-ISTO 5001-2008 Class 3+

- Timer
  - 16 Periodic Interrupt Timers (PITs)
  - Two System Timer Modules (STM)
  - Three Software Watchdog Timers (SWT)
  - 64 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels

- Device/board boundary Scan testing supported with Joint Test Action Group (JTAG) of IEEE 1149.1 and IEEE 1149.7 (CJTAG)

- Security
  - Hardware Security Module (HSMv2)
  - Password and Device Security (PASS) supporting advanced censorship and life-cycle management
  - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts

- Functional Safety
  - ISO26262 ASIL-B compliance

- Multiple operating modes
  - Includes enhanced low power operation

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**Table 4. MPC5746C Family Comparison - RAM Memory Map (continued)**

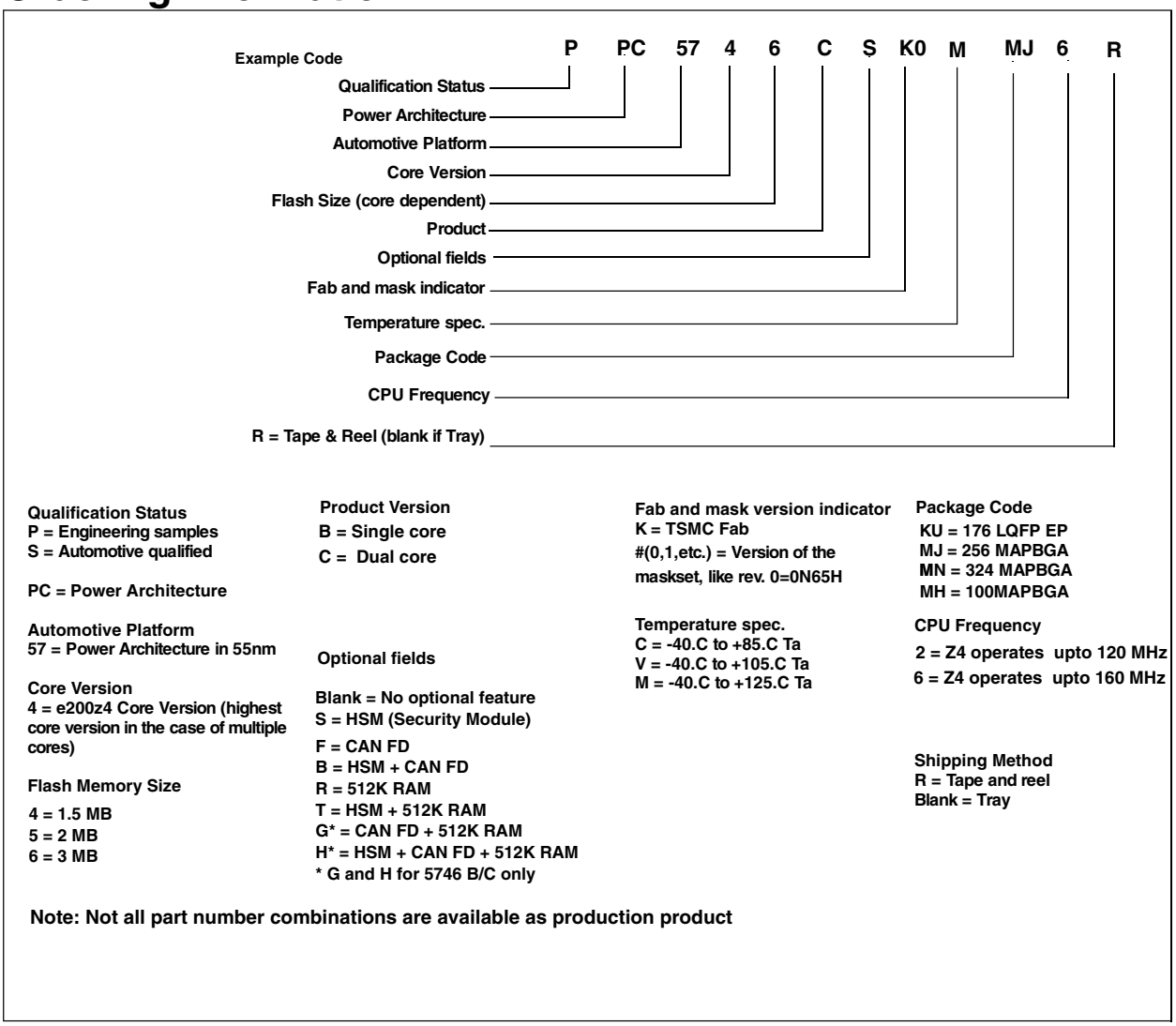
| Start Address | End Address | Allocated size | Description | MPC5744 | MPC5745 | MPC5746 |
|---|---|---|---|---|---|---|
| 0x40030000 | 0x4003FFFF | 64 KB | SRAM4 | not available | available | available |
| 0x40040000 | 0x4004FFFF | 64 KB | SRAM5 | not available | not available | available |
| 0x40050000 | 0x4005FFFF | 64 KB | SRAM6 | not available | not available | available |
| 0x40060000 | 0x4006FFFF | 64 KB | SRAM7 | not available | not available | optional |
| 0x40070000 | 0x4007FFFF | 64 KB | SRAM8 | not available | not available | optional |

# 3 Ordering parts

## 3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5746C.

## 3.2 Ordering Information




**Note: Not all part number combinations are available as production product**

# 4 General

## 4.1 Absolute maximum ratings

**NOTE**

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in Table 5 for specific conditions

## 4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

**NOTE**

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

**Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)**

| Symbol | Parameter | Conditions[1] | Min[2] | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD\_HV\_A}$<br>$V_{DD\_HV\_B}$<br>$V_{DD\_HV\_C}$ | HV IO supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_FLA}$[3] | HV flash supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_ADC1\_REF}$ | HV ADC1 high reference voltage | — | 3.0 | 5.5 | V |
| $V_{DD\_HV\_ADC0}$<br>$V_{DD\_HV\_ADC1}$ | HV ADC supply voltage | — | max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05 | 3.6 | V |
| $V_{SS\_HV\_ADC0}$<br>$V_{SS\_HV\_ADC1}$ | HV ADC supply ground | — | -0.1 | 0.1 | V |
| $V_{DD\_LV}$[4, 5] | Core supply voltage | — | 1.2 | 1.32 | V |
| $V_{IN1\_CMP\_REF}$[6, 7] | Analog Comparator DAC reference voltage | — | 3.15 | 3.6 | V |
| $I_{INJPAD}$ | Injected input current on any pin during overload condition | — | -3.0 | 3.0 | mA |

*Table continues on the next page...*

## Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V) (continued)

| Symbol | Parameter | Conditions[1] | Min[2] | Max | Unit |
|---|---|---|---|---|---|
| $T_A$[8] | Ambient temperature under bias | $f_{CPU}$ ≤ 160 MHz | –40 | 125 | °C |
| $T_J$ | Junction temperature under bias | — | –40 | 150 | °C |

1. All voltages are referred to $V_{SS\_HV}$ unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. Only applicable when supplying from external source.
5. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
6. VIN1_CMP_REF ≤ VDD_HV_A
7. This supply is shorted VDD_HV_A on lower packages.
8. $T_J$=150°C. Assumes $T_A$=125°C
   - Assumes maximum θJA of 2s2p board. See Thermal attributes

**NOTE**

If VDD_HV_A is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. VDD_HV_FLA should not be supplied externally and should only have decoupling capacitor.

## Table 7. Recommended operating conditions ($V_{DD\_HV\_x}$ = 5 V)

| Symbol | Parameter | Conditions [1] | Min[2] | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD\_HV\_A}$<br>$V_{DD\_HV\_B}$<br>$V_{DD\_HV\_C}$ | HV IO supply voltage | — | 4.5 | 5.5 | V |
| $V_{DD\_HV\_FLA}$[3] | HV flash supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_ADC1\_REF}$ | HV ADC1 high reference voltage | — | 3.15 | 5.5 | V |
| $V_{DD\_HV\_ADC0}$<br>$V_{DD\_HV\_ADC1}$ | HV ADC supply voltage | — | max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05 | 5.5 | V |
| $V_{SS\_HV\_ADC0}$<br>$V_{SS\_HV\_ADC1}$ | HV ADC supply ground | — | -0.1 | 0.1 | V |
| $V_{DD\_LV}$[4] | Core supply voltage | — | 1.2 | 1.32 | V |
| $V_{IN1\_CMP\_REF}$[5, 6] | Analog Comparator DAC reference voltage | — | 3.15 | 5.5[5] | V |
| $I_{INJPAD}$ | Injected input current on any pin during overload condition | — | -3.0 | 3.0 | mA |
| $T_A$[7] | Ambient temperature under bias | $f_{CPU}$ ≤ 160 MHz | –40 | 125 | °C |
| $T_J$ | Junction temperature under bias | — | –40 | 150 | °C |

1. All voltages are referred to $V_{SS\_HV}$ unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. When VDD_HV is in 5 V range, VDD_HV_FLA cannot be supplied externally.This pin is decoupled with $C_{flash\_reg}$.

4. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. VIN1_CMP_REF ≤ VDD_HV_A
6. This supply is shorted VDD_HV_A on lower packages.
7. $T_J$=150°C. Assumes $T_A$=125°C
    - Assumes maximum θJA of 2s2p board. See Thermal attributes

## 4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
    - Control of external NPN ballast transistor
    - Generating core supply using internal ballast transistor
    - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector (LVD_FLASH) for 3.3 V flash supply (VDD_HV_FLA)
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

1. BCP56, MCP68 and MJD31are guaranteed ballasts.

**Table 9. Voltage monitor electrical characteristics (continued)**

| Symbol | Parameter | State | Conditions | Configuration | | | Threshold | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Power Up [1] | Mask Opt[2, 2] | Reset Type | Min | Typ | Max | V |
| $V_{LVD\_LV\_PD2\_cold}$ | LV supply low voltage monitoring, detecting at the device pin | Fall | Untrimmed | No | Yes | Functional | Disabled at Start | | | |
| | | | Trimmed | | | | 1.1400 | 1.1550 | 1.1750 | V |
| | | Rise | Untrimmed | | | | Disabled at Start | | | |
| | | | Trimmed | | | | 1.1600 | 1.1750 | 1.1950 | V |

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.
3. There is no voltage monitoring on the $V_{DD\_HV\_ADC0}$, $V_{DD\_HV\_ADC1}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ I/O segments. For applications requiring monitoring of these segments, either connect these to $V_{DD\_HV\_A}$ at the PCB level or monitor externally.

## 4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

**NOTE**

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

**Table 10. Current consumption characteristics**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_BODY\_1}$ [2, 3] | RUN Body Mode Profile Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4, 4] $T_a$ = 125°C [5, 5] $V_{DD\_LV}$ = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 80MHz | — | — | 147 | mA |
| | | $T_a$ = 105°C | — | — | 142 | mA |
| | | $T_a$ = 85 °C | — | — | 137 | mA |

*Table continues on the next page...*

## Table 10. Current consumption characteristics (continued)

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_BODY\_2}$ 6 | RUN Body Mode Profile Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4]<br>$T_a$ = 125°C[5]<br>$V_{DD\_LV}$ = 1.25 V<br>VDD_HV_A = 5.5V<br>SYS_CLK = 160MHz | — | — | 246 | mA |
| | | $T_a$ = 105°C | — | — | 235 | mA |
| | | $T_a$ = 85°C | — | — | 210 | mA |
| $I_{DD\_BODY\_3}$ 7 | RUN Body Mode Profile Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4]<br>$T_a$ = 125 °C [5]<br>$V_{DD\_LV}$ = 1.25 V<br>VDD_HV_A = 5.5V<br>SYS_CLK = 120MHz | — | — | 181 | mA |
| | | $T_a$ = 105 °C | — | — | 176 | mA |
| | | $T_a$ = 85°C | — | — | 171 | mA |
| $I_{DD\_BODY\_4}$[8] | RUN Body Mode Profile Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4]<br>$T_a$ = 125 °C [5]<br>$V_{DD\_LV}$ = 1.25 V<br>VDD_HV_A = 5.5V<br>SYS_CLK = 120MHz | — | — | 264 | mA |
| | | $T_a$ = 105 °C | — | — | 176 | mA |
| | | $T_a$ = 85 °C | — | — | 171 | mA |
| $I_{DD\_STOP}$ | STOP mode Operating current | $T_a$ = 125 °C[9]<br>$V_{DD\_LV}$ = 1.25 V | — | — | 49 | mA |
| | | $T_a$ = 105 °C<br>$V_{DD\_LV}$ = 1.25 V | — | 10.6 | — | |
| | | $T_a$ = 85 °C<br>$V_{DD\_LV}$ = 1.25 V | — | 8.1 | — | |
| | | $T_a$ = 25 °C<br>$V_{DD\_LV}$ = 1.25 V | — | 4.6 | — | |

*Table continues on the next page...*

## Table 10. Current consumption characteristics (continued)

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_HV\_ADC\_REF}$[10, 11, 11] | ADC REF Operating current | $T_a$ = 125 °C[5]<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 5.5 V | — | 200 | 400 | µA |
| | | $T_a$ = 105 °C<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 5.5 V | — | 200 | — | |
| | | $T_a$ = 85 °C<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 5.5 V | — | 200 | — | |
| | | $T_a$ = 25 °C<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 3.6 V | — | 200 | — | |
| $I_{DD\_HV\_ADCx}$[11] | ADC HV Operating current | $T_a$ = 125 °C[5]<br>ADC operating at 80 MHz<br>$V_{DD\_HV\_ADC}$ = 5.5 V | — | 1.2 | 2 | mA |
| | | $T_a$ = 25 °C<br>ADC operating at 80 MHz<br>$V_{DD\_HV\_ADC}$ = 3.6 V | — | 1 | 2 | |
| $I_{DD\_HV\_FLASH}$[12] | Flash Operating current during read access | $T_a$ = 125 °C[5]<br>3.3 V supplies<br>160 MHz frequency | — | 40 | 45 | mA |
| | | $T_a$ = 105 °C<br>3.3 V supplies<br>160 MHz frequency | — | 40 | 45 | |
| | | $T_a$ = 85 °C<br>3.3 V supplies<br>160 MHz frequency | — | 40 | 45 | |

1. The content of the Conditions column identifies the components that draw the specific current.
2. Single e200Z4 core cache disabled @80 MHz, no FlexRay, no ENET, 2 x CAN, 8 LINFlexD, 2 SPI, ADC0 and 1 used constantly, no HSM, Memory: 2M flash, 128K RAM RUN mode, Clocks: FIRC on, XOSC, PLL on, SIRC on for TOD, no 32KHz crystal (TOD runs off SIRC).
3. Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C. In case of internal ballast mode, it is expected that the external ballast is not mounted and BAL_SELECT_INT pin is tied to VDD_HV_A supply on board. Internal ballast can be used for all use cases with current consumption upto 150mA
4. The power consumption does not consider the dynamic current of I/Os
5. Tj=150°C. Assumes Ta=125°C
   - Assumes maximum θJA of 2s2p board. SeeThermal attributes
6. e200Z4 core, 160MHz, cache enabled; e200Z2 core , 80MHz, no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 256K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
7. e200Z4 core, 120MHz, cache enabled; e200Z2 core, 60MHz; no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 128K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal

## 4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

# 5 I/O parameters

## 5.1 AC specifications @ 3.3 V Range

**Table 14. Functional Pad AC Specifications @ 3.3 V Range**

| Symbol | Prop. Delay (ns)[1] L>H/H>L | | Rise/Fall Edge (ns) | | Drive Load (pF) | SIUL2_MSCRn[SRC 1:0] |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | MSB,LSB |
| pad_sr_hv (output) | | 6/6 | | 1.9/1.5 | 25 | 11 |
| | 2.5/2.5 | 8.25/7.5 | 0.8/0.6 | 3.25/3 | 50 | |
| | 6.4/5 | 19.5/19.5 | 3.5/2.5 | 12/12 | 200 | |
| | 2.2/2.5 | 8/8 | 0.55/0.5 | 3.9/3.5 | 25 | 10 |
| | 0.090 | 1.1 | 0.035 | 1.1 | asymmetry[2] | |
| | 2.9/3.5 | 12.5/11 | 1/1 | 7/6 | 50 | |
| | 11/8 | 35/31 | 7.7/5 | 25/21 | 200 | |
| | 8.3/9.6 | 45/45 | 4/3.5 | 25/25 | 50 | 01[3] |
| | 13.5/15 | 65/65 | 6.3/6.2 | 30/30 | 200 | |
| | 13/13 | 75/75 | 6.8/6 | 40/40 | 50 | 00[3] |
| | 21/22 | 100/100 | 11/11 | 51/51 | 200 | |
| pad_i_hv/ pad_sr_hv (input)[4] | | 2/2 | | 0.5/0.5 | 0.5 | NA |

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.
3. Slew rate control modes
4. Input slope = 2ns

**NOTE**

The specification given above is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

**NOTE**

The specification given above is measured between 20% / 80%.

## 5.2 DC electrical specifications @ 3.3V Range

**Table 15. DC electrical specifications @ 3.3V Range**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Vih (pad_i_hv) | Pad_I_HV Input Buffer High Voltage | 0.72*VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil (pad_i_hv) | Pad_I_HV Input Buffer Low Voltage | VDD_HV_x - 0.3 | 0.45*VDD_HV_x | V |
| Vhys (pad_i_hv) | Pad_I_HV Input Buffer Hysteresis | 0.11*VDD_HV_x | | V |
| Vih_hys | CMOS Input Buffer High Voltage (with hysteresis enabled) | 0.67*VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil_hys | CMOS Input Buffer Low Voltage (with hysteresis enabled) | VDD_HV_x - 0.3 | 0.35*VDD_HV_x | V |
| Vih | CMOS Input Buffer High Voltage (with hysteresis disabled) | 0.57 * VDD_HV_x[1, 1] | VDD_HV_x[1] + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage (with hysteresis disabled) | VDD_HV_x - 0.3 | 0.4 * VDD_HV_x[1] | V |
| Vhys | CMOS Input Buffer Hysteresis | 0.09 * VDD_HV_x[1] | | V |
| Pull_IIH (pad_i_hv) | Weak Pullup Current[2, 2] Low | 15 | | µA |
| Pull_IIH (pad_i_hv) | Weak Pullup Current[3, 3] High | | 55 | µA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current[3] Low | 28 | | µA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current[2] High | | 85 | µA |
| Pull_Ioh | Weak Pullup Current[4] | 15 | 50 | µA |
| Pull_Iol | Weak Pulldown Current[5] | 15 | 50 | µA |
| Iinact_d | Digital Pad Input Leakage Current (weak pull inactive) | -2.5 | 2.5 | µA |
| Voh | Output High Voltage[6] | 0.8 *VDD_HV_x[1] | — | V |
| Vol | Output Low Voltage[7]<br>Output Low Voltage[8] | — | 0.2 *VDD_HV_x[1]<br>0.1 *VDD_HV_x | V |
| Ioh_f | Full drive Ioh[9, 9] (SIUL2_MSCRn.SRC[1:0] = 11) | 18 | 70 | mA |
| Iol_f | Full drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 11) | 21 | 120 | mA |
| Ioh_h | Half drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 10) | 9 | 35 | mA |
| Iol_h | Half drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 10) | 10.5 | 60 | mA |

1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

## Table 20. ADC conversion characteristics (for 12-bit) (continued)

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{AD}$[6] | Internal resistance of analog source | — | — | — | 825 | Ω |
| INL | Integral non-linearity (precise channel) | — | –2 | — | 2 | LSB |
| INL | Integral non-linearity (standard channel) | — | –3 | — | 3 | LSB |
| DNL | Differential non-linearity | — | –1 | — | 1 | LSB |
| OFS | Offset error | — | –6 | — | 6 | LSB |
| GNE | Gain error | — | –4 | — | 4 | LSB |
| ADC Analog Pad (pad going to one ADC) | Max leakage (precision channel) | 150 °C | — | — | 250 | nA |
| | Max leakage (standard channel) | 150 °C | — | — | 2500 | nA |
| | Max leakage (standard channel) | 105 °C $_{TA}$ | — | 5 | 250 | nA |
| | Max positive/negative injection | | –5 | — | 5 | mA |
| $TUE_{precision\ channels}$ | Total unadjusted error for precision channels | Without current injection | –6 | +/-4 | 6 | LSB |
| | | With current injection[7, 7] | | +/-5 | | LSB |
| $TUE_{standard/extended\ channels}$ | Total unadjusted error for standard/ extended channels | Without current injection | –8 | +/-6 | 8 | LSB |
| | | With current injection[7] | | +/-8 | | LSB |
| $t_{recovery}$ | STOP mode to Run mode recovery time | | | | < 1 | µs |

1. Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_{sample}$. After the end of the sample time $t_{sample}$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_{sample}$ depend on programming.
4. This parameter does not include the sample time $t_{sample}$, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 6.
7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

## Table 21. ADC conversion characteristics (for 10-bit)

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}$ | ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.) | — | 15.2 | 80 | 80 | MHz |
| $f_s$ | Sampling frequency | — | — | — | 1.00 | MHz |
| $t_{sample}$ | Sample time[3] | 80 MHz@ 100 ohm source impedance | 275 | — | — | ns |

*Table continues on the next page...*

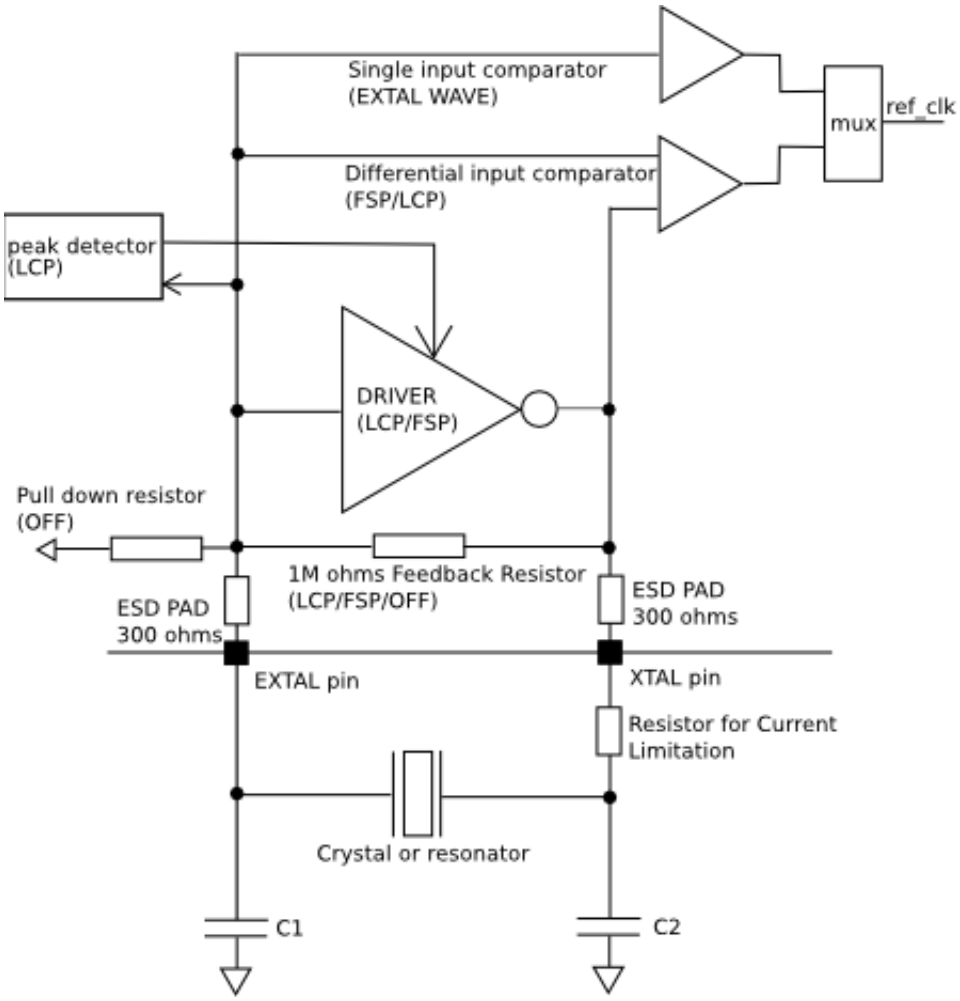



**Figure 7. Oscillator connections scheme**

## Table 23. Main oscillator electrical characteristics

| Symbol | Parameter | Mode | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{XOSCHS}$ | Oscillator frequency | FSP/LCP | | 8 | | 40 | MHz |
| $g_{mXOSCHS}$ | Driver Transconductance | LCP | | | 23 | | mA/V |
| | | FSP | | | 33 | | |
| $V_{XOSCHS}$ | Oscillation Amplitude | LCP[1, 2, 1, 2] | 8 MHz | | 1.0 | | $V_{PP}$ |
| | | | 16 MHz | | 1.0 | | |
| | | | 40 MHz | | 0.8 | | |
| $T_{XOSCHSSU}$ | Startup time | FSP/LCP[1] | 8 MHz | | 2 | | ms |
| | | | 16 MHz | | 1 | | |
| | | | 40 MHz | | 0.5 | | |

*Table continues on the next page...*

**Table 23. Main oscillator electrical characteristics (continued)**

| Symbol | Parameter | Mode | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | Oscillator Analog Circuit supply current | FSP | 8 MHz | | 2.2 | | mA |
| | | | 16 MHz | | 2.2 | | |
| | | | 40 MHz | | 3.2 | | |
| | | LCP | 8 MHz | | 141 | | uA |
| | | | 16 MHz | | 252 | | |
| | | | 40 MHz | | 518 | | |
| $V_{IH}$ | Input High level CMOS Schmitt trigger | EXT Wave | Oscillator supply=3.3 | 1.95 | | | V |
| $V_{IL}$ | Input low level CMOS Schmitt trigger | EXT Wave | Oscillator supply=3.3 | | | 1.25 | V |

1. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board.
2. Typ value for oscillator supply 3.3 V@27 °C

## 6.2.2 32 kHz Oscillator electrical specifications

**Table 24. 32 kHz oscillator electrical specifications**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency | | 32 | | 40 | KHz |
| $t_{cst}$ | Crystal Start-up Time[1, 2] | | | | 2 | s |

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

## 6.2.3 16 MHz RC Oscillator electrical specifications

**Table 25. 16 MHz RC Oscillator electrical specifications**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{Target}$ | IRC target frequency | — | — | 16 | — | MHz |
| PTA | IRC frequency variation after trimming | — | -5 | — | 5 | % |
| $T_{startup}$ | Startup time | — | | — | 1.5 | us |
| $T_{STJIT}$ | Cycle to cycle jitter | | — | — | 1.5 | % |
| $T_{LTJIT}$ | Long term jitter | | — | — | 0.2 | % |

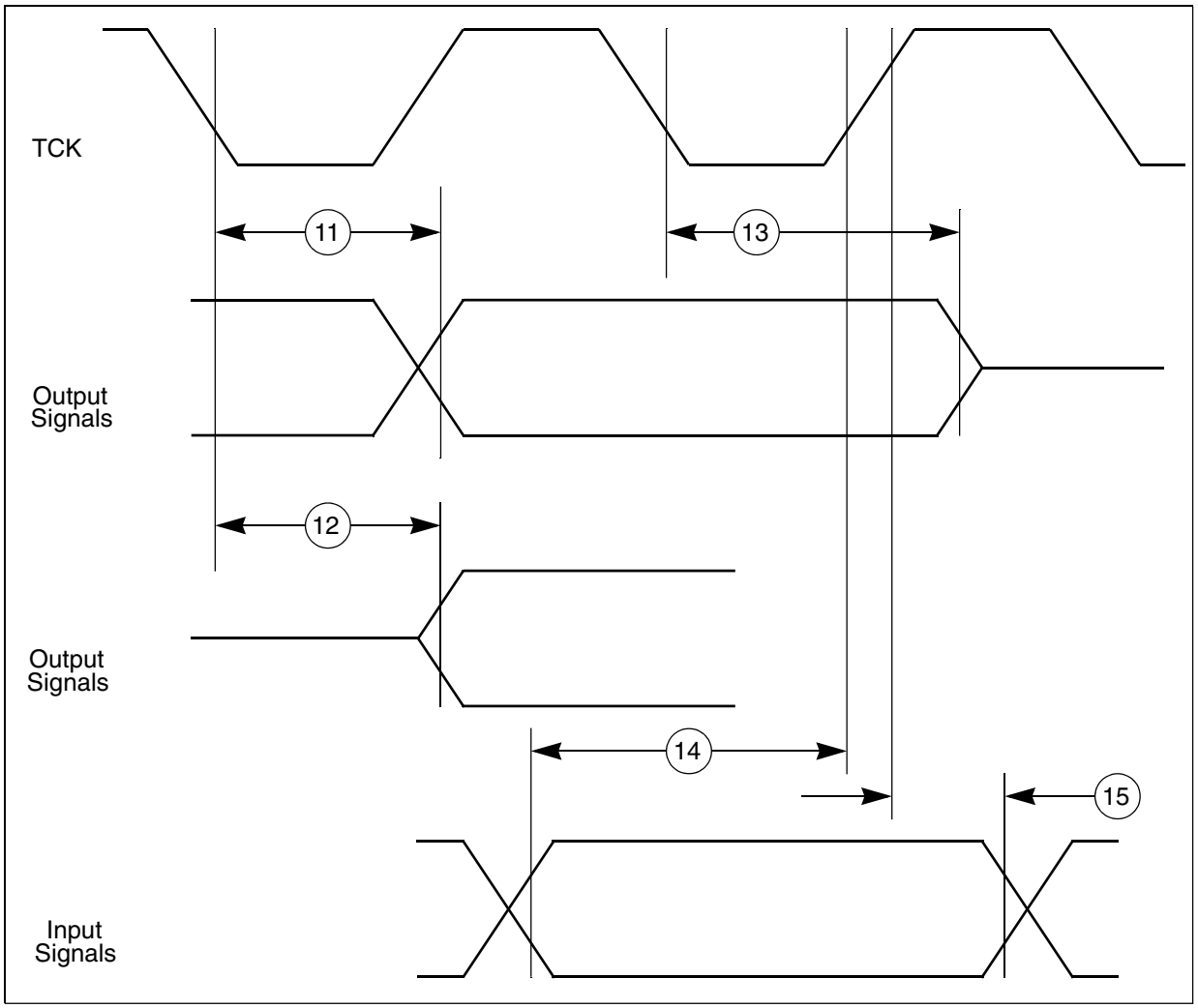



**Figure 27. JTAG boundary scan timing**

## 6.5.2 Nexus timing

### Table 46. Nexus debug port timing [1]

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | $t_{MCYC}$ | MCKO Cycle Time | — | 15.6 | — | ns |
| 2 | $t_{MDC}$ | MCKO Duty Cycle | — | 40 | 60 | % |
| 3 | $t_{MDOV}$ | MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2] | — | –0.1 | 0.25 | tMCYC |
| 4 | $t_{EVTIPW}$ | $\overline{\text{EVTI}}$ Pulse Width | — | 4 | — | tTCYC |
| 5 | $t_{EVTOPW}$ | $\overline{\text{EVTO}}$ Pulse Width | — | 1 | — | tMCYC |
| 6 | $t_{TCYC}$ | TCK Cycle Time[3] | — | 62.5 | — | ns |
| 7 | $t_{TDC}$ | TCK Duty Cycle | — | 40 | 60 | % |
| 8 | $t_{NTDIS}$, $t_{NTMSS}$ | TDI, TMS Data Setup Time | — | 8 | — | ns |

*Table continues on the next page...*

## Table 46. Nexus debug port timing [1] (continued)

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 9 | $t_{NTDIH}$, $t_{NTMSH}$ | TDI, TMS Data Hold Time | — | 5 | — | ns |
| 10 | $t_{JOV}$ | TCK Low to TDO/RDY Data Valid | — | 0 | 25 | ns |

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

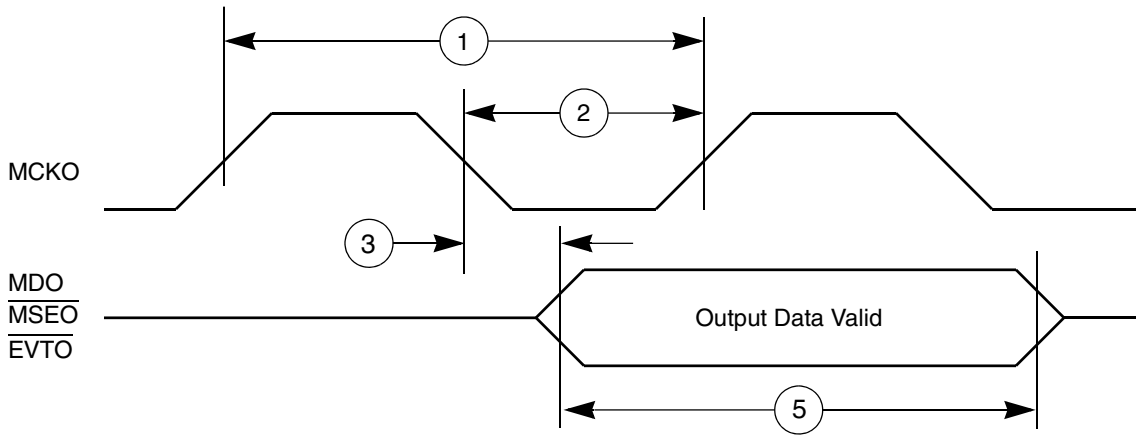



**Figure 28. Nexus output timing**

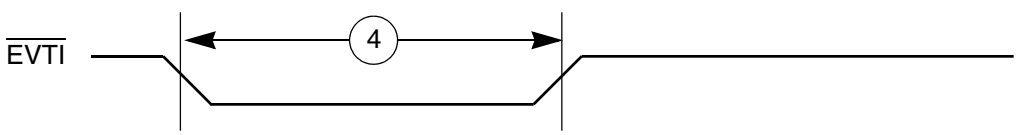



**Figure 29. Nexus EVTI Input Pulse Width**

## Table 51. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| Rev 2 | 7 August 2015 | • In features:<br>  • Updated BAF feature with sentence, Boot Assist Flash (BAF) supports internal flash programming via a serial link (SCI)<br>  • Updated FlexCAN3 with FD support<br>  • Updated number of STMs to two.<br>• In Block diagram:<br>  • Updated SRAM size from 128 KB to 256 KB.<br>• In Family Comparison:<br>  • Added note: All optional features (Flash memory, RAM, Peripherals) start with lowest number or address (e.g. FlexCAN0) and end at highest available number or address (e.g. MPC574xB/D have 6 CAN, ending with FlexCAN5).<br>  • Revised MPC5746C Family Comparison table.<br>• In Ordering parts:<br>  • Updated ordering parts diagram to include 100 MAPBGA information and optional fields.<br>• In table: Absolute maximum ratings<br>  • Removed entry: '$V_{SS\_HV}$'<br>  • Added spec for '$V_{DD12}$'<br>  • Updated 'Max' column for '$V_{INA}$'<br>  • Updated footnote for $V_{DD\_HV\_ADC1\_REF}$.<br>  • Added footnote to 'Conditions', All voltages are referred to $V_{SS\_HV}$ unless otherwise specified<br>  • Removed footnote from 'Max', Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.<br>• In section: Recommended operating conditions<br>  • Added opening text: "The following table describes the operating conditions ... "<br>  • Added note: "$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ are all ... "<br>  • In table: Recommended operating conditions (VDD_HV_x = 3.3 V) and (VDD_HV_x = 5 V)<br>  • Added footnote to 'Conditions' cloumn, (All voltages are referred to $V_{SS\_HV}$ unless otherwise specified).<br>  • Updated footnote for 'Min' column to Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.<br>  • Removed footnote for '$V_{DD\_HV\_A}$', '$V_{DD\_HV\_B}$', and '$V_{DD\_HV\_C}$' entry and updated the parameter column.<br>  • Removed entry : '$V_{SS\_HV}$'<br>  • Updated 'Parameter' column for '$V_{DD\_HV\_FLA}$', '$V_{DD\_HV\_ADC1\_REF}$', '$V_{DD\_LV}$'<br>  • Updated 'Min' column for '$V_{DD\_HV\_ADC0}$' '$V_{DD\_HV\_ADC1}$'<br>  • Updated 'Parameter' 'Min' 'Max' columns for '$V_{SS\_HV\_ADC0}$' and '$V_{SS\_HV\_ADC1}$'<br>  • Updated footnote for '$V_{DD\_LV}$ ' to $V_{DD\_LV}$ supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.<br>  • Removed row for symbol '$V_{SS\_LV}$'<br>  • Removed footnote from 'Max' column of '$V_{DD\_HV\_ADC0}$' and '$V_{DD\_HV\_ADC1}$', (PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1).<br>  • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)<br>  • Removed footnote from '$V_{IN1\_CMP\_REF}$', (Only applicable when supplying from external source).<br>  • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 5 V)<br>  • Added spec for '$V_{IN1\_CMP\_REF}$' and corresponding footnotes. |

*Table continues on the next page...*

## Table 51. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • In section: Voltage monitor electrical characteristics<br>  • Updated description for Low Voltage detector block.<br>  • Added note, BCP56, MCP68 and MJD31 are guaranteed ballasts.<br>  • In table: Voltage regulator electrical specifications<br>  • Added footnote, Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.<br>  • Revised table, Voltage monitor electrical characteristics |
| | | • In section: Supply current characteristics<br>  • In table: Current consumption characteristics<br>  • $I_{DD\_BODY\_4}$: Updated SYS_CLK to 120 MHz.<br>  • $I_{DD\_BODY\_4}$: Updated Max for $T_a$= 105 °C fand 85 °C )<br>  • $I_{dd\_STOP}$: Added condition for $T_a$= 105 °C and removed Max value for $T_a$= 85 °C.<br>  • $I_{DD\_HV\_ADC\_REF}$: Added condition for $T_a$= 105 °C and 85 °C and removed Max value for $T_a$= 25 °C.<br>  • $I_{DD\_HV\_FLASH}$: Added condition for $T_a$= 105 °C and 85 °C<br>  • In table: Low Power Unit (LPU) Current consumption characteristics<br>  • LPU_RUN and LPU_STOP: Added condition for $T_a$= 105 °C and 85 °C<br>  • In table: STANDBY Current consumption characteristics<br>  • Added condition for $T_a$= 105 °C and 85 °C for all entries.<br><br>• In section: I/O parameters<br>  • In table: Functional Pad AC Specifications @ 3.3 V Range<br>  • Updated values for 'pad_sr_hv (output)'<br>  • In table: DC electrical specifications @ 3.3V Range<br>  • Updateded Min and Max values for Vih and Vil respectively.<br>  • In table: Functional Pad AC Specifications @ 5 V Range<br>  • Updated values for 'pad_sr_hv (output)'<br>  • In table DC electrical specifications @ 5 V Range<br>  • Updated Min value for Vhys |

*Table continues on the next page...*

## Table 51. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • In section, Thermal attributes<br>  • Added table for 100 MAPBGA<br><br>• In section Obtaining package dimensions<br>  • Updated package details for 100 MAPBGA |
| | | • Editoral updates throughtout including correction of various module names. |

*Table continues on the next page...*