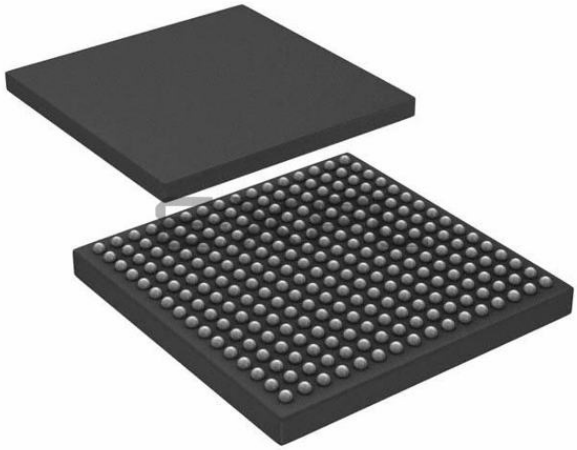

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, I²S, POR, WDT
Number of I/O	178
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 36x10b, 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746bk1mmj6

1 Block diagram

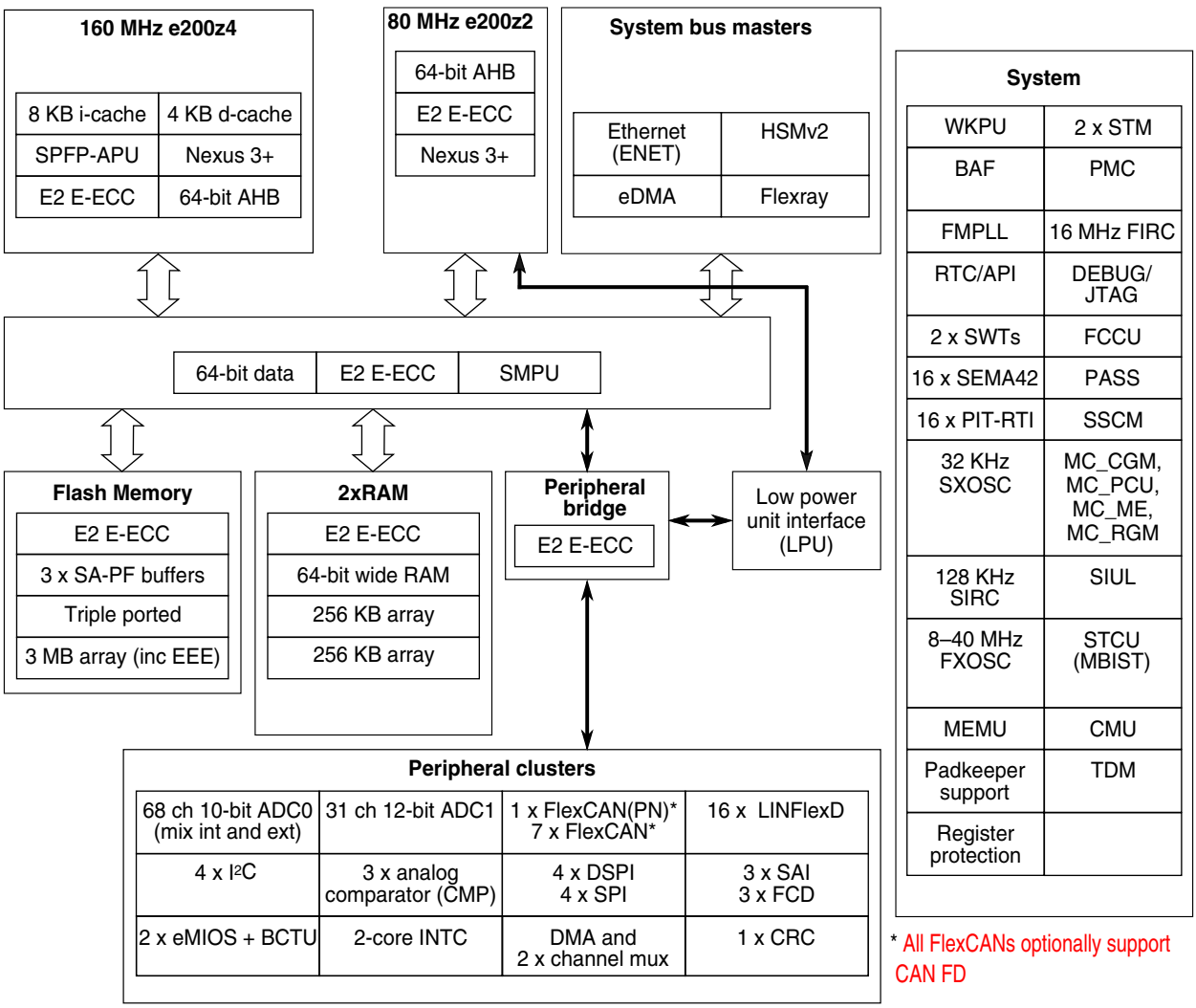
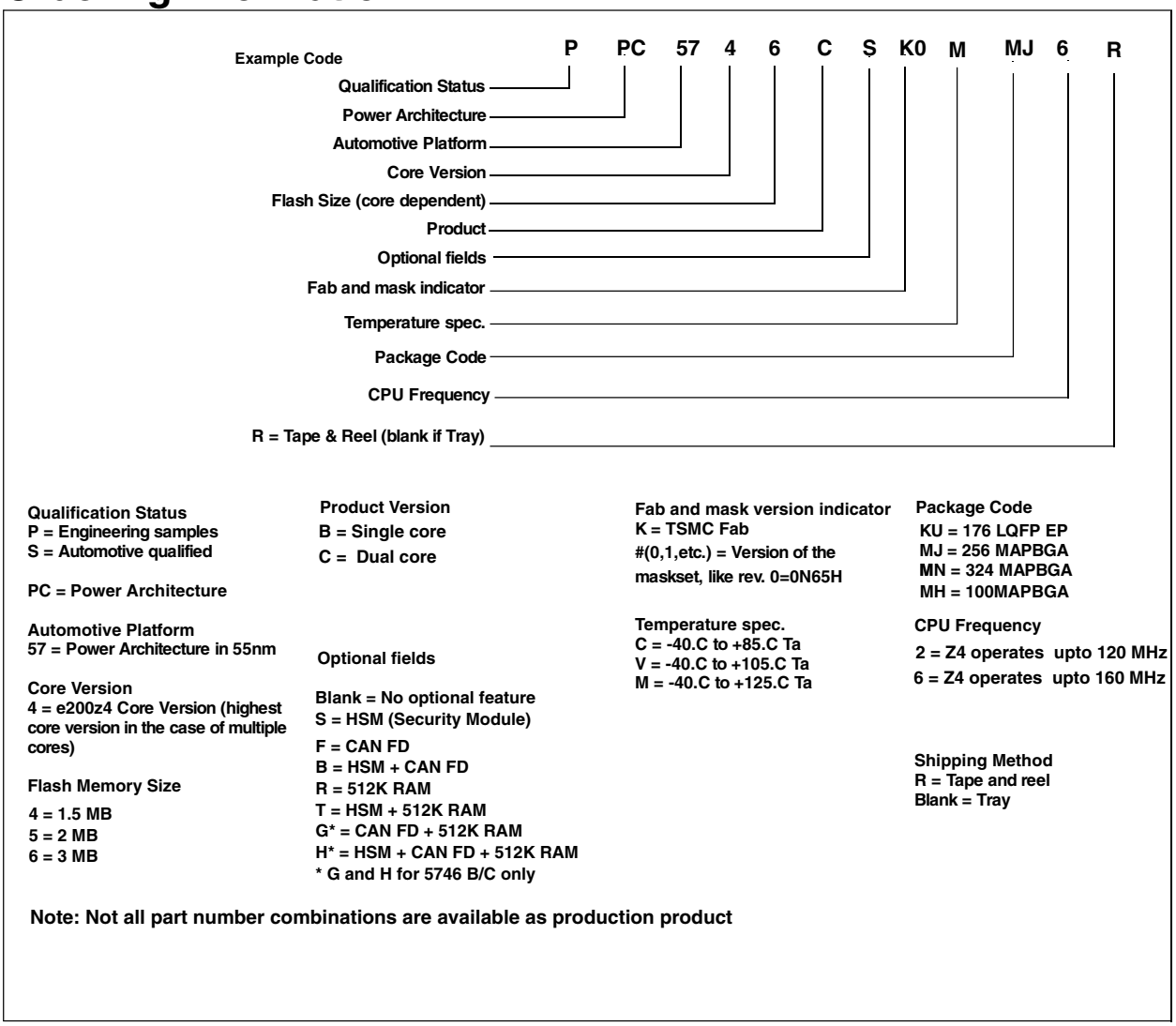


Figure 1. MPC5746C block diagram

2 Family comparison

The following table provides a summary of the different members of the MPC5746C family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

3.2 Ordering Information



Note: Not all part number combinations are available as production product

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in Table 5 for specific conditions

Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V) (continued)

Symbol	Parameter	Conditions[1]	Min[2]	Max	Unit
T_A[8]	Ambient temperature under bias	f_{CPU} ≤ 160 MHz	–40	125	°C
T_J	Junction temperature under bias	—	–40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. Only applicable when supplying from external source.
5. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
6. VIN1_CMP_REF ≤ VDD_HV_A
7. This supply is shorted VDD_HV_A on lower packages.
8. T_J=150°C. Assumes T_A=125°C
   - Assumes maximum θJA of 2s2p board. See Thermal attributes

NOTE

If VDD_HV_A is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. VDD_HV_FLA should not be supplied externally and should only have decoupling capacitor.

Table 7. Recommended operating conditions ($V_{DD\_HV\_x}$ = 5 V)

Symbol	Parameter	Conditions [1]	Min[2]	Max	Unit
$V_{DD\_HV\_A}$ $V_{DD\_HV\_B}$ $V_{DD\_HV\_C}$	HV IO supply voltage	—	4.5	5.5	V
$V_{DD\_HV\_FLA}$[3]	HV flash supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_ADC1\_REF}$	HV ADC1 high reference voltage	—	3.15	5.5	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	HV ADC supply voltage	—	max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05	5.5	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV}[4]	Core supply voltage	—	1.2	1.32	V
$V_{IN1\_CMP\_REF}$[5, 6]	Analog Comparator DAC reference voltage	—	3.15	5.5[5]	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_A[7]	Ambient temperature under bias	f_{CPU} ≤ 160 MHz	–40	125	°C
T_J	Junction temperature under bias	—	–40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. When VDD_HV is in 5 V range, VDD_HV_FLA cannot be supplied externally.This pin is decoupled with C_{flash_reg}.

4. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. VIN1_CMP_REF ≤ VDD_HV_A
6. This supply is shorted VDD_HV_A on lower packages.
7. T_J=150°C. Assumes T_A=125°C
    - Assumes maximum θJA of 2s2p board. See Thermal attributes

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
    - Control of external NPN ballast transistor
    - Generating core supply using internal ballast transistor
    - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector (LVD_FLASH) for 3.3 V flash supply (VDD_HV_FLA)
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

1. BCP56, MCP68 and MJD31are guaranteed ballasts.

4.4 Voltage monitor electrical characteristics

Table 9. Voltage monitor electrical characteristics

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt[2, 2]	Reset Type	Min	Typ	Max	V
V_{POR_LV}	LV supply power on reset detector	Fall	Untrimmed	Yes	No	Destructive	0.930	0.979	1.028	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				0.980	1.029	1.078	V
			Trimmed				-	-	-	V
$V_{HVD\_LV\_cold}$	LV supply high voltage monitoring, detecting at device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.325	1.345	1.375	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.345	1.365	1.395	V
$V_{LVD\_LV\_PD2\_hot}$	LV supply low voltage monitoring, detecting on the PD2 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1250	1.1425	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1450	1.1625	1.1800	V
$V_{LVD\_LV\_PD1\_hot\ (BGFP)}$	LV supply low voltage monitoring, detecting on the PD1 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.140	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
$V_{LVD\_LV\_PD0\_hot\ (BGFP)}$	LV supply low voltage monitoring, detecting on the PD0 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
V_{POR_HV}	HV supply power on reset detector	Fall	Untrimmed	Yes	No	Destructive	2.7000	2.8500	3.0000	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				2.7500	2.9000	3.0500	V
			Trimmed				-	-	-	V
$V_{LVD\_IO\_A\_LO}$[3, 3]	HV IO_A supply low voltage monitoring - low range	Fall	Untrimmed	Yes	No	Destructive	2.7500	2.9230	3.0950	V
			Trimmed				2.9780	3.0390	3.1000	V
		Rise	Untrimmed				2.7800	2.9530	3.1250	V
			Trimmed				3.0080	3.0690	3.1300	V
$V_{LVD\_IO\_A\_HI}$[3]	HV IO_A supply low voltage monitoring - high range	Fall	Trimmed	No	Yes	Destructive	Disabled at Start			
							4.0600	4.151	4.2400	V
		Rise	Trimmed				Disabled at Start			
							4.1150	4.2010	4.3000	V

Table continues on the next page...

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_BODY\_2}$ 6	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125°C[5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	—	246	mA
		T_a = 105°C	—	—	235	mA
		T_a = 85°C	—	—	210	mA
$I_{DD\_BODY\_3}$ 7	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125 °C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	181	mA
		T_a = 105 °C	—	—	176	mA
		T_a = 85°C	—	—	171	mA
$I_{DD\_BODY\_4}$[8]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125 °C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	264	mA
		T_a = 105 °C	—	—	176	mA
		T_a = 85 °C	—	—	171	mA
I_{DD_STOP}	STOP mode Operating current	T_a = 125 °C[9] V_{DD_LV} = 1.25 V	—	—	49	mA
		T_a = 105 °C V_{DD_LV} = 1.25 V	—	10.6	—	
		T_a = 85 °C V_{DD_LV} = 1.25 V	—	8.1	—	
		T_a = 25 °C V_{DD_LV} = 1.25 V	—	4.6	—	

Table continues on the next page...

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 14. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry[2]	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01[3]
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00[3]
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input)[4]		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.
3. Slew rate control modes
4. Input slope = 2ns

NOTE

The specification given above is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The specification given above is measured between 20% / 80%.

Table 18. Functional reset pad electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{HYS}	CMOS Input Buffer hysterisis	—	300	—	—	mV
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current [1, 1]	Device under power-on reset $V_{DD\_HV\_A}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD\_HV\_A}$	0.2	—	—	mA
		Device under power-on reset $V_{DD\_HV\_A}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD\_HV\_IO}$	11	—	—	mA
W_{FRST}	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	$\overline{\text{RESET}}$ input not filtered pulse	—	2000	—	—	ns
$\|I_{WPU}\|$	Weak pull-up current absolute value	RESET pin V_{IN} = V_{DD}	23	—	82	µA

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{\text{PORST}}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{\text{PORST}}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	0.65 x $V_{DD\_HV\_A}$	—	—	V
V_{IL}	Input low level	—	—	0.35 x $V_{DD\_HV\_A}$	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

6.1.1.1 Input equivalent circuit and ADC conversion characteristics

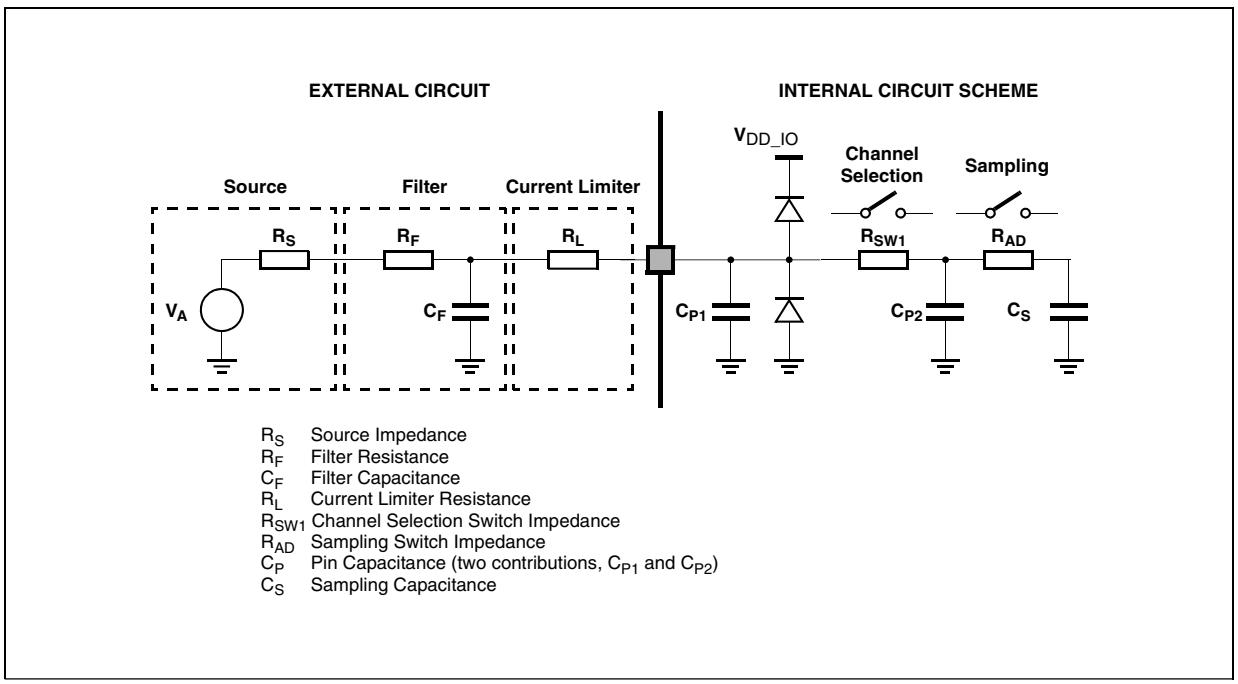


Figure 6. Input equivalent circuit

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

Table 20. ADC conversion characteristics (for 12-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	250	—	—	ns
t_{conv}	Conversion time[4]	80 MHz	700	—	—	ns
t_{total_conv}	Total Conversion time t_{sample} + t_{conv} (for standard and extended channels)	80 MHz	1.5[5]	—	—	µs
	Total Conversion time t_{sample} + t_{conv} (for precision channels)		1	—	—	
C_S[6, 6]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[6]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[6]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω

Table continues on the next page...

Table 20. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
R_{AD}[6]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity (precise channel)	—	–2	—	2	LSB
INL	Integral non-linearity (standard channel)	—	–3	—	3	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (precision channel)	150 °C	—	—	250	nA
	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C $_{TA}$	—	5	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{precision\ channels}$	Total unadjusted error for precision channels	Without current injection	–6	+/-4	6	LSB
		With current injection[7, 7]		+/-5		LSB
$TUE_{standard/extended\ channels}$	Total unadjusted error for standard/ extended channels	Without current injection	–8	+/-6	8	LSB
		With current injection[7]		+/-8		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	µs

1. Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 6.
7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

Table 23. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
	Oscillator Analog Circuit supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		
		LCP	8 MHz		141		uA
			16 MHz		252		
			40 MHz		518		
V_{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3	1.95			V
V_{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3			1.25	V

1. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board.
2. Typ value for oscillator supply 3.3 V@27 °C

6.2.2 32 kHz Oscillator electrical specifications

Table 24. 32 kHz oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{osc_lo}	Oscillator crystal or resonator frequency		32		40	KHz
t_{cst}	Crystal Start-up Time[1, 2]				2	s

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 16 MHz RC Oscillator electrical specifications

Table 25. 16 MHz RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F_{Target}	IRC target frequency	—	—	16	—	MHz
PTA	IRC frequency variation after trimming	—	-5	—	5	%
$T_{startup}$	Startup time	—		—	1.5	us
T_{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T_{LTJIT}	Long term jitter		—	—	0.2	%

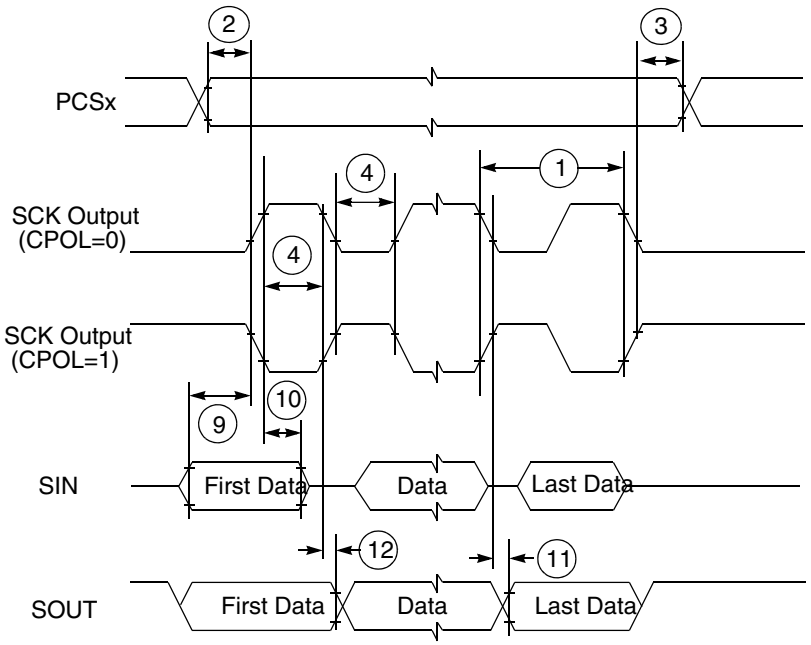


Figure 8. DSPI classic SPI timing — master, CPHA = 0

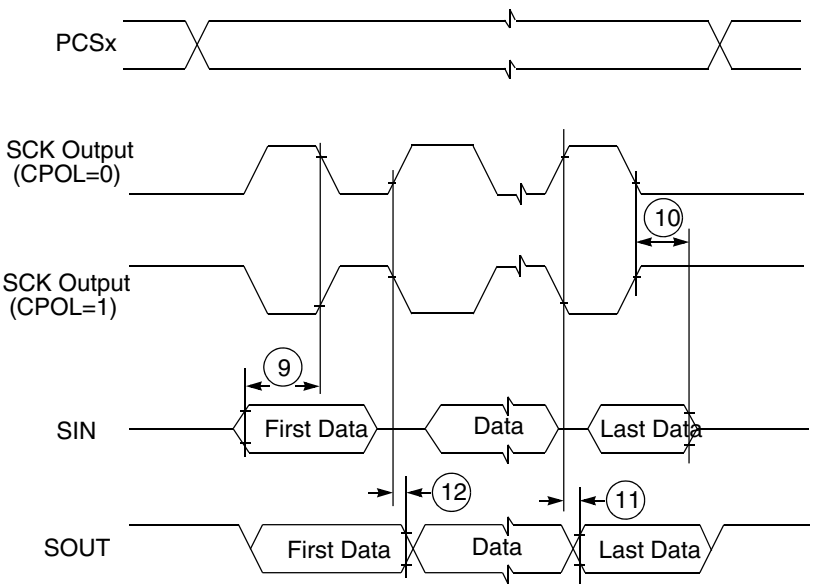


Figure 9. DSPI classic SPI timing — master, CPHA = 1

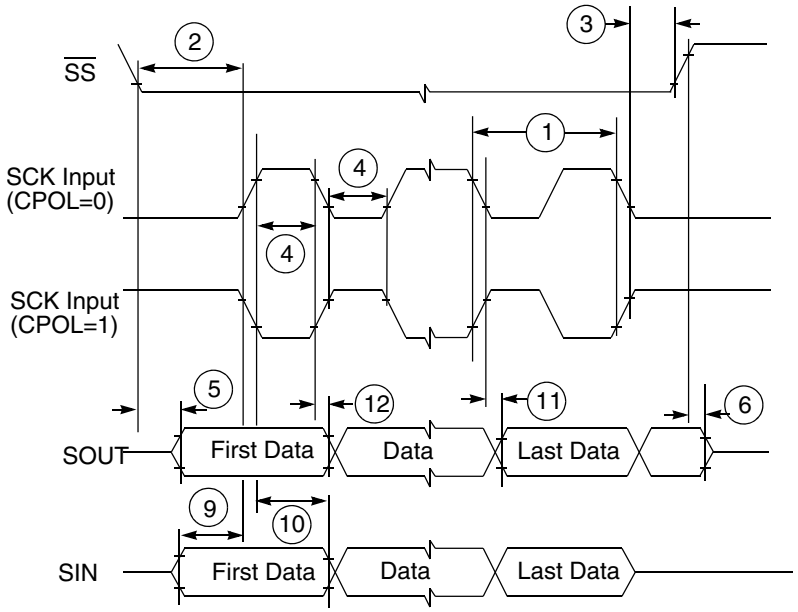


Figure 10. DSPI classic SPI timing — slave, CPHA = 0

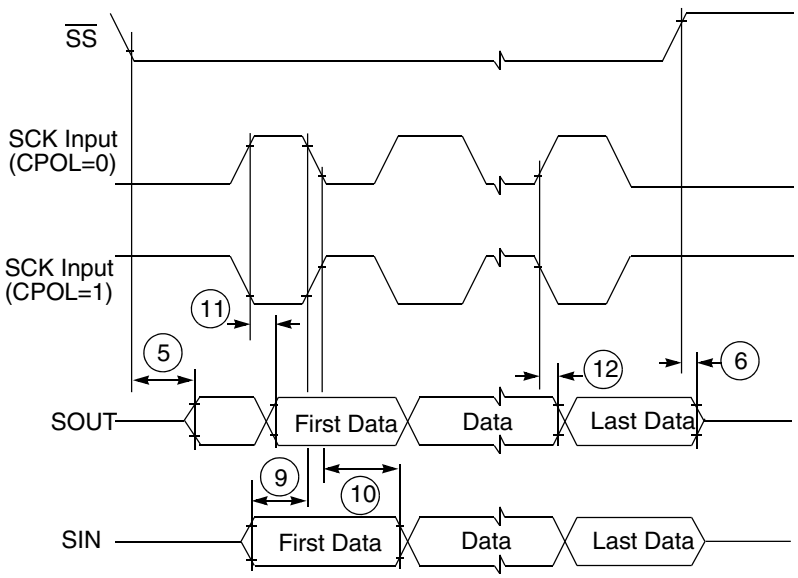


Figure 11. DSPI classic SPI timing — slave, CPHA = 1

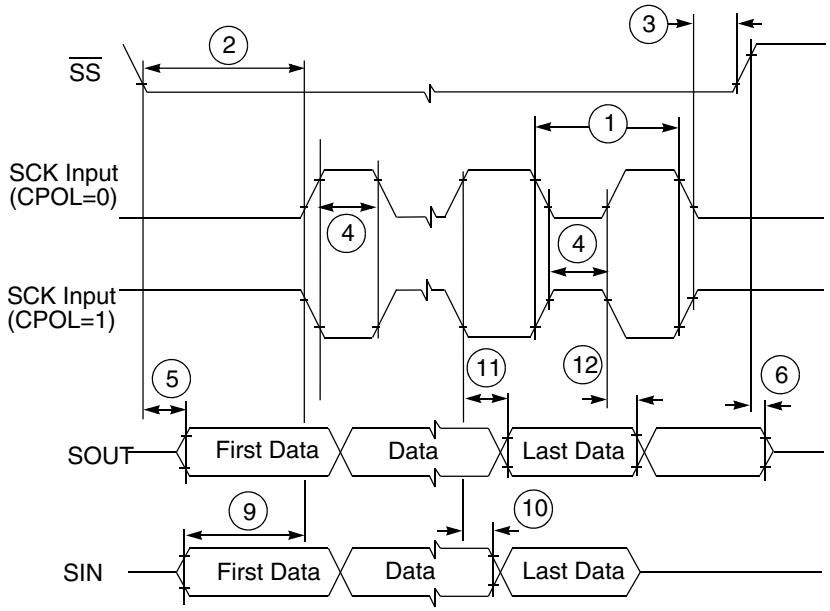


Figure 14. DSPI modified transfer format timing – slave, CPHA = 0

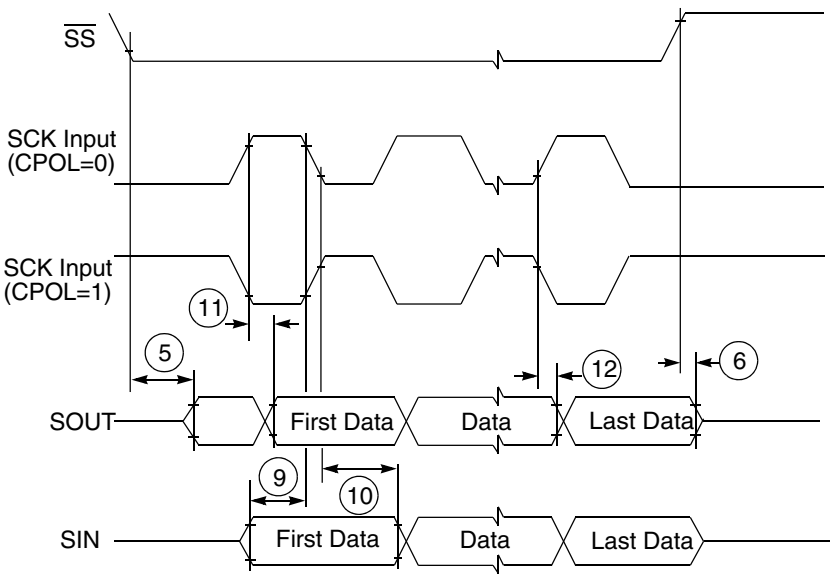


Figure 15. DSPI modified transfer format timing — slave, CPHA = 1

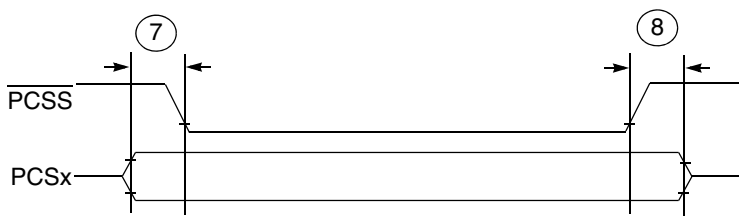


Figure 16. DSPI PCS strobe (PCSS) timing

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = –40 oC / 150 oC.

6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 41. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

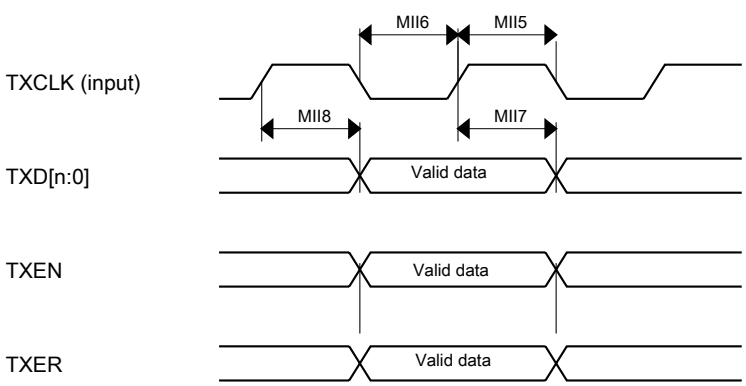


Figure 21. RMII/MII transmit signal timing diagram

Table 45. JTAG pin AC electrical characteristics [1] (continued)

#	Symbol	Characteristic	Min	Max	Unit
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

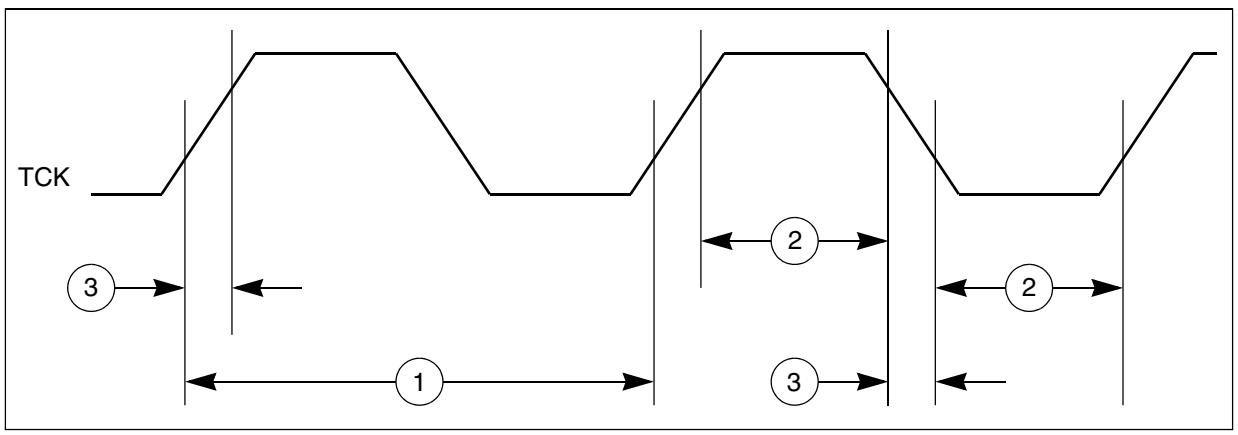


Figure 25. JTAG test clock input timing

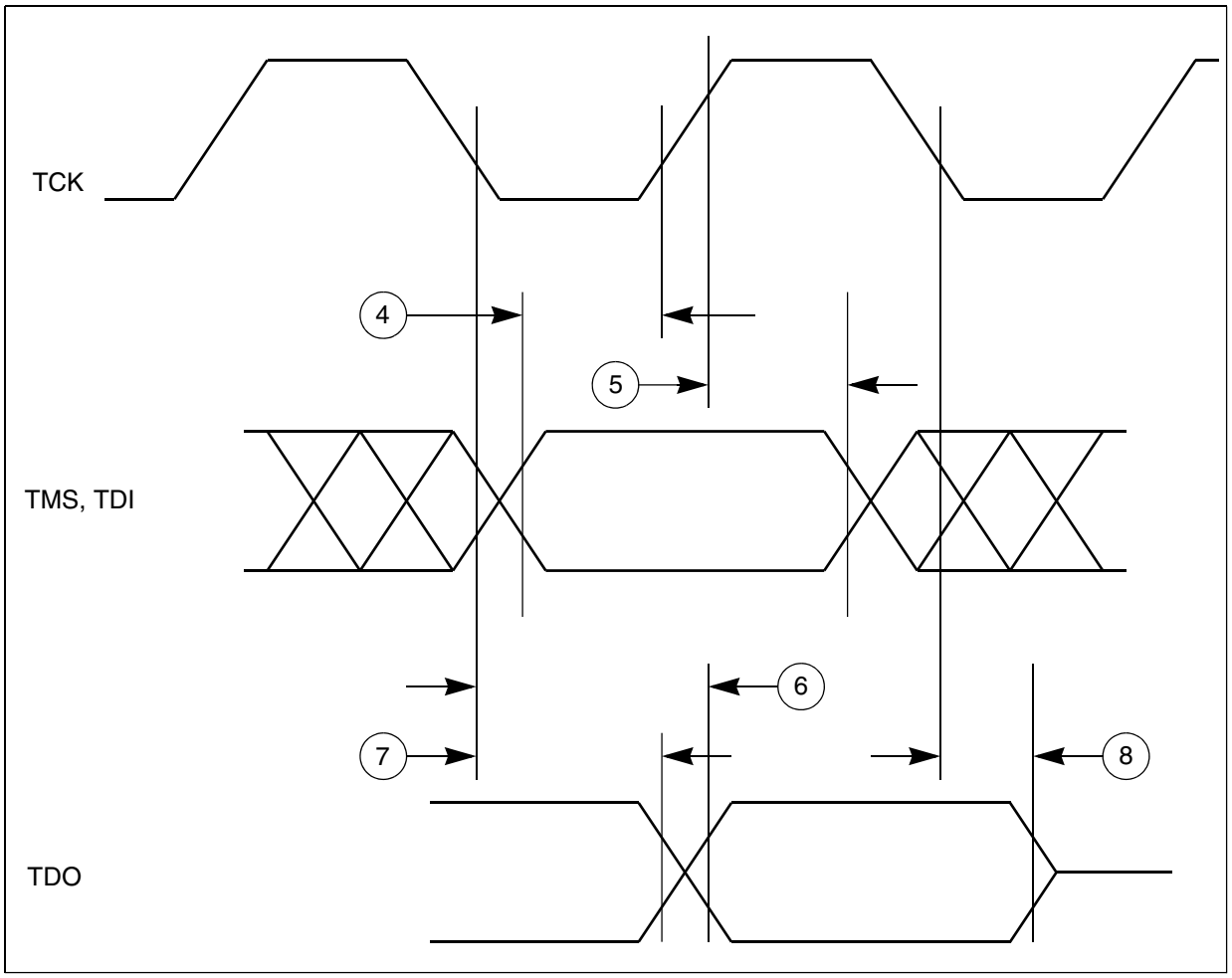


Figure 26. JTAG test access port timing

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In section, Thermal attributes
		  • Added table for 100 MAPBGA
		
		• In section Obtaining package dimensions
		  • Updated package details for 100 MAPBGA

		• Editoral updates throughtout including correction of various module names.

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

Rev 4	9 March 2016	• In section, Voltage regulator electrical characteristics
		  • In table, Voltage regulator electrical specifications:
		  • Updated the footnote on $V_{DD\_HV\_BALLAST}$

Rev 5	27 February 2017	• In Family Comparison section:
		  • Updated the "MPC5746C Family Comparison" table.
		  • added "NVM Memory Map 1", "NVM Memory Map 2", and "RAM Memory Map" tables.
		
		• Updated the product version, flash memory size and optional fields information in Ordering Information section.
		
		• In Recommended Operating Conditions section, removed the note related to additional crossover current.
		
		• VDD_HV_C row added in "Voltage regulator electrical specifications" table in Voltage regulator electrical characteristics section.
		
		• In Voltage Monitor Electrical Characteristics section, updated the "Trimmed" Fall and Rise specs of VHVD_LV_cold parameter in "Voltage Monitor Electrical Characteristics" table.
		
		• In AC Electrical Specifications: 3.3 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” in the table.
		• In DC Electrical Specifications: 3.3 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” and updated "Vol min and max" values in the table.
		• In AC Electrical Specifications: 5 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” in the table.
		• In DC Electrical Specifications: 5 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” and updated "Vol min and max" values in the table.
		
		• In "Flash memory AC timing specifications" table in Flash memory AC timing specifications section:
		  • Updated the "t_{psus}" typ value from 7 us to 9.4 us.
		  • Updated the "t_{psus}" max value from 9.1 us to 11.5 us.
		
		• Added "Continuous SCK Timing" table in DSPI timing section.
		
		• Added "ADC pad leakage" at 105°C TA conditions in "ADC conversion characteristics (for 12-bit)" table in ADC electrical specifications section.
		
		• In "STANDBY Current consumption characteristics" table in Supply current characteristics section:
		  • Updated the Typ and max values of IDD Standby current.
		  • Added IDD Standby3 current spec for FIRC ON.
		
		• Removed IVDDHV and IVDDLV specs in 16 MHz RC Oscillator electrical specifications section.
		
		• Added Reset Sequence section, with Reset Sequence Duration, BAF execution duration section, and Reset Sequence Distribution as its sub-sections.

Table continues on the next page...