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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, FlexRay, I ² C, LINbus, SPI
Peripherals	DMA, I ² S, POR, WDT
Number of I/O	129
Program Memory Size	3MB (3M × 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 36x10b, 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746bsk1amku2

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40030000	0x4003FFFF	64 KB	SRAM4	not available	available	available
0x40040000	0x4004FFFF	64 KB	SRAM5	not available	not available	available
0x40050000	0x4005FFFF	64 KB	SRAM6	not available	not available	available
0x40060000	0x4006FFFF	64 KB	SRAM7	not available	not available	optional
0x40070000	0x4007FFFF	64 KB	SRAM8	not available	not available	optional

 Table 4.
 MPC5746C Family Comparison - RAM Memory Map (continued)

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5746C.

Table 6. Recommended operating conditions ($V_{DD HV x} = 3.3 V$) (continued)

Symbol	Parameter	Conditions ¹	Min ²	Мах	Unit
T _A ⁸	Ambient temperature under bias	f _{CPU} ≤ 160 MHz	-40	125	°C
TJ	Junction temperature under bias		-40	150	°C

1. All voltages are referred to $V_{SS\ HV}$ unless otherwise specified

- 2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
- 3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
- 4. Only applicable when supplying from external source.
- 5. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
- 6. VIN1_CMP_REF \leq VDD_HV_A
- 7. This supply is shorted VDD_HV_A on lower packages.
- 8. T_J =150°C. Assumes T_A =125°C
 - Assumes maximum θ JA of 2s2p board. See Thermal attributes

NOTE

If VDD_HV_A is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. VDD_HV_FLA should not be supplied externally and should only have decoupling capacitor.

Table 7. Recommended operating conditions ($V_{DD_HV_x} = 5 V$)

Symbol	Parameter	Conditions ¹	Min ²	Мах	Unit
V _{DD_HV_A}	HV IO supply voltage		4.5	5.5	V
V _{DD_HV_B}					
V _{DD_HV_C}					
V _{DD_HV_FLA} ³	HV flash supply voltage		3.15	3.6	V
V _{DD_HV_ADC1_REF}	HV ADC1 high reference voltage		3.15	5.5	V
V _{DD_HV_ADC0}	HV ADC supply voltage	—	max(VDD_H V_A,VDD_H	5.5	V
VDD_HV_ADC1			V_B,VDD_H V_C) - 0.05		
V _{SS_HV_ADC0}	HV ADC supply ground		-0.1	0.1	V
V _{SS_HV_ADC1}					
V _{DD_LV} ⁴	Core supply voltage		1.2	1.32	V
V _{IN1_CMP_REF} ^{5, 6}	Analog Comparator DAC reference voltage		3.15	5.5 ⁵	V
I _{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T _A ⁷	Ambient temperature under bias	f _{CPU} ≤ 160 MHz	-40	125	°C
TJ	Junction temperature under bias		-40	150	°C

1. All voltages are referred to $V_{\text{SS}\ \text{HV}}$ unless otherwise specified

2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.

3. When VDD_HV is in 5 V range, VDD_HV_FLA cannot be supplied externally. This pin is decoupled with $C_{flash_{reg}}$.

- 5. 1. For VDD_HV_x, 1µf on each side of the chip
 - a. 0.1 μ f close to each VDD/VSS pin pair.
 - b. 10 μf near for each power supply source
 - c. For VDD_LV, 0.1uf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter.
 - For VDD_LV, 0.1uf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this
 amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as
 specified by CFP_REG parameter
- 6. Only applicable to ADC1
- 7. In external ballast configuration the following must be ensured during power-up and power-down (Note: If V_{DD_HV_BALLAST} is supplied from the same source as VDD_HV_A this condition is implicitly met):
 - During power-up, V_{DD_HV_BALLAST} must have met the min spec of 2.25V before VDD_HV_A reaches the POR_HV_RISE min of 2.75V.
 - During power-down, $V_{DD_HV_BALLAST}$ must not drop below the min spec of 2.25V until VDD_HV_A is below POR_HV_FALL min of 2.7V.

NOTE

For a typical configuration using an external ballast transistor with separate supply for VDD_HV_A and the ballast collector, a bulk storage capacitor (as defined in Table 8) is required on VDD_HV_A close to the device pins to ensure a stable supply voltage.

Extra care must be taken if the VDD_HV_A supply is also being used to power the external ballast transistor or the device is running in internal regulation mode. In these modes, the inrush current on device Power Up or on exit from Low Power Modes is significant and may case the VDD_HV_A voltage to drop resulting in an LVD reset event. To avoid this, the board layout should be optimized to reduce common trace resistance or additional capacitance at the ballast transistor collector (or VDD_HV_A pins in the case of internal regulation mode) is required. NXP recommends that customers simulate the external voltage supply circuitry.

In all circumstances, the voltage on VDD_HV_A must be maintained within the specified operating range (see Recommended operating conditions) to prevent LVD events.

Symbol	Parameter	State	Conditions	Configuration				Threshol	d	Unit
				Power Up	Mask Opt ^{2, 2}	Reset Type	Min	Тур	Max	v
V _{LVD_LV_PD}	LV supply low	Fall	Untrimmed	No	Yes	Function	Disabled	Disabled at Start		
2_cold	voltage		Trimmed			al	1.1400	1.1550	1.1750	V
	detecting at the	Rise	Untrimmed				Disabled	at Start		
	device pin		Trimmed				1.1600	1.1750	1.1950	V

 Table 9. Voltage monitor electrical characteristics (continued)

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.

2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.

3. There is no voltage monitoring on the V_{DD_HV_ADC0}, V_{DD_HV_ADC1}, V_{DD_HV_B} and V_{DD_HV_C} I/O segments. For applications requiring monitoring of these segments, either connect these to V_{DD_HV_A} at the PCB level or monitor externally.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Symbol	Parameter	Conditions ¹	Min	Тур	Max	Unit
I _{DD_BODY_1}	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply +	_	_	147	mA
_, 0		2 x HV ADC supplies ^{4, 4}				
		T _a = 125°C ^{5, 5}				
		V _{DD_LV} = 1.25 V				
		VDD_HV_A = 5.5V				
		SYS_CLK = 80MHz				
		T _a = 105°C	—	—	142	mA
		T _a = 85 °C	_	—	137	mA

 Table 10.
 Current consumption characteristics

Table continues on the next page...

Symbol	Parameter	Conditions ¹	Min	Тур	Max	Unit
STANDBY2	STANDBY with	T _a = 25 °C	_	75	_	μA
	128K RAM	T _a = 85 °C	—	155	730	
		T _a = 105 °C	—	255	1350	
		$T_a = 125 \ ^{\circ}C^{2}$	—	396	2600	
STANDBY3	STANDBY with	$T_a = 25 \text{ °C}$	—	80	_	μA
	256K RAM	T _a = 85 °C	—	180	800	
		T _a = 105 °C	—	290	1425	
		$T_{a} = 125 \ ^{\circ}C^{2}$	—	465	2900	
STANDBY3	FIRC ON	T _a = 25 °C	—	500	—	μA

Table 12. STANDBY Current consumption characteristics (continued)

1. The content of the Conditions column identifies the components that draw the specific current.

 Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts \times (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Symbol	Parameter	Conditions ¹	Class	Max value ²	Unit
V _{ESD(HBM)}	Electrostatic discharge	T _A = 25 °C	H1C	2000	V
	(Human Body Model)	conforming to AEC- Q100-002			
V _{ESD(CDM)}	Electrostatic discharge	T _A = 25 °C	C3A	500	V
	(Charged Device Model)	conforming to AEC- Q100-011		750 (corners)	

Table 13. ESD ratings

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2. Data based on characterization results, not tested in production.

5.2 DC electrical specifications @ 3.3V Range

Table 15. DC electrical specifications @ 3.3V Range

Symbol	Parameter	Va	lue	Unit
		Min	Max	
Vih (pad_i_hv)	Pad_I_HV Input Buffer High Voltage	0.72*VDD_HV_ x	VDD_HV_x + 0.3	V
Vil (pad_i_hv)	Pad_I_HV Input Buffer Low Voltage	VDD_HV_x - 0.3	0.45*VDD_HV_ x	V
Vhys (pad_i_hv)	Pad_I_HV Input Buffer Hysteresis	0.11*VDD_HV_ x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.67*VDD_HV_ x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VDD_HV_x - 0.3	0.35*VDD_HV_ x	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.57 * VDD_HV_x ^{1, 1}	VDD_HV_x ¹ + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VDD_HV_x - 0.3	0.4 * VDD_HV_x ¹	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x ¹		V
Pull_IIH (pad_i_hv)	Weak Pullup Current ^{2, 2} Low	15		μA
Pull_IIH (pad_i_hv)	Weak Pullup Current ^{3, 3} High		55	μΑ
Pull_IIL (pad_i_hv)	Weak Pulldown Current ³ Low	28		μΑ
Pull_IIL (pad_i_hv)	Weak Pulldown Current ² High		85	μΑ
Pull_loh	Weak Pullup Current ⁴	15	50	μA
Pull_lol	Weak Pulldown Current ⁵	15	50	μA
linact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	μΑ
Voh	Output High Voltage ⁶	0.8 *VDD_HV_x ¹	_	V
Vol	Output Low Voltage ⁷	_	0.2 *VDD_HV_x ¹	V
			0.1 *VDD_HV_x	
loh_f	Full drive loh ^{9, 9} (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
lol_f	Full drive lol ⁹ (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
loh_h	Half drive loh ⁹ (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
lol_h	Half drive Iol ⁹ (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

- 1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
- 2. Measured when pad=0.69*VDD_HV_x
- 3. Measured when pad=0.49*VDD_HV_x
- 4. Measured when pad = 0 V
- 5. Measured when pad = VDD_HV_x
- 6. Measured when pad is sourcing 2 mA
- 7. Measured when pad is sinking 2 mA
- 8. Measured when pad is sinking 1.5 mA $\,$
- 9. Ioh/IoI is derived from spice simulations. These values are NOT guaranteed by test.

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

6.2.4 128 KHz Internal RC oscillator Electrical specifications Table 26. 128 KHz Internal RC oscillator electrical specifications

Symbol	Parameter	Condition	Min	Тур	Max	Unit
F _{oscu} ¹	Oscillator frequency	Calibrated	119	128	136.5	KHz
	Temperature dependence				600	ppm/C
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	μΑ
		Clock stopped			200	nA

1. Vdd=1.2 V, 1.32V, T_a=-40 C, 125 C

6.2.5 PLL electrical specifications

Table 27. PLL electrical specifications

Parameter	Min	Тур	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 28	ps	NON SSCG mode
TIE			See Table 28		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	μs	Calibration mode

Table 28. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J _{SN} ¹	Jitter due to Fractional Mode (ps) J _{SDM} ²	Jitter due to Fractional Mode J _{SSCG} (ps) ³	1 Sigma Random Jitter J _{RJ} (ps) ⁴	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	+/-(J_{SN} + J_{SDM} + J_{SSCG} + $N^{[4]}$ × J_{RJ})

Table continues on the next page...

Type of jitter	Jitter due to Supply Noise (ps) J _{SN} ¹	Jitter due to Fractional Mode (ps) J _{SDM} ²	Jitter due to Fractional Mode J _{SSCG} (ps) ³	1 Sigma Random Jitter J _{RJ} (ps) ⁴	Total Period Jitter (ps)
Long Term Jitter (Integer Mode)				40	+/-(N x J _{RJ})
Long Term jitter (Fractional Mode)				100	+/-(N x J _{RJ})

Table 28. Jitter calculation (continued)

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on VDD_LV and VSS_LV.

2. This jitter component is added when the PLL is working in the fractional mode.

3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.

4. The value of N is dependent on the accuracy requirement of the application. See Table 29

Table 29. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27
4	6.30 × 1e-03
5	5.63 × 1e-05
6	2.00 × 1e-07
7	2.82 × 1e-10

6.3 Memory interfaces

6.3.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.

Memory interfaces

Symbol	Characteristic	Min	Typical	Max ^{1, 1}	Units 2, 2
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	_	_	8192 x Tperiod x Nread	_
t _{mr16kseq}	Margin Read time for sequential sequence on 16 KB block.	73.81	_	110.7	μs
t _{mr32kseq}	Margin Read time for sequential sequence on 32 KB block.	128.43	_	192.6	μs
t _{mr64kseq}	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	μs
t _{mr256kseq}	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	μs

Table 31. Flash memory Array Integrity and Margin Read specifications (continued)

- Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The
 equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and
 Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires
 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the
 address pipeline set to 2, Nread would equal 4 (or 6 2).)
- 2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

6.3.3 Flash memory module life specifications Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks. ^{1, 1}	—	250,000	_	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks. ^{2, 2}	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10		Years

1. Program and erase supported across standard temperature specs.

2. Program and erase supported across standard temperature specs.

6.3.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



Figure 8. DSPI classic SPI timing — master, CPHA = 0



Figure 9. DSPI classic SPI timing — master, CPHA = 1

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

6.4.2.2 TxEN



Figure 17. TxEN signal

Name	Description	Min	Max	Unit
dCCTxEN _{RISE25}	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN _{FALL25}	Fall time of TxEN signal at CC	_	9	ns
dCCTxEN ₀₁	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	_	25	ns
dCCTxEN ₁₀	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	_	25	ns

1. All parameters specified for $V_{DD_HV_IOx}$ = 3.3 V -5%, +±10%, TJ = -40 °C / 150 °C, TxEN pin load maximum 25 pF





6.4.2.3 TxD



Figure 19. TxD Signal

Table 39.	TxD outpu	it characteristics
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Name	Description ¹	Min	Max	Unit
dCCT _{xAsym}	Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns)	-2.45	2.45	ns
dCCTxD _{RISE25} +dCCTx D _{FALL25}	Sum of Rise and Fall time of TxD signal at the output		9 ²	ns

Table continues on the next page...

Name	Description ¹	Min	Max	Unit
dCCTxD ₀₁	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxD ₁₀	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	_	25	ns

Table 39. TxD output characteristics (continued)

1. All parameters specified for $V_{DD_HV_IOx}$ = 3.3 V -5%, +±10%, TJ = -40 °C / 150 °C, TxD pin load maximum 25 pF.

2. For $3.3 \text{ V} \pm 10\%$ operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 20. TxD Signal propagation delays

6.4.2.4 RxD

Table 40.	RxD	input	characteristic
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Name	Description ¹	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
dCCRxD ₀₁	Sum of delay from actual input to the D input of the first FF, rising edge	_	10	ns
dCCRxD ₁₀	Sum of delay from actual input to the D input of the first FF, falling edge	_	10	ns





Figure 27. JTAG boundary scan timing

6.5.2 Nexus timing

Table 46. Nexus debug port timing 1

No.	Symbol	Parameter	Condition	Min	Max	Unit
			S			
1	t _{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t _{MDC}	MCKO Duty Cycle	—	40	60	%
3	t _{MDOV}	MCKO Low to MDO, MSEO, EVTO Data Valid ²	—	-0.1	0.25	tMCYC
4	t _{EVTIPW}	EVTI Pulse Width	—	4	—	tTCYC
5	t _{EVTOPW}	EVTO Pulse Width	—	1	—	tMCYC
6	t _{TCYC}	TCK Cycle Time ³	—	62.5	—	ns
7	t _{TDC}	TCK Duty Cycle	—	40	60	%
8	t _{NTDIS} , t _{NTMSS}	TDI, TMS Data Setup Time	_	8	_	ns

Table continues on the next page...

Table 46. Nexus debug port timing ¹ (continued)

No.	Symbol	Parameter	Condition s	Min	Max	Unit
9	t _{NTDIH} , t _{NTMSH}	TDI, TMS Data Hold Time	_	5	_	ns
10	t _{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.

- 2. For all Nexus modes except DDR mode, MDO, MSEO, and EVTO data is held valid until next MCKO low cycle.
- 3. The system clock frequency needs to be four times faster than the TCK frequency.



Figure 28. Nexus output timing



Figure 29. Nexus EVTI Input Pulse Width

6.5.4 External interrupt timing (IRQ pin) Table 48. External interrupt timing specifications

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t _{IPWL}	IRQ pulse width low	—	3	—	t _{CYC}
2	t _{IPWH}	IRQ pulse width high	_	3	_	t _{CYC}
3	t _{ICYC}	IRQ edge to edge time	_	6		t _{CYC}

These values applies when IRQ pins are configured for rising edge or falling edge events, but not both.



Figure 31. External interrupt timing

7 Thermal attributes

7.1 Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Single-layer (1s)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	50.7	°C/W	11, 22
Four-layer (2s2p)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	24.2	°C/W	1, 2, 33
Single-layer (1s)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	38.1	°C/W	1, 3

Table continues on the next page ...

Thermal attributes

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
—	R _{θJB}	Thermal resistance, junction to board	16.8	°C/W	44
	R _{0JC}	Thermal resistance, junction to case	7.4	°C/W	55
_	Ψ _{JT}	Thermal characterization parameter, junction to package top natural convection	0.2	°C/W	66
_	Ψ _{JB}	Thermal characterization parameter, junction to package bottom natural convection	7.3	°C/W	77

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
- 3. Per JEDEC JESD51-6 with the board horizontal
- 4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
- 7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
Single-layer (1s)	R _{eJA}	Thermal resistance, junction to ambient (natural convection)	42.6	°C/W	11, 22
Four-layer (2s2p)	R _{0JA}	Thermal resistance, junction to ambient (natural convection)	26.0	°C/W	1,2,33
Single-layer (1s)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	31.0	°C/W	1,3
Four-layer (2s2p)	R _{eJMA}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	21.3	°C/W	1,3
_	R _{θJB}	Thermal resistance, junction to board	12.8	°C/W	44

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Reset sequence















Figure 35. Functional reset sequence long

Rev. No.	Date	Substantial Changes
		 In section, Thermal attributes Added table for 100 MAPBGA
		 In section Obtaining package dimensions Updated package details for 100 MAPBGA
		Editoral updates throughtout including correction of various module names.

Table 51. Revision History (continued)

Table continues on the next page...

Table 51. Revision History (continue

Rev. No.	Date	Substantial Changes
Rev 4	9 March 2016	 In section, Voltage regulator electrical characteristics In table, Voltage regulator electrical specifications: Updated the footnote on V_{DD-HV_BALLAST}
Rev 5	27 February 2017	 In Family Comparison section: Updated the "MPC5746C Family Comparison" table. added "NVM Memory Map 1", "NVM Memory Map 2", and "RAM Memory Map" tables.
		 Updated the product version, flash memory size and optional fields information in Ordering Information section.
		 In Recommended Operating Conditions section, removed the note related to additional crossover current.
		 VDD_HV_C row added in "Voltage regulator electrical specifications" table in Voltage regulator electrical characteristics section.
		 In Voltage Monitor Electrical Characteristics section, updated the "Trimmed" Fall and Rise specs of VHVD_LV_cold parameter in "Voltage Monitor Electrical Characteristics" table.
		 In AC Electrical Specifications: 3.3 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. In DC Electrical Specifications: 3.3 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" and updated "Vol min and max" values in the table. In AC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. In AC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. In DC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" and updated "Vol min and max" values in the table.
		 In "Flash memory AC timing specifications" table in Flash memory AC timing specifications section: Updated the "t_{psus}" typ value from 7 us to 9.4 us. Updated the "t_{psus}" max value from 9.1 us to 11.5 us.
		Added "Continuous SCK Timing" table in DSPI timing section.
		 Added "ADC pad leakage" at 105°C TA conditions in "ADC conversion characteristics (for 12-bit)" table in ADC electrical specifications section.
		 In "STANDBY Current consumption characteristics" table in Supply current characteristics section: Updated the Typ and max values of IDD Standby current. Added IDD Standby3 current spec for FIRC ON.
		 Removed IVDDHV and IVDDLV specs in 16 MHz RC Oscillator electrical specifications section.
		Added Reset Sequence section, with Reset Sequence Duration, BAF execution duration section, and Reset Sequence Distribution as its sub-sections.

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