



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, FlexRay, I <sup>2</sup> C, LINbus, SPI
Peripherals	DMA, I <sup>2</sup> S, POR, WDT
Number of I/O	129
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 36x10b, 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746bsk1vku2

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# **Table of Contents**

1	Block diagram4							
2	Family comparison4							
3	Orde	ring parts	ing parts8					
	3.1	Determi	ning valid orderable parts8					
	3.2	Ordering	g Information9					
4	Gene	eral	9					
	4.1	Absolute	e maximum ratings9					
	4.2	Recom	nended operating conditions11					
	4.3	Voltage	regulator electrical characteristics13					
	4.4	Voltage	monitor electrical characteristics17					
	4.5	Supply	current characteristics18					
	4.6	Electros	tatic discharge (ESD) characteristics22					
	4.7	Electror	nagnetic Compatibility (EMC) specifications23					
5	I/O p	arameter	s23					
	5.1	AC spec	cifications @ 3.3 V Range23					
	5.2	DC elec	trical specifications @ 3.3V Range24					
	5.3	AC spec	cifications @ 5 V Range25					
	5.4	DC elec	trical specifications @ 5 V Range25					
	5.5	Reset p	ad electrical characteristics26					
	5.6	PORST	electrical specifications					
6	Perip	heral ope	erating requirements and behaviours28					
	6.1	Analog.						
		6.1.1	ADC electrical specifications					
		6.1.2	Analog Comparator (CMP) electrical					
			specifications					
	6.2	Clocks a	and PLL interfaces modules34					
		6.2.1	Main oscillator electrical characteristics34					
		6.2.2	32 kHz Oscillator electrical specifications36					
		6.2.3	16 MHz RC Oscillator electrical					
			specifications					
		6.2.4	128 KHz Internal RC oscillator Electrical					
			specifications					
		6.2.5	PLL electrical specifications					
	6.3	Memory	interfaces					
		6.3.1	Flash memory program and erase					
			specifications					

	6.3.2	Flash memory Array Integrity and Margin
		Read specifications
	6.3.3	Flash memory module life specifications40
	6.3.4	Data retention vs program/erase cycles40
	6.3.5	Flash memory AC timing specifications41
	6.3.6	Flash read wait state and address pipeline
		control settings42
6.4	Commu	ication interfaces43
	6.4.1	DSPI timing43
	6.4.2	FlexRay electrical specifications49
		6.4.2.1 FlexRay timing49
		6.4.2.2 TxEN49
		6.4.2.3 TxD50
		6.4.2.4 RxD51
	6.4.3	Ethernet switching specifications52
	6.4.4	SAI electrical specifications53
6.5	Debug s	pecifications55
	6.5.1	JTAG interface timing55
	6.5.2	Nexus timing58
	6.5.3	WKPU/NMI timing60
	6.5.4	External interrupt timing (IRQ pin)61
Ther	mal attribu	tes61
7.1	Thermal	attributes61
Dime	nsions	
8.1	Obtainin	g package dimensions65
Pinou	uts	
9.1	Package	pinouts and signal descriptions
Rese	t sequend	e66
10.1	Reset se	quence66
	10.1.1	Reset sequence duration
	10.1.2	BAF execution duration
	10.1.3	Reset sequence description
Revis	sion Histo	у69
11.1	Revision	History

MPC5746C Microcontroller Datasheet Data Sheet, Rev. 5.1, 05/2017.

#### Family comparison

### Table 1. MPC5746C Family Comparison1 (continued)

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C	
l <sup>2</sup> C	4	4	4	4			
SAI/I <sup>2</sup> S	3	3	3		3		
FXOSC			8 - 40	) MHz			
SXOSC			32	KHz			
FIRC			16 1	MHz			
SIRC			128	KHz			
FMPLL				1			
Low Power Unit (LPU)			Y	es			
FlexRay 2.1 (dual channel)	Yes, 128 MB	Yes, 128 MB	Yes, 128 MB		Yes, 128 MB		
Ethernet (RMII, MII + 1588, Muti queue AVB support)	1	1	1		1		
CRC			-	1			
MEMU			2	2			
STCU2			-	1			
HSM-v2 (security)			Opti	onal			
Censorship			Y	es			
FCCU			-	1			
Safety level			Specific functions	ASIL-B certifiable			
User MBIST			Y	es			
I/O Retention in Standby			Y	es			
GPIO <sup>6</sup>			Up to 264 GPI an	d up to 246 GPIO			
Debug			JTA	GC,			
			cJT	AG			
Nexus		Z4 N3+ (C	Only available on 3	24BGA (developm	ent only))		
		Z2 N3+ (C	Only available on 3	24BGA (developm	ient only))		
Packages	176 LQFP-EP	176 LQFP-EP	176 LQFP-EP	176 LQFP-EP	176 LQFP-EP	176 LQFP-EP	
	256 BGA	256 BGA	256 BGA	256 BGA	256 BGA	256 BGA,	
	100 BGA	100 BGA	100 BGA	100 BGA	100 BGA	324 BGA (development only)	
						100 BGA	

1. Feature set dependent on selected peripheral multiplexing, table shows example. Peripheral availability is package dependent.

- 2. Based on 125°C ambient operating temperature and subject to full device characterization.
- 3. Contact NXP representative for part number
- 4. Additional SWT included when HSM option selected
- 5. See device datasheet and reference manual for information on to timer channel configuration and functions.
- 6. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.





Figure 2. Voltage regulator capacitance connection

## NOTE

On BGA, VSS\_LV and VSS\_HV have been joined on substrate and renamed as VSS.

Table 8.	Voltage regulator	electrical	specifications
	<b>U U</b>		-

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C <sub>fp_reg</sub> 1	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2 <sup>2</sup>	3	μF
	Combined ESR of external capacitor	_	0.001	_	0.03	Ohm
C <sub>lp/ulp_reg</sub>	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	μF
	Combined ESR of external capacitor	_	0.001	—	0.1	Ohm
C <sub>be_fpreg</sub> <sup>3</sup>	Capacitor in parallel to base-	BCP68 and BCP56		3.3		nF
	emitter	MJD31		4.7		

- e200Z4 core, 160MHz, cache enabled; e200Z4 core, 80MHz; HSM fully operational (Z0 core @80MHz) FlexRay, 5x CAN, 5x LINFlexD, 2x SPI, 1x ADC used constantly, 1xeMIOS (5 ch), Memory: 3M flash, 384K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
- 9. Assuming Ta=Tj, as the device is in Stop mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes.
- 10. Internal structures hold the input voltage less than V<sub>DD\_HV\_ADC\_REF</sub> + 1.0 V on all pads powered by V<sub>DDA</sub> supplies, if the maximum injection current specification is met (3 mA for all pins) and V<sub>DDA</sub> is within the operating voltage specifications.
- 11. This value is the total current for two ADCs.Each ADC might consume upto 2mA at max.
- 12. This assumes the default configuration of flash controller register. For more details, refer to Flash memory program and erase specifications

Table 11. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions <sup>1</sup>	Min	Тур	Max	Unit
LPU_RUN	with 256K RAM	$T_a = 25 \ ^{\circ}C$	-	10	—	mA
		SYS_CLK = 16MHz				
		ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF				
		T <sub>a</sub> = 85 °C	—	10.5	_	
		SYS_CLK = 16MHz				
		ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON				
		T <sub>a</sub> = 105 °C	—	11	—	
		SYS_CLK = 16MHz				
		ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON				
		$T_a = 125 \ ^{\circ}C^{2, 2}$	—	—	26	
		SYS_CLK = 16MHz				
		ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON				
LPU_STOP	with 256K RAM	T <sub>a</sub> = 25 °C	—	0.18	—	mA
		T <sub>a</sub> = 85 °C	—	0.60	_	
		T <sub>a</sub> = 105 °C	—	1.00	_	
		$T_{a} = 125 \text{ °C }^{2}$	—	_	10.6	

- 1. The content of the Conditions column identifies the components that draw the specific current.
- Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

Table 12. STANDBY Current consumption characteristics

Symbol	Parameter	Conditions <sup>1</sup>	Min	Тур	Мах	Unit
STANDBY0	STANDBY with	T <sub>a</sub> = 25 °C	—	71	—	μA
	8K RAM	T <sub>a</sub> = 85 °C	_	125	700	
		T <sub>a</sub> = 105 °C	—	195	1225	
		$T_a = 125 \text{ °C}^{2,2}$	—	314	2100	
STANDBY1	STANDBY with 64K RAM	T <sub>a</sub> = 25 °C	_	72	_	μA
		T <sub>a</sub> = 85 °C	—	140	715	
		T <sub>a</sub> = 105 °C	—	225	1275	
		$T_{a} = 125 \text{ °C}^{2}$	—	358	2250	

## 4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

## 5 I/O parameters

## 5.1 AC specifications @ 3.3 V Range

Prop. Delay (ns) <sup>1</sup> L>H/H>L		<sup>1</sup> Rise/Fall Edge (n		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
Min	Max	Min	Max		MSB,LSB
	6/6		1.9/1.5	25	11
2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
6.4/5	19.5/19.5	3.5/2.5	12/12	200	
2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
0.090	1.1	0.035	1.1	asymmetry <sup>2</sup>	
2.9/3.5	12.5/11	1/1	7/6	50	
11/8	35/31	7.7/5	25/21	200	
8.3/9.6	45/45	4/3.5	25/25	50	01 <sup>3</sup>
13.5/15	65/65	6.3/6.2	30/30	200	
13/13	75/75	6.8/6	40/40	50	00 <sup>3</sup>
21/22	100/100	11/11	51/51	200	
	2/2		0.5/0.5	0.5	NA
	Prop. De L>H Min 2.5/2.5 6.4/5 2.2/2.5 0.090 2.9/3.5 11/8 8.3/9.6 13.5/15 13/13 21/22	Prop. Delay (ns) <sup>1</sup> L>H/H>L         Min       Max         6/6         2.5/2.5       8.25/7.5         6.4/5       19.5/19.5         2.2/2.5       8/8         0.090       1.1         2.9/3.5       12.5/11         11/8       35/31         8.3/9.6       45/45         13.5/15       65/65         13/13       75/75         21/22       100/100         2/2       2/2	Prop. Delay (ns) <sup>1</sup> Rise/Fall           L>H/H>L         Min           Min         Max         Min           6/6	Prop. Delay (ns)' L>H/H>LRise/Fall Edge (ns)MinMaxMinMax $6/6$ 1.9/1.5 $2.5/2.5$ $8.25/7.5$ $0.8/0.6$ $3.25/3$ $6.4/5$ $19.5/19.5$ $3.5/2.5$ $12/12$ $2.2/2.5$ $8/8$ $0.55/0.5$ $3.9/3.5$ $0.090$ $1.1$ $0.035$ $1.1$ $2.9/3.5$ $12.5/11$ $1/1$ $7/6$ $11/8$ $35/31$ $7.7/5$ $25/21$ $8.3/9.6$ $45/45$ $4/3.5$ $25/25$ $13.5/15$ $65/65$ $6.3/6.2$ $30/30$ $13/13$ $75/75$ $6.8/6$ $40/40$ $21/22$ $100/100$ $11/11$ $51/51$ $2/2$ $2/2$ $0.5/0.5$	Prop. Delay (ns) ' L>H/H>LRise/Fall Edge (ns) Rise/Fall Edge (ns)Drive Load (pF)MinMaxMinMax $6/6$ 1.9/1.5252.5/2.58.25/7.50.8/0.63.25/350 $6.4/5$ 19.5/19.53.5/2.512/122002.2/2.58/80.55/0.53.9/3.5250.0901.10.0351.1asymmetry <sup>2</sup> 2.9/3.512.5/111/17/65011/835/317.7/525/212008.3/9.645/454/3.525/255013.5/1565/656.3/6.230/3020013/1375/756.8/640/405021/22100/10011/1151/51200

### Table 14. Functional Pad AC Specifications @ 3.3 V Range

1. As measured from 50% of core side input to Voh/Vol of the output

- This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.
- 3. Slew rate control modes
- 4. Input slope = 2ns

## NOTE

The specification given above is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

### NOTE

The specification given above is measured between 20% / 80%.

Symbol	Parameter	Conditions	Min	Typ <sup>1</sup>	Max	Unit
R <sub>AD</sub> <sup>6</sup>	Internal resistance of analog source	—	_	_	825	Ω
INL	Integral non-linearity (precise channel)	—	-2	_	2	LSB
INL	Integral non-linearity (standard channel)	—	-3	—	3	LSB
DNL	Differential non-linearity	—	-1	—	1	LSB
OFS	Offset error	—	-6	—	6	LSB
GNE	Gain error	—	-4	_	4	LSB
ADC Analog Pad	Max leakage (precision channel)	150 °C	_		250	nA
(pad going to one	Max leakage (standard channel)	150 °C	—	—	2500	nA
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Max leakage (standard channel)	105 °C <sub>TA</sub>	—	5	250	nA
	Max positive/negative injection		-5		5	mA
TUEprecision channels	Total unadjusted error for precision	Without current injection	-6	+/-4	6	LSB
	channels	With current injection <sup>7, 7</sup>		+/-5		LSB
TUE <sub>standard/extended</sub>	Total unadjusted error for standard/	Without current injection	-8	+/-6	8	LSB
channels	extended channels	With current injection <sup>7</sup>		+/-8		LSB
t <sub>recovery</sub>	STOP mode to Run mode recovery time				< 1	μs

### Table 20. ADC conversion characteristics (for 12-bit) (continued)

- Active ADC input, VinA < [min(ADC\_VrefH, ADC\_ADV, VDD\_HV\_IOx)]. VDD\_HV\_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD\_HV\_x = 3.3 V)' for required relation between IO\_supply\_A,B,C and ADC\_Supply.</li>
- 2. The internally generated clock (known as AD\_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C<sub>S</sub> can be charged/discharged by the external source. The internal
  resistance of the analog source must allow the capacitance to reach its final voltage level within t<sub>sample</sub>. After the end of the
  sample time t<sub>sample</sub>, changes of the analog input voltage have no effect on the conversion result. Values for the sample
  clock t<sub>sample</sub> depend on programming.
- This parameter does not include the sample time t<sub>sample</sub>, but only the time for determining the digital result and the time to load the result register with the conversion result.
- 5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
- 6. See Figure 6.
- 7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

### Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ <sup>1</sup>	Max	Unit
fск	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK <sup>2</sup> frequency.)	_	15.2	80	80	MHz
f <sub>s</sub>	Sampling frequency	_	—	—	1.00	MHz
t <sub>sample</sub>	Sample time <sup>3</sup>	80 MHz@ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

Symbol	Parameter	Conditions	Min	Typ <sup>1</sup>	Max	Unit
t <sub>conv</sub>	Conversion time <sup>4</sup>	80 MHz	550	—	—	ns
t <sub>total_conv</sub>	Total Conversion time tsample + tconv (for standard channels)	80 MHz	1			μs
	Total Conversion time tsample + tconv (for extended channels)		1.5	_		
C <sub>S</sub> <sup>5</sup>	ADC input sampling capacitance	—	_	3	5	pF
C <sub>P1</sub> <sup>5</sup>	ADC input pin capacitance 1	—	_	—	5	pF
C <sub>P2</sub> <sup>5</sup>	ADC input pin capacitance 2	—		—	0.8	pF
R <sub>SW1</sub> <sup>5</sup>	Internal resistance of analog	$V_{REF}$ range = 4.5 to 5.5 V	_	—	0.3	kΩ
	source	$V_{REF}$ range = 3.15 to 3.6 V	_	—	875	Ω
R <sub>AD</sub> <sup>5</sup>	Internal resistance of analog source	_	—	_	825	Ω
INL	Integral non-linearity	—	-2	—	2	LSB
DNL	Differential non-linearity	—	-1	—	1	LSB
OFS	Offset error	—	-4	—	4	LSB
GNE	Gain error	—	-4	—	4	LSB
ADC Analog Pad	Max leakage (standard channel)	150 °C		—	2500	nA
(pad going to one	Max positive/negative injection		-5	—	5	mA
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Max leakage (standard channel)	105 °C <sub>TA</sub>		5	250	nA
TUE <sub>standard/extended</sub>	Total unadjusted error for standard	Without current injection	-4	+/-3	4	LSB
channels	channels	With current injection <sup>6</sup>		+/-4		LSB
t <sub>recovery</sub>	STOP mode to Run mode recovery time				< 1	μs

 Table 21. ADC conversion characteristics (for 10-bit) (continued)

- Active ADC Input, VinA < [min(ADC\_ADV, IO\_Supply\_A,B,C)]. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO\_supply\_A, B, C and ADC\_Supply.</li>
- 2. The internally generated clock (known as AD\_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C<sub>S</sub> can be charged/discharged by the external source. The internal
  resistance of the analog source must allow the capacitance to reach its final voltage level within t<sub>sample</sub>. After the end of the
  sample time t<sub>sample</sub>, changes of the analog input voltage have no effect on the conversion result. Values for the sample
  clock t<sub>sample</sub> depend on programming.
- 4. This parameter does not include the sample time t<sub>sample</sub>, but only the time for determining the digital result and the time to load the result register with the conversion result.
- 5. See Figure 65
- 6. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

## 6.4 Communication interfaces

## 6.4.1 DSPI timing

Table 35. DSPI electrical specifications

No	Symbol	Parameter	Conditions	High Speed Mode		low Spe	ed mode	Unit
				Min	Max	Min	Max	1
1	t <sub>SCK</sub>	DSPI cycle	Master (MTFE = 0)	25	—	50	_	ns
		time	Slave (MTFE = 0)	40	_	60	_	1
2	t <sub>csc</sub>	PCS to SCK delay	_	16	_	_	-	ns
3	t <sub>ASC</sub>	After SCK delay	_	16	_	_	_	ns
4	t <sub>SDC</sub>	SCK duty cycle		t <sub>SCK</sub> /2 - 10	t <sub>SCK</sub> /2 + 10	_	_	ns
5	t <sub>A</sub>	Slave access time	SS active to SOUT valid	_	40	—	_	ns
6	t <sub>DIS</sub>	Slave SOUT disable time	<sub>SS</sub> inactive to SOUT High-Z or invalid		10	_	_	ns
7	t <sub>PCSC</sub>	PCSx to PCSS time	_	13		_	_	ns
8	t <sub>PASC</sub>	PCSS to PCSx time	_	13		_	_	ns
9	t <sub>SUI</sub>	Data setup	Master (MTFE = 0)	NA	—	20	—	ns
		time for	Slave	2	—	2	_	
		inputo	Master (MTFE = 1, CPHA = 0)	15		8 <sup>1, 1</sup>	_	
			Master (MTFE = 1, CPHA = 1)	15		20	-	
10	t <sub>HI</sub>	Data hold	Master (MTFE = 0)	NA	—	-5	—	ns
		time for	Slave	4	—	4	—	
		mpate	Master (MTFE = 1, CPHA = 0)	0		11 <sup>1</sup>	-	
			Master (MTFE = 1, CPHA = 1)	0		-5	_	
11	t <sub>SUO</sub>	Data valid	Master (MTFE = 0)	_	NA	—	4	ns
		(after SCK	Slave	_	15	_	23	1
			Master (MTFE = 1, CPHA = 0)	_	4	_	16 <sup>1</sup>	
			Master (MTFE = 1, CPHA = 1)	—	4	—	4	

No	Symbol	Parameter	arameter Conditions		High Speed Mode		ed mode	Unit
				Min	Мах	Min	Max	
12 t <sub>HO</sub>	t <sub>HO</sub>	Data hold time for outputs	Master (MTFE = 0)	NA	_	-2	_	ns
			Slave	4	—	6	—	
			Master (MTFE = 1, CPHA = 0)	-2	—	10 <sup>1</sup>	—	
			Master (MTFE = 1, CPHA = 1)	-2		-2	—	

Table 35. DSPI electrical specifications (continued)

1. SMPL\_PTR should be set to 1

### NOTE

Restriction For High Speed modes

- DSPI2, DSPI3, SPI1 and SPI2 will support 40MHz Master mode SCK
- DSPI2, DSPI3, SPI1 and SPI2 will support 25MHz Slave SCK frequency
- Only one {SIN,SOUT and SCK} group per DSPI/SPI will support high frequency mode
- For Master mode MTFE will be 1 for high speed mode
- For high speed slaves, their master have to be in MTFE=1 mode or should be able to support 15ns tSUO delay

## NOTE

For numbers shown in the following figures, see Table 35

Table 36.	Continuous	SCK	timing
-----------	------------	-----	--------

Spec	Characteristics	Pad Drive/Load	Value	
			Min	Мах
tSCK	SCK cycle timing	strong/50 pF	100 ns	-
-	PCS valid after SCK	strong/50 pF	-	15 ns
-	PCS valid after SCK	strong/50 pF	-4 ns	-

Table 37.	DSPI high speed mode I/C	)s
-----------	--------------------------	----

DSPI	High speed SCK	High speed SIN	High speed SOUT
DSPI2	GPIO[78]	GPIO[76]	GPIO[77]
DSPI3	GPIO[100]	GPIO[101]	GPIO[98]
SPI1	GPIO[173]	GPIO[175]	GPIO[176]
SPI2	GPIO[79]	GPIO[110]	GPIO[111]



Figure 14. DSPI modified transfer format timing – slave, CPHA = 0



Figure 15. DSPI modified transfer format timing — slave, CPHA = 1



Figure 16. DSPI PCS strobe (PCSS) timing

No	Parameter	Value		Unit
		Min	Max	
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

Table 44. Slave mode SAI Timing (continued)



Figure 24. Slave mode SAI Timing

## 6.5 Debug specifications

## 6.5.1 JTAG interface timing

Table 45. JTAG pin AC electrical characteristics <sup>1</sup>

#	Symbol	Characteristic	Min	Мах	Unit
1	t <sub>JCYC</sub>	TCK Cycle Time <sup>2, 2</sup>	62.5	—	ns
2	t <sub>JDC</sub>	TCK Clock Pulse Width	40	60	%
3	t <sub>TCKRISE</sub>	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t <sub>TMSS</sub> , t <sub>TDIS</sub>	TMS, TDI Data Setup Time	5	_	ns
5	t <sub>TMSH</sub> , t <sub>TDIH</sub>	TMS, TDI Data Hold Time	5	_	ns
6	t <sub>TDOV</sub>	TCK Low to TDO Data Valid	—	20 <sup>3, 3</sup>	ns
7	t <sub>TDOI</sub>	TCK Low to TDO Data Invalid	0	_	ns
8	t <sub>TDOHZ</sub>	TCK Low to TDO High Impedance		15	ns
11	t <sub>BSDV</sub>	TCK Falling Edge to Output Valid	—	600 <sup>4, 4</sup>	ns

Table continues on the next page...

#### **Debug specifications**

### Table 45. JTAG pin AC electrical characteristics <sup>1</sup> (continued)

#	Symbol	Characteristic	Min	Мах	Unit
12	t <sub>BSDVZ</sub>	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t <sub>BSDHZ</sub>	TCK Falling Edge to Output High Impedance		600	ns
14	t <sub>BSDST</sub>	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t <sub>BSDHT</sub>	TCK Rising Edge to Boundary Scan Input Invalid	15	_	ns

- 1. These specifications apply to JTAG boundary scan only.
- 2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
- 3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
- 4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.



Figure 25. JTAG test clock input timing

**Debug specifications** 



Figure 30. Nexus TDI, TMS, TDO timing

## 6.5.3 WKPU/NMI timing

### Table 47. WKPU/NMI glitch filter

No.	Symbol	Parameter	Min	Тур	Max	Unit
1	W <sub>FNMI</sub>	NMI pulse width that is rejected	—	—	20	ns
2	W <sub>NFNMI</sub> D	NMI pulse width that is passed	400	_	—	ns

#### Thermal attributes

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
_	R <sub>θJC</sub>	Thermal resistance, junction to case	7.9	°C/W	55
	Ψ <sub>JT</sub>	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	66
	R <sub>0JB_CSB</sub>	Thermal characterization parameter, junction to package bottom outside center (natural convection)	9.0	°C/W	77

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal
- 4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
- 7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	100 MAPBGA	Unit	Notes
Single-layer (1s)	R <sub>0JA</sub>	Thermal resistance, junction to ambient (natural convection)	50.9	°C/W	1, 21,2
Four-layer (2s2p)	R <sub>0JA</sub>	Thermal resistance, junction to ambient (natural convection)	27.0	°C/W	1,2,33
Single-layer (1s)	R <sub>ejma</sub>	Thermal resistance, junction to ambient (200 ft./ min. air speed)	38.0	°C/W	1,3
Four-layer (2s2p)	R <sub>eJMA</sub>	Thermal resistance, junction to ambient (200 ft./ min. air speed)	22.2	°C/W	1,3

**Reset sequence** 















Figure 35. Functional reset sequence long



Figure 36. Functional reset sequence short

The reset sequences shown in Figure 35 and Figure 36 are triggered by functional reset events. RESET\_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET\_B low for the duration of the internal reset sequence. See the RGM\_FBRE register in the device reference manual for more information.

## **11 Revision History**

## 11.1 Revision History

The following table provides a revision history for this document.

Rev. No.	Date	Substantial Changes
Rev 1	14 March 2013	Initial Release

Rev. No.	Date	Substantial Changes
		<ul> <li>In section: Voltage monitor electrical characteristics         <ul> <li>Updated description for Low Voltage detector block.</li> <li>Added note, BCP56, MCP68 and MJD31 are guaranteed ballasts.</li> <li>In table: Voltage regulator electrical specifications                 <ul></ul></li></ul></li></ul>
		<ul> <li>In section: Supply current characteristics <ul> <li>In table: Current consumption characteristics</li> <li>I<sub>DD_BODY_4</sub>: Updated SYS_CLK to 120 MHz.</li> <li>I<sub>DD_BODY_4</sub>: Updated Max for T<sub>a</sub>= 105 °C fand 85 °C )</li> <li>I<sub>dd_STOP</sub>: Added condition for T<sub>a</sub>= 105 °C and removed Max value for T<sub>a</sub>= 85 °C.</li> <li>I<sub>DD_HV_ADC_REF</sub>: Added condition for T<sub>a</sub>= 105 °C and 85 °C and removed Max value for T<sub>a</sub>= 25 °C.</li> <li>I<sub>DD_HV_FLASH</sub>: Added condition for T<sub>a</sub>= 105 °C and 85 °C</li> </ul> </li> <li>In table: Low Power Unit (LPU) Current consumption characteristics <ul> <li>LPU_RUN and LPU_STOP: Added condition for T<sub>a</sub>= 105 °C and 85 °C</li> <li>In table: STANDBY Current consumption characteristics</li> <li>Added condition for T<sub>a</sub>= 105 °C for all entries.</li> </ul> </li> </ul>
		<ul> <li>In section: I/O parameters</li> <li>In table: Functional Pad AC Specifications @ 3.3 V Range <ul> <li>Updated values for 'pad_sr_hv (output)'</li> </ul> </li> <li>In table: DC electrical specifications @ 3.3V Range <ul> <li>Updateded Min and Max values for Vih and Vil respectively.</li> </ul> </li> <li>In table: Functional Pad AC Specifications @ 5 V Range <ul> <li>Updated values for 'pad_sr_hv (output)'</li> </ul> </li> <li>In table DC electrical specifications @ 5 V Range <ul> <li>Updated values for 'pad_sr_hv (output)'</li> </ul> </li> <li>In table DC electrical specifications @ 5 V Range <ul> <li>Updated values for 'pad_sr_hv (output)'</li> </ul> </li> </ul>

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes
		<ul> <li>In section: Reset pad electrical characteristics         <ul> <li>Revised table, Reset electrical characteristics</li> <li>Deleted note, There are some specific ports that supports TTL functionality. These ports are, PB[4], PB[5], PB[6], PB[7], PB[8], PB[9], PD[0], PD[1], PD[2], PD[3], PD[4], PD[5], PD[6], PD[7], PD[8], PD[9], PD[10], and PD[11].</li> </ul> </li> <li>In section: PORST electrical specifications         <ul> <li>Updated 'Min' value for W<sub>NFPORST</sub></li> </ul> </li> </ul>
		<ul> <li>In section: Peripheral operating requirements and behaviours</li> <li>Changed section title from Input impedance and ADC accuracy to Input equivalent circuit and ADC conversion characteristics.</li> <li>Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit)</li> <li>Removed table, ADC supply configurations.</li> </ul>
		<ul> <li>In section: Analogue Comparator (CMP) electrical specifications <ul> <li>In table: Comparator and 6-bit DAC electrical specifications</li> <li>Updated 'Max' value of I<sub>DDLS</sub></li> <li>Updated 'Min' and 'Max' for V<sub>AIO</sub> and DNL</li> <li>Updated 'Descripton' 'Min' 'Max' od V<sub>H</sub></li> <li>Updated row for t<sub>DHS</sub></li> <li>Added row for t<sub>DLS</sub></li> <li>Removed row for V<sub>CMPOh</sub> and V<sub>CMPOI</sub></li> </ul> </li> </ul>
		<ul> <li>In section: Clocks and PLL interfaces modules <ul> <li>In table: Main oscillator electrical characteristics</li> <li>V<sub>XOSCHS</sub>: Removed values for 4 MHz.</li> <li>T<sub>XOSCHSSU</sub>: Updated range to 8-40 MHz.</li> </ul> </li> <li>In table: 16 MHz RC Oscillator electrical specifications <ul> <li>Updated 'Max' for T<sub>startup</sub> and T<sub>LTJIT</sub></li> <li>Removed F<sub>Untrimmed</sub> row</li> </ul> </li> <li>In table: 128 KHz Internal RC oscillator electrical specifications <ul> <li>Fosc: Removed Uncaliberated 'Condition' and updated 'Min', 'Typ', and 'Max' for Caliberated condition</li> <li>Fosc: Updated 'Temperature dependence' and 'Supply dependence' Max values</li> </ul> </li> </ul>
		<ul> <li>In table: PLL electrical specifications</li> <li>Removed entries for Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (V<sub>DD_LV</sub>), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption</li> <li>Removed 'Typ' value for Duty Cycle at pllclkout</li> <li>Removed 'Min' value for Lock Time in calibration mode.</li> <li>In table: Jitter calculation</li> <li>Added 1 Sigma Random Jitter and Total Period Jitter values for Long Term Jitter (Interger and Fractional Mode) rows.</li> </ul>
		<ul> <li>In section Flash read wait state and address pipeline control settings</li> <li>In Flash Read Wait State and Address Pipeline Control: Updated APC for 40 MHz.</li> <li>Removed section: On-chip peripherals</li> </ul>

### Table 51. Revision History (continued)

Table 51.	Revision	History	(continued)
	11011011	1113101 y	(ooninaca)

Rev. No.	Date	Substantial Changes
Rev 3	2 March 2016	In section, Recommended operating conditions
		Added a new Note
		In section, Voltage regulator electrical characteristics
		<ul> <li>In table, Voltage regulator electrical specifications:</li> </ul>
		Added a new row for C <sub>HV_VDD_B</sub>
		<ul> <li>Added a footnote on V<sub>DD_HV_BALLAST</sub></li> <li>Added a new Note at the end of this section</li> </ul>
		In section, Voltage monitor electrical characteristics
		<ul> <li>In table, Voltage monitor electrical characteristics:</li> <li>Removed "Vue</li></ul>
		LPBG as reference" rows
		<ul> <li>Updated Fall and Rise trimmed Minimum values for V<sub>HVD_LV_cold</sub></li> </ul>
		In section, Supply current characteristics
		In table, Current consumption characteristics:
		<ul> <li>Updated the footnote mentioned in the Condition column of I<sub>DD_STOP</sub> row</li> </ul>
		Updated all TBD values     In table Low Power Unit (LBL) Current consumption above staristics:
		<ul> <li>In table, Low Power Onit (LPO) Current consumption characteristics.</li> <li>Updated the typical value of LPU_STOP to 0.18 mA</li> </ul>
		Updated all TBD values
		<ul> <li>In table, STANDBY Current consumption characteristics:</li> </ul>
		Updated all IBD values
		In section, AC specifications @ 3.3 V Range
		In table, Functional Pad AC Specifications @ 3.3 V Range:
		Updated Rise/Fall Edge values
		In section, DC electrical specifications @ 3.3V Range
		In table, DC electrical specifications @ 3.3V Range:
		<ul> <li>Updated Max value for Vol to 0.1 ^ VDD_HV_x</li> </ul>
		In section, AC specifications @ 5 V Range
		In table, Functional Pad AC Specifications @ 5 V Range:
		Updated Rise/Fall Edge values
		<ul> <li>In section, DC electrical specifications @ 5 V Range</li> </ul>
		In table, DC electrical specifications @ 5 V Range:
		<ul> <li>Updated Min and Max values for Pull_Ion and Pull_IoI rows</li> <li>Updated Max value for Vol to 0.1 * VDD_HV_x</li> </ul>
		In section, Reset pad electrical characteristics
		<ul> <li>In table, Functional reset pad electrical specifications:</li> <li>Updated parameter column for Val. Val. and Value rows</li> </ul>
		• Updated Min and Max values for $V_{IH}$ and $V_{IL}$ rows
		In section, PORST electrical specifications     In table_PORST electrical specifications:
		• Updated Unit and Min/Max values for $V_{IH}$ and $V_{IL}$ rows
		<ul> <li>In section, input equivalent size it and ADC conversion shorestaristics</li> </ul>
		<ul> <li>In section, input equivalent circuit and ADC conversion characteristics</li> <li>In table, ADC conversion characteristics (for 12-bit);</li> </ul>
		Updated "ADC Analog Pad (pad going to one ADC)" row
		In table, ADC conversion characteristics (for 10-bit):
		<ul> <li>Updated "ADC Analog Pad (pad going to one ADC)" row</li> </ul>
		In section, Analog Comparator (CMP) electrical specifications
		In table, Comparator and 6-bit DAC electrical specifications:
	MPC57	46C Microcontroller Datasheet Data Sheet, Rev. 5.1, 05/2017.
74		NXP Semiconductors
		In section, Main oscillator electrical characteristics

#### How to Reach Us:

Home Page: www.nxp.com

Web Support: www.nxp.com/support Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, C-5, CodeTest, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. ARM, AMBA, ARM Powered, Artisan, Cortex, Jazelle, Keil, SecurCore, Thumb, TrustZone, and µVision are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. ARM7, ARM9, ARM11, big.LITTLE, CoreLink, CoreSight, DesignStart, Mali, mbed, NEON, POP, Sensinode, Socrates, ULINK and Versatile are trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2017 NXP B.V.





Document Number: MPC5746C Rev. 5.1, 05/2017