



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, FlexRay, I ² C, LINbus, SPI
Peripherals	DMA, I ² S, POR, WDT
Number of I/O	129
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 36x10b, 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746bsk1vku2r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Debug functionality
 - e200z2 core:NDI per IEEE-ISTO 5001-2008 Class3+
 - e200z4 core: NDI per IEEE-ISTO 5001-2008 Class 3+
- Timer
 - 16 Periodic Interrupt Timers (PITs)
 - Two System Timer Modules (STM)
 - Three Software Watchdog Timers (SWT)
 - 64 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels
- Device/board boundary Scan testing supported with Joint Test Action Group (JTAG) of IEEE 1149.1 and IEEE 1149.7 (CJTAG)
- Security
 - Hardware Security Module (HSMv2)
 - Password and Device Security (PASS) supporting advanced censorship and life-cycle management
 - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Functional Safety
 - ISO26262 ASIL-B compliance
- Multiple operating modes
 - Includes enhanced low power operation

Family comparison

Table 1. MPC5746C Family Comparison1 (continued)

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C
l ² C	4	4	4		4	•
SAI/I ² S	3	3	3		3	
FXOSC			8 - 40) MHz		
SXOSC			32	KHz		
FIRC			16 1	MHz		
SIRC			128	KHz		
FMPLL				1		
Low Power Unit (LPU)			Y	es		
FlexRay 2.1 (dual channel)	Yes, 128 MB	Yes, 128 MB	Yes, 128 MB		Yes, 128 MB	
Ethernet (RMII, MII + 1588, Muti queue AVB support)	1	1	1		1	
CRC			-	1		
MEMU			2	2		
STCU2			-	1		
HSM-v2 (security)			Opti	onal		
Censorship			Y	es		
FCCU			-	1		
Safety level			Specific functions	ASIL-B certifiable		
User MBIST			Y	es		
I/O Retention in Standby			Y	es		
GPIO ⁶			Up to 264 GPI an	d up to 246 GPIO		
Debug			JTA	GC,		
			cJT	AG		
Nexus		Z4 N3+ (C	Only available on 3	24BGA (developm	ent only))	
		Z2 N3+ (C	Only available on 3	24BGA (developm	ient only))	
Packages	176 LQFP-EP	176 LQFP-EP	176 LQFP-EP	176 LQFP-EP	176 LQFP-EP	176 LQFP-EP
	256 BGA	256 BGA	256 BGA	256 BGA	256 BGA	256 BGA,
	100 BGA	100 BGA	100 BGA	100 BGA	100 BGA	324 BGA (development only)
						100 BGA

1. Feature set dependent on selected peripheral multiplexing, table shows example. Peripheral availability is package dependent.

- 2. Based on 125°C ambient operating temperature and subject to full device characterization.
- 3. Contact NXP representative for part number
- 4. Additional SWT included when HSM option selected
- 5. See device datasheet and reference manual for information on to timer channel configuration and functions.
- 6. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.





Figure 2. Voltage regulator capacitance connection

NOTE

On BGA, VSS_LV and VSS_HV have been joined on substrate and renamed as VSS.

Table 8.	Voltage regulator	electrical	specifications
	U U		-

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{fp_reg} 1	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2 ²	3	μF
	Combined ESR of external capacitor	_	0.001	_	0.03	Ohm
C _{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	μF
	Combined ESR of external capacitor	_	0.001	—	0.1	Ohm
C _{be_fpreg} ³	Capacitor in parallel to base-	BCP68 and BCP56		3.3		nF
	emitter	MJD31		4.7		

Table continues on the next page ...

General

- 5. 1. For VDD_HV_x, 1µf on each side of the chip
 - a. 0.1 μ f close to each VDD/VSS pin pair.
 - b. 10 μf near for each power supply source
 - c. For VDD_LV, 0.1uf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter.
 - For VDD_LV, 0.1uf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this
 amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as
 specified by CFP_REG parameter
- 6. Only applicable to ADC1
- 7. In external ballast configuration the following must be ensured during power-up and power-down (Note: If V_{DD_HV_BALLAST} is supplied from the same source as VDD_HV_A this condition is implicitly met):
 - During power-up, V_{DD_HV_BALLAST} must have met the min spec of 2.25V before VDD_HV_A reaches the POR_HV_RISE min of 2.75V.
 - During power-down, $V_{DD_HV_BALLAST}$ must not drop below the min spec of 2.25V until VDD_HV_A is below POR_HV_FALL min of 2.7V.

NOTE

For a typical configuration using an external ballast transistor with separate supply for VDD_HV_A and the ballast collector, a bulk storage capacitor (as defined in Table 8) is required on VDD_HV_A close to the device pins to ensure a stable supply voltage.

Extra care must be taken if the VDD_HV_A supply is also being used to power the external ballast transistor or the device is running in internal regulation mode. In these modes, the inrush current on device Power Up or on exit from Low Power Modes is significant and may case the VDD_HV_A voltage to drop resulting in an LVD reset event. To avoid this, the board layout should be optimized to reduce common trace resistance or additional capacitance at the ballast transistor collector (or VDD_HV_A pins in the case of internal regulation mode) is required. NXP recommends that customers simulate the external voltage supply circuitry.

In all circumstances, the voltage on VDD_HV_A must be maintained within the specified operating range (see Recommended operating conditions) to prevent LVD events.

5.2 DC electrical specifications @ 3.3V Range

Table 15. DC electrical specifications @ 3.3V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	Pad_I_HV Input Buffer High Voltage	0.72*VDD_HV_ x	VDD_HV_x + 0.3	V
Vil (pad_i_hv)	Pad_I_HV Input Buffer Low Voltage	VDD_HV_x - 0.3	0.45*VDD_HV_ x	V
Vhys (pad_i_hv)	Pad_I_HV Input Buffer Hysteresis	0.11*VDD_HV_ x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.67*VDD_HV_ x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VDD_HV_x - 0.3	0.35*VDD_HV_ x	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.57 * VDD_HV_x ^{1, 1}	VDD_HV_x ¹ + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VDD_HV_x - 0.3	0.4 * VDD_HV_x ¹	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x ¹		V
Pull_IIH (pad_i_hv)	Weak Pullup Current ^{2, 2} Low	15		μA
Pull_IIH (pad_i_hv)	Weak Pullup Current ^{3, 3} High		55	μΑ
Pull_IIL (pad_i_hv)	Weak Pulldown Current ³ Low	28		μΑ
Pull_IIL (pad_i_hv)	Weak Pulldown Current ² High		85	μΑ
Pull_loh	Weak Pullup Current ⁴	15	50	μA
Pull_lol	Weak Pulldown Current ⁵	15	50	μA
linact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	μΑ
Voh	Output High Voltage ⁶	0.8 *VDD_HV_x ¹	_	V
Vol	Output Low Voltage ⁷	_	0.2 *VDD_HV_x ¹	V
			0.1 *VDD_HV_x	
loh_f	Full drive loh ^{9, 9} (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
lol_f	Full drive lol ⁹ (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
loh_h	Half drive loh ⁹ (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
lol_h	Half drive Iol ⁹ (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

- 1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
- 2. Measured when pad=0.69*VDD_HV_x
- 3. Measured when pad=0.49*VDD_HV_x
- 4. Measured when pad = 0 V
- 5. Measured when pad = VDD_HV_x
- 6. Measured when pad is sourcing 2 mA
- 7. Measured when pad is sinking 2 mA
- 8. Measured when pad is sinking 1.5 mA $\,$
- 9. Ioh/IoI is derived from spice simulations. These values are NOT guaranteed by test.

I/O parameters









Table 18.	Functional reset	pad electrical s	pecifications
-----------	------------------	------------------	---------------

Symbol	Parameter	Conditions	Value		Unit	
			Min	Тур	Мах	
V _{IH}	CMOS Input Buffer High Voltage	—	0.65*V _D	_	V _{DD_HV_x}	V
			D_HV_x		+0.3	
VIL	CMOS Input Buffer Low Voltage	—	V _{DD_HV_}	—	0.35*V _{DD_HV}	V
			_x -0.3		_x	

Table continues on the next page...



Figure 5. ADC characteristics and error definitions

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
R _{AD} ⁶	Internal resistance of analog source	—	_	_	825	Ω
INL	Integral non-linearity (precise channel)	—	-2	_	2	LSB
INL	Integral non-linearity (standard channel)	—	-3	—	3	LSB
DNL	Differential non-linearity	—	-1	—	1	LSB
OFS	Offset error	—	-6	—	6	LSB
GNE	Gain error	—	-4	—	4	LSB
ADC Analog Pad	Max leakage (precision channel)	150 °C	_		250	nA
(pad going to one	Max leakage (standard channel)	150 °C	—	—	2500	nA
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Max leakage (standard channel)	105 °C _{TA}	—	5	250	nA
	Max positive/negative injection		-5		5	mA
TUEprecision channels	Total unadjusted error for precision	Without current injection	-6	+/-4	6	LSB
	channels	With current injection ^{7, 7}		+/-5		LSB
TUE _{standard/extended}	Total unadjusted error for standard/	Without current injection	-8	+/-6	8	LSB
channels	extended channels	With current injection ⁷		+/-8		LSB
t _{recovery}	STOP mode to Run mode recovery time				< 1	μs

Table 20. ADC conversion characteristics (for 12-bit) (continued)

- Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
- 2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal
 resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the
 sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample
 clock t_{sample} depend on programming.
- This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
- 5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
- 6. See Figure 6.
- 7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
fск	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK ² frequency.)	_	15.2	80	80	MHz
f _s	Sampling frequency	_	—	—	1.00	MHz
t _{sample}	Sample time ³	80 MHz@ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

Type of jitter	Jitter due to Supply Noise (ps) J _{SN} ¹	Jitter due to Fractional Mode (ps) J _{SDM} ²	Jitter due to Fractional Mode J _{SSCG} (ps) ³	1 Sigma Random Jitter J _{RJ} (ps) ⁴	Total Period Jitter (ps)
Long Term Jitter (Integer Mode)				40	+/-(N x J _{RJ})
Long Term jitter (Fractional Mode)				100	+/-(N x J _{RJ})

Table 28. Jitter calculation (continued)

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on VDD_LV and VSS_LV.

2. This jitter component is added when the PLL is working in the fractional mode.

3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.

4. The value of N is dependent on the accuracy requirement of the application. See Table 29

Table 29. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27
4	6.30 × 1e-03
5	5.63 × 1e-05
6	2.00 × 1e-07
7	2.82 × 1e-10

6.3 Memory interfaces

6.3.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.



6.3.5 Flash memory AC timing specifications Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t _{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	_	9.4 plus four system clock periods	11.5 plus four system clock periods	μs
t _{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	_	16 plus four system clock periods	20.8 plus four system clock periods	μs
t _{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	_	100	ns
t _{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	_	5	ns
t _{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.		16 plus four system clock periods	20.8 plus four system clock periods	μs

Table continues on the next page...

Symbol	Characteristic	Min	Typical	Max	Units
t _{drov}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	_	45 plus seven system clock periods	μs
t _{aistart}	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP			5	ns
t _{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	_	_	80 plus fifteen system clock periods	ns
t _{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	_	20.42 plus four system clock periods	μs

 Table 33.
 Flash memory AC timing specifications (continued)

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

 Table 34.
 Flash Read Wait State and Address Pipeline Control Combinations

Flash frequency	RWSC setting	APC setting
0 MHz < fFlash <= 33 MHz	0	0
33 MHz < fFlash <= 100 MHz	2	1
100 MHz < fFlash <= 133 MHz	3	1
133 MHz < fFlash <= 160 MHz	4	1

6.4 Communication interfaces

6.4.1 DSPI timing

Table 35. DSPI electrical specifications

No	Symbol	Parameter	Conditions	High Speed Mode		low Spe	ed mode	Unit
				Min	Мах	Min	Max	1
1	t _{SCK}	DSPI cycle	Master (MTFE = 0)	25	_	50		ns
		time	Slave (MTFE = 0)	40	_	60	_	1
2	t _{csc}	PCS to SCK delay	_	16	_	_	_	ns
3	t _{ASC}	After SCK delay	_	16	_	_	_	ns
4	t _{SDC}	SCK duty cycle		t _{SCK} /2 - 10	t _{SCK} /2 + 10	_	_	ns
5	t _A	Slave access time	SS active to SOUT valid		40	—	_	ns
6	t _{DIS}	Slave SOUT disable time	_{SS} inactive to SOUT High-Z or invalid		10	_	_	ns
7	t _{PCSC}	PCSx to PCSS time	_	13	_	_	_	ns
8	t _{PASC}	PCSS to PCSx time	_	13		_	_	ns
9	t _{sui}	Data setup	Master (MTFE = 0)	NA	—	20	_	ns
		time for	Slave	2	—	2	—	
		inputo	Master (MTFE = 1, CPHA = 0)	15	_	8 ^{1, 1}	_	
			Master (MTFE = 1, CPHA = 1)	15		20	_	
10	t _{HI}	Data hold	Master (MTFE = 0)	NA	—	-5	_	ns
		time for	Slave	4	—	4	_	
		inputo	Master (MTFE = 1, CPHA = 0)	0	_	11 ¹	_	
			Master (MTFE = 1, CPHA = 1)	0		-5	-	
11	t _{SUO}	Data valid	Master (MTFE = 0)	—	NA	_	4	ns
		(after SCK	Slave	_	15	—	23	1
			Master (MTFE = 1, CPHA = 0)	_	4	_	16 ¹	
			Master (MTFE = 1, CPHA = 1)	—	4	—	4	1

Table continues on the next page...



Figure 14. DSPI modified transfer format timing – slave, CPHA = 0



Figure 15. DSPI modified transfer format timing — slave, CPHA = 1



Figure 16. DSPI PCS strobe (PCSS) timing

Name	Description ¹	Min	Max	Unit
dCCTxD ₀₁	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxD ₁₀	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	_	25	ns

Table 39. TxD output characteristics (continued)

1. All parameters specified for $V_{DD_HV_IOx}$ = 3.3 V -5%, +±10%, TJ = -40 °C / 150 °C, TxD pin load maximum 25 pF.

2. For $3.3 \text{ V} \pm 10\%$ operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 20. TxD Signal propagation delays

6.4.2.4 RxD

Table 40.	RxD	input	characteristic
-----------	-----	-------	----------------

Name	Description ¹	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
dCCRxD ₀₁	Sum of delay from actual input to the D input of the first FF, rising edge	_	10	ns
dCCRxD ₁₀	Sum of delay from actual input to the D input of the first FF, falling edge	_	10	ns

Debug specifications



Figure 26. JTAG test access port timing

6.5.4 External interrupt timing (IRQ pin) Table 48. External interrupt timing specifications

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t _{IPWL}	IRQ pulse width low	—	3	—	t _{CYC}
2	t _{IPWH}	IRQ pulse width high	_	3	_	t _{CYC}
3	t _{ICYC}	IRQ edge to edge time	_	6		t _{CYC}

These values applies when IRQ pins are configured for rising edge or falling edge events, but not both.



Figure 31. External interrupt timing

7 Thermal attributes

7.1 Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Single-layer (1s)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	50.7	°C/W	11, 22
Four-layer (2s2p)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	24.2	°C/W	1, 2, 33
Single-layer (1s)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	38.1	°C/W	1, 3

Table continues on the next page ...

Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Four-layer (2s2p)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	17.8	°C/W	1, 3
_	R _{θJB}	Thermal resistance, junction to board	10.9	°C/W	44
_	R _{θJC}	Thermal resistance, junction to case	8.4	°C/W	55
_	Ψ _{JT}	Thermal resistance, junction to package top	0.5	°C/W	66
_	Ψ _{JB}	Thermal characterization parameter, junction to package bottom	0.3	°C/W	77

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal.
- 4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
- 7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	31.0	°C/W	11, 22
Four-layer (2s2p)	R _{0JA}	Thermal resistance, junction to ambient (natural convection)	24.3	°C/W	1,2,33
Single-layer (1s)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	23.5	°C/W	1, 3
Four-layer (2s2p)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	20.1	°C/W	1,3

Table continues on the next page...

Reset sequence















Figure 35. Functional reset sequence long

Rev. No.	Date	Substantial Changes
		 In section: Reset pad electrical characteristics Revised table, Reset electrical characteristics Deleted note, There are some specific ports that supports TTL functionality. These ports are, PB[4], PB[5], PB[6], PB[7], PB[8], PB[9], PD[0], PD[1], PD[2], PD[3], PD[4], PD[5], PD[6], PD[7], PD[8], PD[9], PD[10], and PD[11]. In section: PORST electrical specifications Updated 'Min' value for W_{NFPORST}
		 In section: Peripheral operating requirements and behaviours Changed section title from Input impedance and ADC accuracy to Input equivalent circuit and ADC conversion characteristics. Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit) Removed table, ADC supply configurations.
		 In section: Analogue Comparator (CMP) electrical specifications In table: Comparator and 6-bit DAC electrical specifications Updated 'Max' value of I_{DDLS} Updated 'Min' and 'Max' for V_{AIO} and DNL Updated 'Descripton' 'Min' 'Max' od V_H Updated row for t_{DHS} Added row for t_{DLS} Removed row for V_{CMPOh} and V_{CMPOI}
		 In section: Clocks and PLL interfaces modules In table: Main oscillator electrical characteristics V_{XOSCHS}: Removed values for 4 MHz. T_{XOSCHSSU}: Updated range to 8-40 MHz. In table: 16 MHz RC Oscillator electrical specifications Updated 'Max' for T_{startup} and T_{LTJIT} Removed F_{Untrimmed} row In table: 128 KHz Internal RC oscillator electrical specifications Fosc: Removed Uncaliberated 'Condition' and updated 'Min', 'Typ', and 'Max' for Caliberated condition Fosc: Updated 'Temperature dependence' and 'Supply dependence' Max values
		 In table: PLL electrical specifications Removed entries for Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (V_{DD_LV}), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption Removed 'Typ' value for Duty Cycle at pllclkout Removed 'Min' value for Lock Time in calibration mode. In table: Jitter calculation Added 1 Sigma Random Jitter and Total Period Jitter values for Long Term Jitter (Interger and Fractional Mode) rows.
		 In section Flash read wait state and address pipeline control settings In Flash Read Wait State and Address Pipeline Control: Updated APC for 40 MHz. Removed section: On-chip peripherals

Table 51. Revision History (continued)

Table continues on the next page ...