

Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746cbk1avku6

- Debug functionality
 - e200z2 core: NDI per IEEE-ISTO 5001-2008 Class3+
 - e200z4 core: NDI per IEEE-ISTO 5001-2008 Class 3+
- Timer
 - 16 Periodic Interrupt Timers (PITs)
 - Two System Timer Modules (STM)
 - Three Software Watchdog Timers (SWT)
 - 64 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels
- Device/board boundary Scan testing supported with Joint Test Action Group (JTAG) of IEEE 1149.1 and IEEE 1149.7 (CJTAG)
- Security
 - Hardware Security Module (HSMv2)
 - Password and Device Security (PASS) supporting advanced censorship and life-cycle management
 - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Functional Safety
 - ISO26262 ASIL-B compliance
- Multiple operating modes
 - Includes enhanced low power operation

Table 1. MPC5746C Family Comparison¹ (continued)

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C
I ² C	4	4	4	4		
SAI/I ² S	3	3	3	3		
FXOSC	8 - 40 MHz					
SXOSC	32 KHz					
FIRC	16 MHz					
SIRC	128 KHz					
FMPLL	1					
Low Power Unit (LPU)	Yes					
FlexRay 2.1 (dual channel)	Yes, 128 MB	Yes, 128 MB	Yes, 128 MB	Yes, 128 MB		
Ethernet (RMII, MII + 1588, Multi queue AVB support)	1	1	1	1		
CRC	1					
MEMU	2					
STCU2	1					
HSM-v2 (security)	Optional					
Censorship	Yes					
FCCU	1					
Safety level	Specific functions ASIL-B certifiable					
User MBIST	Yes					
I/O Retention in Standby	Yes					
GPIO ⁶	Up to 264 GPI and up to 246 GPIO					
Debug	JTAGC, cJTAG					
Nexus	Z4 N3+ (Only available on 324BGA (development only)) Z2 N3+ (Only available on 324BGA (development only))					
Packages	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA, 324 BGA (development only) 100 BGA

1. Feature set dependent on selected peripheral multiplexing, table shows example. Peripheral availability is package dependent.
2. Based on 125°C ambient operating temperature and subject to full device characterization.
3. Contact NXP representative for part number
4. Additional SWT included when HSM option selected
5. See device datasheet and reference manual for information on to timer channel configuration and functions.
6. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

4. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. $V_{IN1_CMP_REF} \leq V_{DD_HV_A}$
6. This supply is shorted VDD_HV_A on lower packages.
7. $T_J=150^{\circ}\text{C}$. Assumes $T_A=125^{\circ}\text{C}$
 - Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#)

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
 - Control of external NPN ballast transistor
 - Generating core supply using internal ballast transistor
 - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD_HV_IO_A}$ supply
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD_HV_IO_A}$ supply
- Low voltage detector (LVD_FLASH) for 3.3 V flash supply ($V_{DD_HV_FLA}$)
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors¹ are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for I_{dd} , collector voltage, etc

1. BCP56, MCP68 and MJD31 are guaranteed ballasts.

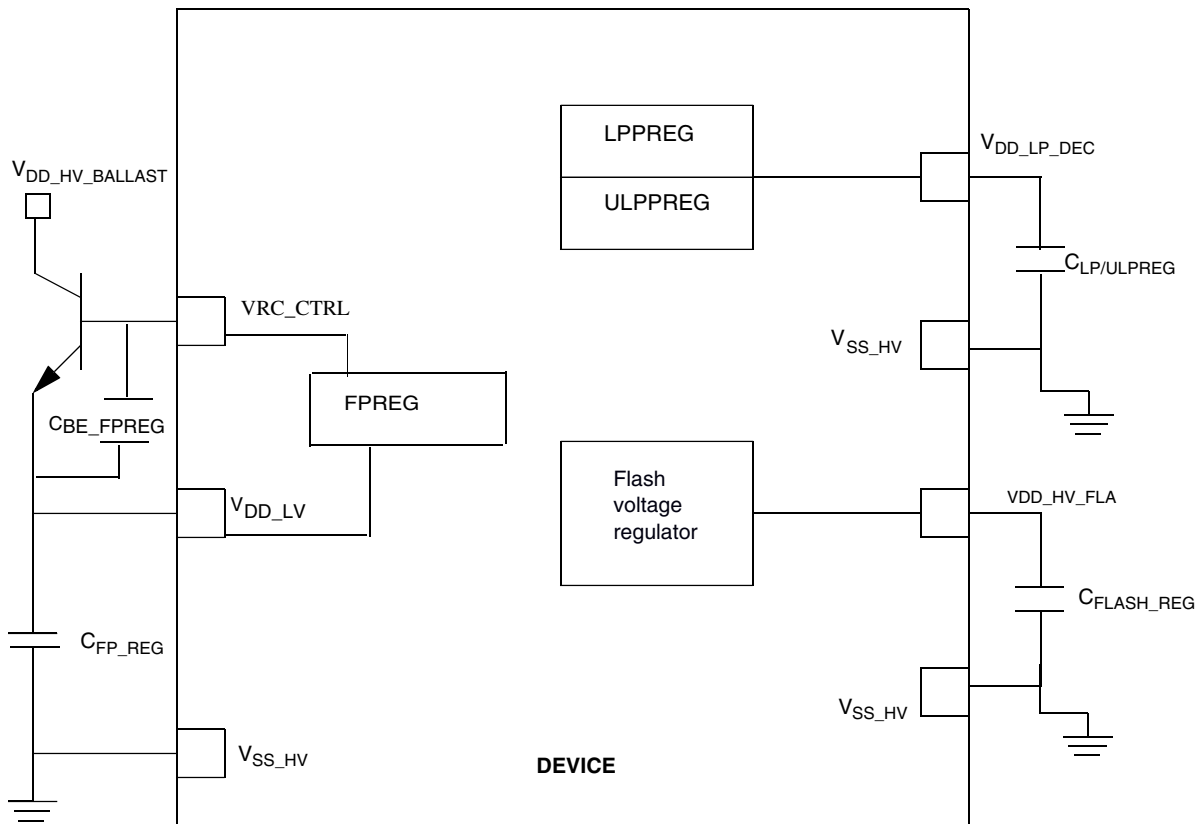


Figure 2. Voltage regulator capacitance connection

NOTE

On BGA, VSS_LV and VSS_HV have been joined on substrate and renamed as VSS.

Table 8. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _{fp_reg} ¹	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2 ²	3	μF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
C _{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	μF
	Combined ESR of external capacitor	—	0.001	—	0.1	Ohm
C _{be_fpreg} ³	Capacitor in parallel to base-emitter	BCP68 and BCP56		3.3		nF
		MJD31		4.7		

Table continues on the next page...

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
I _{DD_BODY_2} 6	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies ⁴ T _a = 125°C ⁵ V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	—	246	mA
		T _a = 105°C	—	—	235	mA
		T _a = 85°C	—	—	210	mA
I _{DD_BODY_3} 7	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies ⁴ T _a = 125 °C ⁵ V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	181	mA
		T _a = 105 °C	—	—	176	mA
		T _a = 85°C	—	—	171	mA
I _{DD_BODY_4} ⁸	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies ⁴ T _a = 125 °C ⁵ V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	264	mA
		T _a = 105 °C	—	—	176	mA
		T _a = 85 °C	—	—	171	mA
I _{DD_STOP}	STOP mode Operating current	T _a = 125 °C ⁹ V _{DD_LV} = 1.25 V	—	—	49	mA
		T _a = 105 °C V _{DD_LV} = 1.25 V	—	10.6	—	
		T _a = 85 °C V _{DD_LV} = 1.25 V	—	8.1	—	
		T _a = 25 °C V _{DD_LV} = 1.25 V	—	4.6	—	

Table continues on the next page...

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
$I_{DD_HV_ADC_REF}$ ^{10, 11, 11}	ADC REF Operating current	$T_a = 125\text{ }^\circ\text{C}$ ⁵ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 5.5\text{ V}$	—	200	400	μA
		$T_a = 105\text{ }^\circ\text{C}$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 5.5\text{ V}$	—	200	—	
		$T_a = 85\text{ }^\circ\text{C}$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 5.5\text{ V}$	—	200	—	
		$T_a = 25\text{ }^\circ\text{C}$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 3.6\text{ V}$	—	200	—	
$I_{DD_HV_ADCx}$ ¹¹	ADC HV Operating current	$T_a = 125\text{ }^\circ\text{C}$ ⁵ ADC operating at 80 MHz $V_{DD_HV_ADC} = 5.5\text{ V}$	—	1.2	2	mA
		$T_a = 25\text{ }^\circ\text{C}$ ADC operating at 80 MHz $V_{DD_HV_ADC} = 3.6\text{ V}$	—	1	2	
$I_{DD_HV_FLASH}$ ¹²	Flash Operating current during read access	$T_a = 125\text{ }^\circ\text{C}$ ⁵ 3.3 V supplies 160 MHz frequency	—	40	45	mA
		$T_a = 105\text{ }^\circ\text{C}$ 3.3 V supplies 160 MHz frequency	—	40	45	
		$T_a = 85\text{ }^\circ\text{C}$ 3.3 V supplies 160 MHz frequency	—	40	45	

- The content of the Conditions column identifies the components that draw the specific current.
- Single e200Z4 core cache disabled @80 MHz, no FlexRay, no ENET, 2 x CAN, 8 LINFlexD, 2 SPI, ADC0 and 1 used constantly, no HSM, Memory: 2M flash, 128K RAM RUN mode, Clocks: FIRC on, XOSC, PLL on, SIRC on for TOD, no 32KHz crystal (TOD runs off SIRC).
- Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C. In case of internal ballast mode, it is expected that the external ballast is not mounted and BAL_SELECT_INT pin is tied to VDD_HV_A supply on board. Internal ballast can be used for all use cases with current consumption upto 150mA
- The power consumption does not consider the dynamic current of I/Os
- $T_j=150^\circ\text{C}$. Assumes $T_a=125^\circ\text{C}$
 - Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#)
- e200Z4 core, 160MHz, cache enabled; e200Z2 core , 80MHz, no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 256K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
- e200Z4 core, 120MHz, cache enabled; e200Z2 core, 60MHz; no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 128K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal

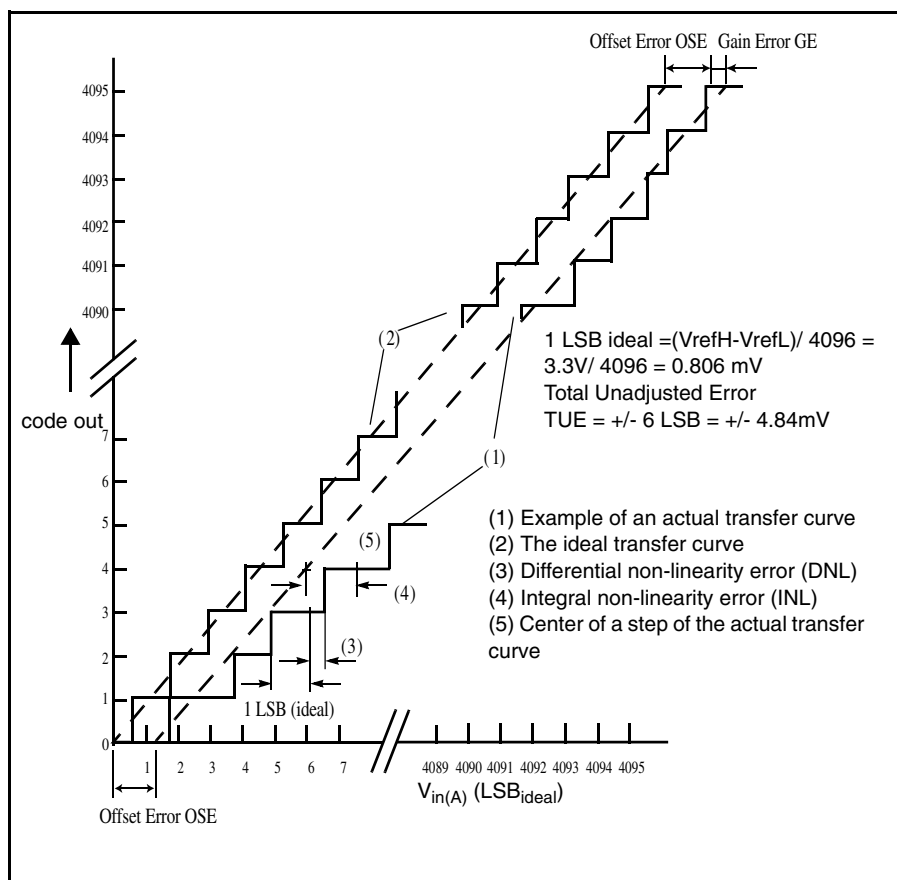


Figure 5. ADC characteristics and error definitions

Table 21. ADC conversion characteristics (for 10-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
t_{conv}	Conversion time ⁴	80 MHz	550	—	—	ns
t_{total_conv}	Total Conversion time $t_{sample} + t_{conv}$ (for standard channels)	80 MHz	1	—	—	μ s
	Total Conversion time $t_{sample} + t_{conv}$ (for extended channels)		1.5	—	—	
C_S ⁵	ADC input sampling capacitance	—	—	3	5	pF
C_{P1} ⁵	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2} ⁵	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1} ⁵	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	k Ω
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD} ⁵	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	-2	—	2	LSB
DNL	Differential non-linearity	—	-1	—	1	LSB
OFS	Offset error	—	-4	—	4	LSB
GNE	Gain error	—	-4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max positive/negative injection		-5	—	5	mA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
$TUE_{standard/extended}$ channels	Total unadjusted error for standard channels	Without current injection	-4	+/-3	4	LSB
		With current injection ⁶		+/-4		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	μ s

1. Active ADC Input, $V_{inA} < [\min(\text{ADC_ADV}, \text{IO_Supply_A,B,C})]$. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO_supply_A, B, C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See [Figure 65](#)
6. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

6.1.2 Analog Comparator (CMP) electrical specifications

Table 22. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	μA
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	μA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1_CMP_REF}$	V
V_{AIO}	Analog input offset voltage ^{1, 1}	-47	—	47	mV
V_H	Analog comparator hysteresis ^{2, 2} <ul style="list-style-type: none"> • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11 	—	1	25	mV
		—	20	50	mV
		—	40	70	mV
		—	60	105	mV
		—	—	—	—
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) ^{1, 3, 3}	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) ^{1, 3}	—	5	21	μs
	Analog comparator initialization delay, High speed mode ^{4, 4}	—	4		μs
	Analog comparator initialization delay, Low speed mode ⁴	—	100		μs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	μA
	5V Reference Voltage	—	10	16	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ⁵
DNL	6-bit DAC differential non-linearity	-0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD_HV_A}-0.6\text{V}$
3. Full swing = V_{IH} , V_{IL}
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

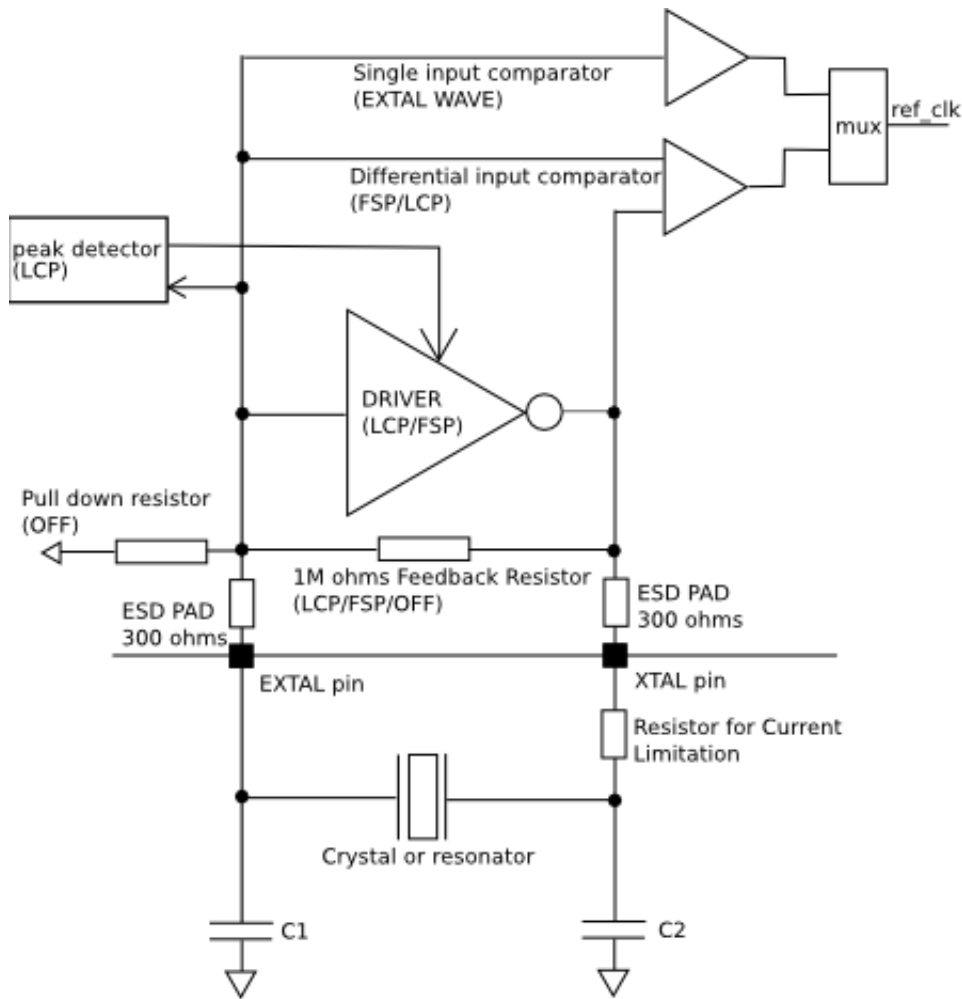


Figure 7. Oscillator connections scheme

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	LCP			23		mA/V
		FSP			33		
V_{XOSCHS}	Oscillation Amplitude	LCP ^{1, 2, 1, 2}	8 MHz		1.0		V_{PP}
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP ¹	8 MHz		2		ms
			16 MHz		1		
			40 MHz		0.5		

Table continues on the next page...

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

6.2.4 128 KHz Internal RC oscillator Electrical specifications**Table 26. 128 KHz Internal RC oscillator electrical specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{oscu}^1	Oscillator frequency	Calibrated	119	128	136.5	KHz
	Temperature dependence				600	ppm/C
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	μA
		Clock stopped			200	nA

1. Vdd=1.2 V, 1.32V, T_a=-40 C, 125 C

6.2.5 PLL electrical specifications**Table 27. PLL electrical specifications**

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 28	ps	NON SSCG mode
TIE			See Table 28		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	μs	Calibration mode

Table 28. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN}^1	Jitter due to Fractional Mode (ps) J_{SDM}^2	Jitter due to Fractional Mode J_{SSCG}^3 (ps)	1 Sigma Random Jitter J_{RJ}^4 (ps)	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	+/- ($J_{\text{SN}} + J_{\text{SDM}} + J_{\text{SSCG}} + N^{[4]} \times J_{\text{RJ}}$)

Table continues on the next page...

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	μ s
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	μ s

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 34. Flash Read Wait State and Address Pipeline Control Combinations

Flash frequency	RWSC setting	APC setting
0 MHz < fFlash <= 33 MHz	0	0
33 MHz < fFlash <= 100 MHz	2	1
100 MHz < fFlash <= 133 MHz	3	1
133 MHz < fFlash <= 160 MHz	4	1

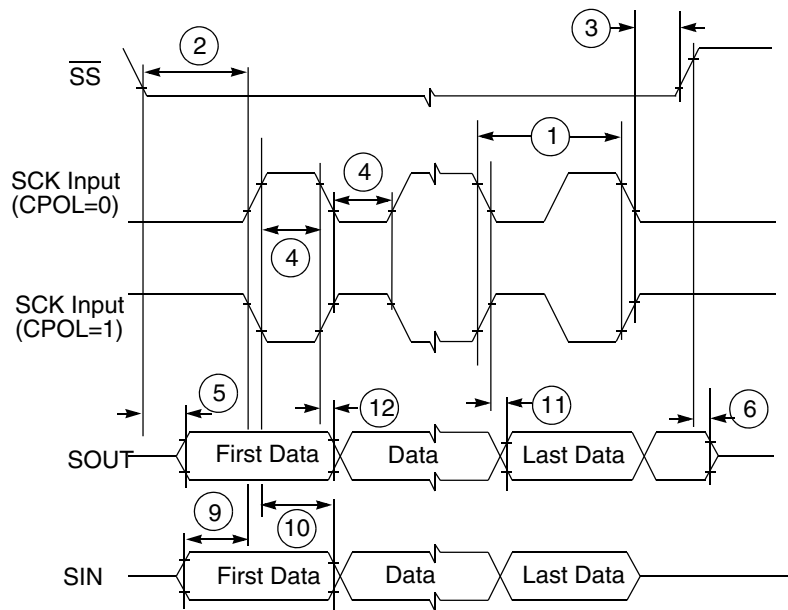


Figure 10. DSPI classic SPI timing — slave, CPHA = 0

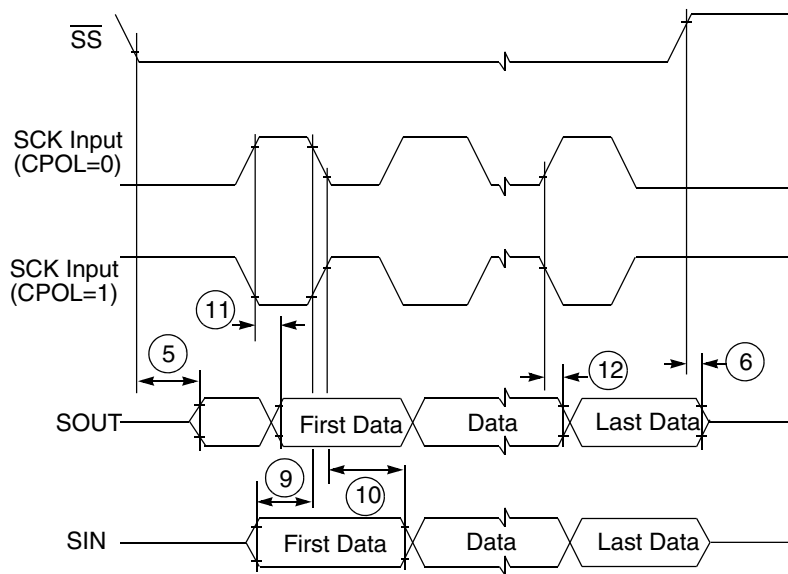


Figure 11. DSPI classic SPI timing — slave, CPHA = 1

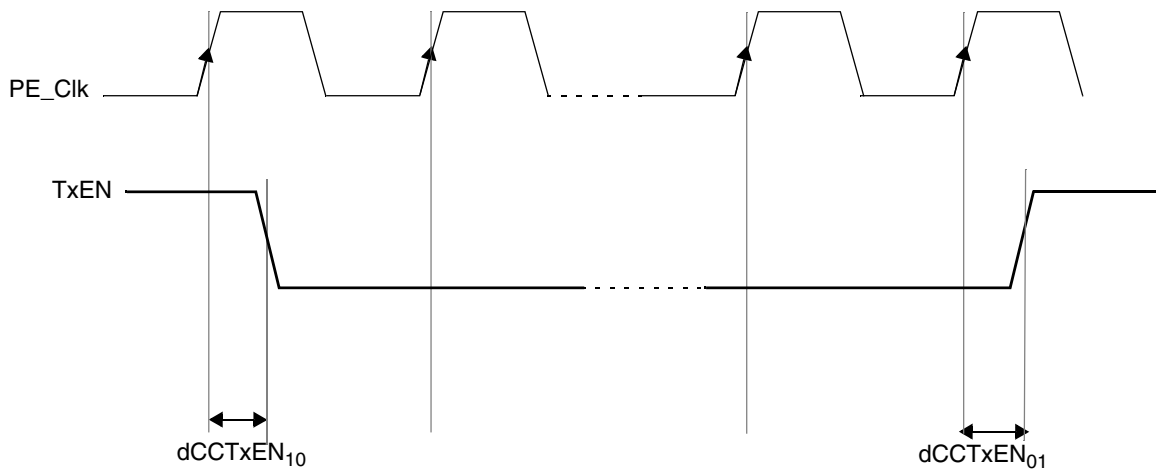


Figure 18. TxEN signal propagation delays

6.4.2.3 TxD

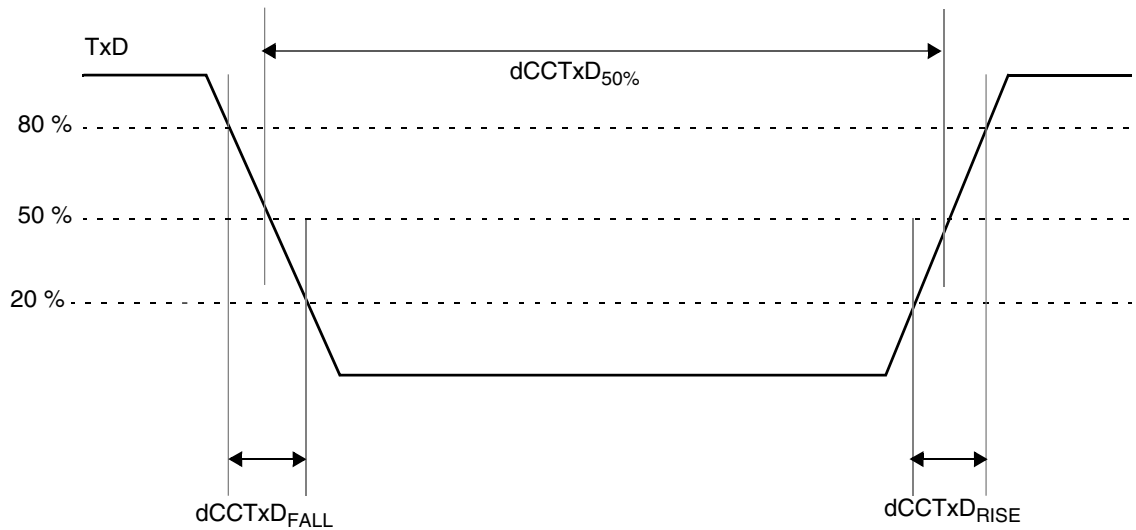


Figure 19. TxD Signal

Table 39. TxD output characteristics

Name	Description ¹	Min	Max	Unit
dCCT _x Asym	Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns)	-2.45	2.45	ns
dCCTxD _{RISE25} +dCCTxD _{FALL25}	Sum of Rise and Fall time of TxD signal at the output	—	9 ²	ns

Table continues on the next page...

Table 44. Slave mode SAI Timing (continued)

No	Parameter	Value		Unit
		Min	Max	
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

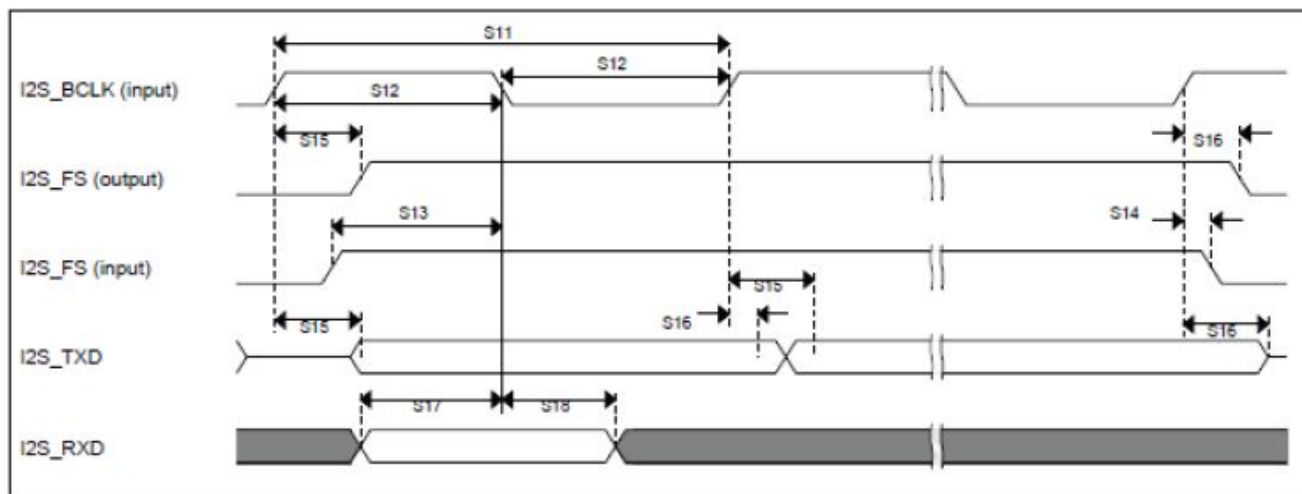


Figure 24. Slave mode SAI Timing

6.5 Debug specifications

6.5.1 JTAG interface timing

Table 45. JTAG pin AC electrical characteristics ¹

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time ^{2, 2}	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20 ^{3, 3}	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600 ^{4, 4}	ns

Table continues on the next page...

Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	17.8	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.9	°C/W	44
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.4	°C/W	55
—	Ψ_{JT}	Thermal resistance, junction to package top	0.5	°C/W	66
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom	0.3	°C/W	77

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- Per JEDEC JESD51-6 with the board horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	31.0	°C/W	11, 22
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	24.3	°C/W	1,2,33
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	23.5	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	20.1	°C/W	1,3

Table continues on the next page...

Thermal attributes

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
—	$R_{\theta JC}$	Thermal resistance, junction to case	7.9	°C/W	55
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	66
—	$R_{\theta JB_CSB}$	Thermal characterization parameter, junction to package bottom outside center (natural convection)	9.0	°C/W	77

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- Per JEDEC JESD51-6 with the board horizontal
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
- Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	100 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50.9	°C/W	1, 21,2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	27.0	°C/W	1,2,33
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	38.0	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	22.2	°C/W	1,3

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev 4	9 March 2016	<ul style="list-style-type: none"> In section, Voltage regulator electrical characteristics <ul style="list-style-type: none"> In table, Voltage regulator electrical specifications: <ul style="list-style-type: none"> Updated the footnote on V_{DD_HV_BALLAST}
Rev 5	27 February 2017	<ul style="list-style-type: none"> In Family Comparison section: <ul style="list-style-type: none"> Updated the "MPC5746C Family Comparison" table. added "NVM Memory Map 1", "NVM Memory Map 2", and "RAM Memory Map" tables. Updated the product version, flash memory size and optional fields information in Ordering Information section. In Recommended Operating Conditions section, removed the note related to additional crossover current. VDD_HV_C row added in "Voltage regulator electrical specifications" table in Voltage regulator electrical characteristics section. In Voltage Monitor Electrical Characteristics section, updated the "Trimmed" Fall and Rise specs of VHVD_LV_cold parameter in "Voltage Monitor Electrical Characteristics" table. In AC Electrical Specifications: 3.3 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. In DC Electrical Specifications: 3.3 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" and updated "Vol min and max" values in the table. In AC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. In DC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" and updated "Vol min and max" values in the table. In "Flash memory AC timing specifications" table in Flash memory AC timing specifications section: <ul style="list-style-type: none"> Updated the "t_{psus}" typ value from 7 us to 9.4 us. Updated the "t_{psus}" max value from 9.1 us to 11.5 us. Added "Continuous SCK Timing" table in DSPI timing section. Added "ADC pad leakage" at 105°C TA conditions in "ADC conversion characteristics (for 12-bit)" table in ADC electrical specifications section. In "STANDBY Current consumption characteristics" table in Supply current characteristics section: <ul style="list-style-type: none"> Updated the Typ and max values of IDD Standby current. Added IDD Standby3 current spec for FIRC ON. Removed IVDDHV and IVDDLv specs in 16 MHz RC Oscillator electrical specifications section. Added Reset Sequence section, with Reset Sequence Duration, BAF execution duration section, and Reset Sequence Distribution as its sub-sections.

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev 5.1	22 May 2017	<ul style="list-style-type: none"> • Removed the Introduction section from Section 4 "General". • In AC Specifications@3.3V section, removed note related to Cz results and added two notes. • In AC Specifications@5V section, added two notes. • In ADC Electrical Specifications section, added spec value of "ADC Analog Pad" at Max leakage (standard channel)@ 105 C T_A in "ADC conversion characteristics (for 10-bit)" table. • In PLL Electrical Specifications section, updated the first footnote of "Jitter calculation" table. • In Analog Comparator Electrical Specifications section, updated the TDLS (propagation delay, low power mode) max value in "Comparator and 6-bit DAC electrical specifications" table to 21 us. • In Recommended Operating Conditions section, updated the footnote link to T_A in "Recommended operating conditions (V DD_HV_x = 5V)" table.