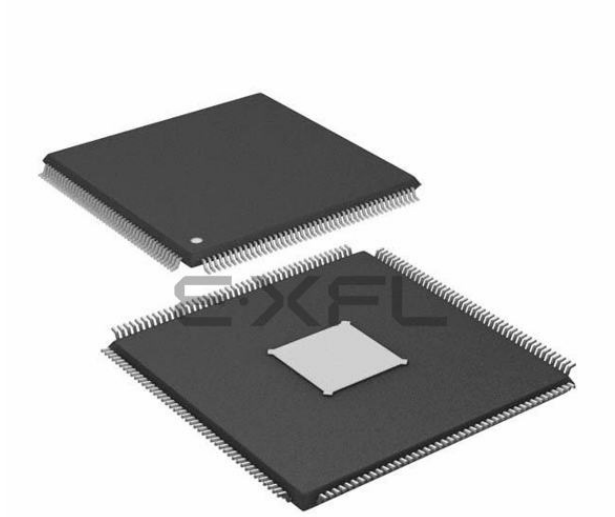

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z2, e200z4 |
| Core Size | 32-Bit Dual-Core |
| Speed | 80MHz/160MHz |
| Connectivity | CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG |
| Peripherals | DMA, LVD, POR, WDT |
| Number of I/O | 129 |
| Program Memory Size | 3MB (3M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 80x10b, 64x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP Exposed Pad |
| Supplier Device Package | 176-LQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746chk0amku6 |

- Debug functionality
  - e200z2 core:NDI per IEEE-ISTO 5001-2008 Class3+
  - e200z4 core: NDI per IEEE-ISTO 5001-2008 Class 3+

- Timer
  - 16 Periodic Interrupt Timers (PITs)
  - Two System Timer Modules (STM)
  - Three Software Watchdog Timers (SWT)
  - 64 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels

- Device/board boundary Scan testing supported with Joint Test Action Group (JTAG) of IEEE 1149.1 and IEEE 1149.7 (CJTAG)

- Security
  - Hardware Security Module (HSMv2)
  - Password and Device Security (PASS) supporting advanced censorship and life-cycle management
  - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts

- Functional Safety
  - ISO26262 ASIL-B compliance

- Multiple operating modes
  - Includes enhanced low power operation

## 4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

**NOTE**

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

**Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)**

| Symbol | Parameter | Conditions[1] | Min[2] | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD\_HV\_A}$<br>$V_{DD\_HV\_B}$<br>$V_{DD\_HV\_C}$ | HV IO supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_FLA}$[3] | HV flash supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_ADC1\_REF}$ | HV ADC1 high reference voltage | — | 3.0 | 5.5 | V |
| $V_{DD\_HV\_ADC0}$<br>$V_{DD\_HV\_ADC1}$ | HV ADC supply voltage | — | max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05 | 3.6 | V |
| $V_{SS\_HV\_ADC0}$<br>$V_{SS\_HV\_ADC1}$ | HV ADC supply ground | — | -0.1 | 0.1 | V |
| $V_{DD\_LV}$[4, 5] | Core supply voltage | — | 1.2 | 1.32 | V |
| $V_{IN1\_CMP\_REF}$[6, 7] | Analog Comparator DAC reference voltage | — | 3.15 | 3.6 | V |
| $I_{INJPAD}$ | Injected input current on any pin during overload condition | — | -3.0 | 3.0 | mA |

*Table continues on the next page...*

4. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. VIN1_CMP_REF ≤ VDD_HV_A
6. This supply is shorted VDD_HV_A on lower packages.
7. $T_J$=150°C. Assumes $T_A$=125°C
    - Assumes maximum θJA of 2s2p board. See Thermal attributes

## 4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
    - Control of external NPN ballast transistor
    - Generating core supply using internal ballast transistor
    - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector (LVD_FLASH) for 3.3 V flash supply (VDD_HV_FLA)
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

1. BCP56, MCP68 and MJD31are guaranteed ballasts.

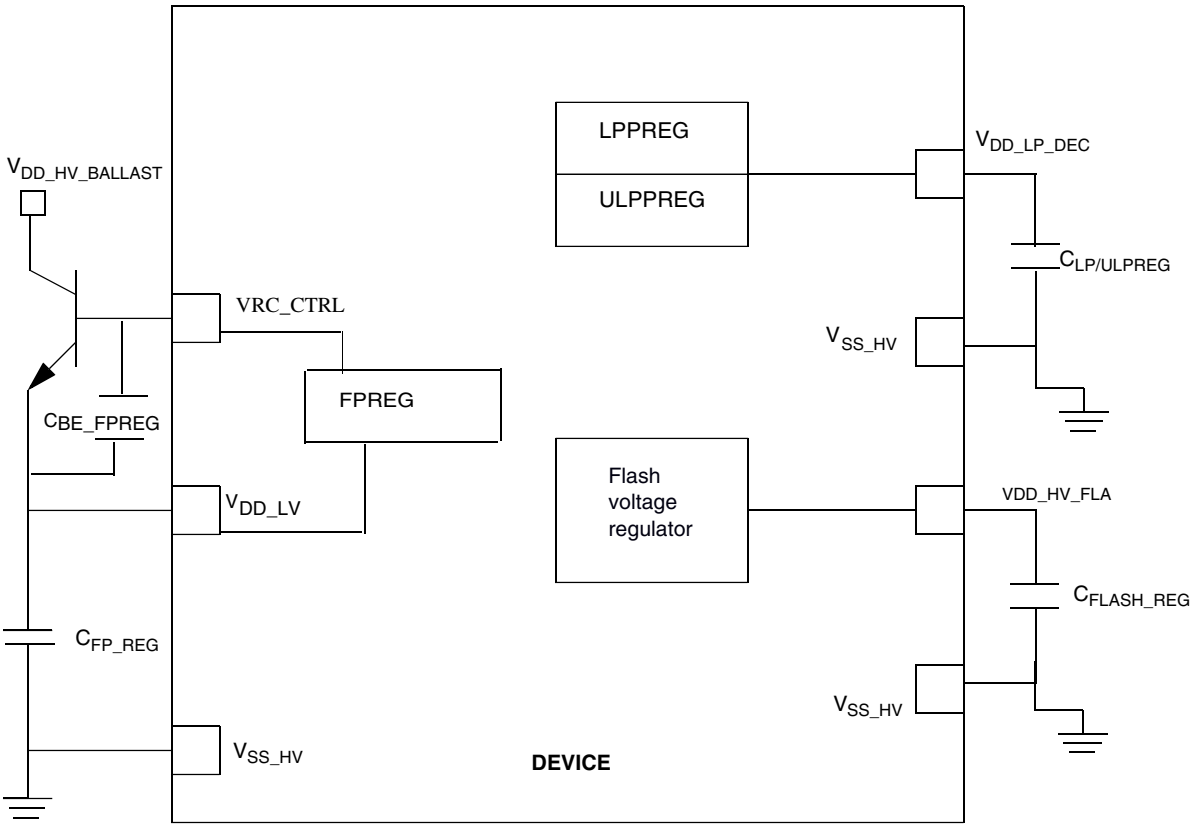



**Figure 2. Voltage regulator capacitance connection**

## NOTE

On BGA, VSS_LV and VSS_HV have been joined on substrate and renamed as VSS.

**Table 8. Voltage regulator electrical specifications**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{fp\_reg}$[1] | External decoupling / stability capacitor | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1.32 | 2.2[2] | 3 | µF |
| | Combined ESR of external capacitor | — | 0.001 | — | 0.03 | Ohm |
| $C_{lp/ulp\_reg}$ | External decoupling / stability capacitor for internal low power regulators | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 0.8 | 1 | 1.4 | µF |
| | Combined ESR of external capacitor | — | 0.001 | — | 0.1 | Ohm |
| $C_{be\_fpreg}$[3] | Capacitor in parallel to base-emitter | BCP68 and BCP56 | | 3.3 | | nF |
| | | MJD31 | | 4.7 | | |

*Table continues on the next page...*

## 4.4 Voltage monitor electrical characteristics

### Table 9. Voltage monitor electrical characteristics

| Symbol | Parameter | State | Conditions | Configuration | | | Threshold | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Power Up [1] | Mask Opt[2, 2] | Reset Type | Min | Typ | Max | V |
| $V_{POR\_LV}$ | LV supply power on reset detector | Fall | Untrimmed | Yes | No | Destructive | 0.930 | 0.979 | 1.028 | V |
| | | | Trimmed | | | | - | - | - | V |
| | | Rise | Untrimmed | | | | 0.980 | 1.029 | 1.078 | V |
| | | | Trimmed | | | | - | - | - | V |
| $V_{HVD\_LV\_cold}$ | LV supply high voltage monitoring, detecting at device pin | Fall | Untrimmed | No | Yes | Functional | Disabled at Start | | | |
| | | | Trimmed | | | | 1.325 | 1.345 | 1.375 | V |
| | | Rise | Untrimmed | | | | Disabled at Start | | | |
| | | | Trimmed | | | | 1.345 | 1.365 | 1.395 | V |
| $V_{LVD\_LV\_PD2\_hot}$ | LV supply low voltage monitoring, detecting on the PD2 core (hot) area | Fall | Untrimmed | Yes | No | Destructive | 1.0800 | 1.1200 | 1.1600 | V |
| | | | Trimmed | | | | 1.1250 | 1.1425 | 1.1600 | V |
| | | Rise | Untrimmed | | | | 1.1000 | 1.1400 | 1.1800 | V |
| | | | Trimmed | | | | 1.1450 | 1.1625 | 1.1800 | V |
| $V_{LVD\_LV\_PD1\_hot\ (BGFP)}$ | LV supply low voltage monitoring, detecting on the PD1 core (hot) area | Fall | Untrimmed | Yes | No | Destructive | 1.0800 | 1.1200 | 1.1600 | V |
| | | | Trimmed | | | | 1.1140 | 1.1370 | 1.1600 | V |
| | | Rise | Untrimmed | | | | 1.1000 | 1.140 | 1.1800 | V |
| | | | Trimmed | | | | 1.1340 | 1.1570 | 1.1800 | V |
| $V_{LVD\_LV\_PD0\_hot\ (BGFP)}$ | LV supply low voltage monitoring, detecting on the PD0 core (hot) area | Fall | Untrimmed | Yes | No | Destructive | 1.0800 | 1.1200 | 1.1600 | V |
| | | | Trimmed | | | | 1.1140 | 1.1370 | 1.1600 | V |
| | | Rise | Untrimmed | | | | 1.1000 | 1.1400 | 1.1800 | V |
| | | | Trimmed | | | | 1.1340 | 1.1570 | 1.1800 | V |
| $V_{POR\_HV}$ | HV supply power on reset detector | Fall | Untrimmed | Yes | No | Destructive | 2.7000 | 2.8500 | 3.0000 | V |
| | | | Trimmed | | | | - | - | - | V |
| | | Rise | Untrimmed | | | | 2.7500 | 2.9000 | 3.0500 | V |
| | | | Trimmed | | | | - | - | - | V |
| $V_{LVD\_IO\_A\_LO}$[3, 3] | HV IO_A supply low voltage monitoring - low range | Fall | Untrimmed | Yes | No | Destructive | 2.7500 | 2.9230 | 3.0950 | V |
| | | | Trimmed | | | | 2.9780 | 3.0390 | 3.1000 | V |
| | | Rise | Untrimmed | | | | 2.7800 | 2.9530 | 3.1250 | V |
| | | | Trimmed | | | | 3.0080 | 3.0690 | 3.1300 | V |
| $V_{LVD\_IO\_A\_HI}$[3] | HV IO_A supply low voltage monitoring - high range | Fall | Trimmed | No | Yes | Destructive | Disabled at Start | | | |
| | | | | | | | 4.0600 | 4.151 | 4.2400 | V |
| | | Rise | Trimmed | | | | Disabled at Start | | | |
| | | | | | | | 4.1150 | 4.2010 | 4.3000 | V |

*Table continues on the next page...*

## Table 10. Current consumption characteristics (continued)

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_HV\_ADC\_REF}$[10, 11, 11] | ADC REF Operating current | $T_a$ = 125 °C[5]<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 5.5 V | — | 200 | 400 | µA |
| | | $T_a$ = 105 °C<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 5.5 V | — | 200 | — | |
| | | $T_a$ = 85 °C<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 5.5 V | — | 200 | — | |
| | | $T_a$ = 25 °C<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 3.6 V | — | 200 | — | |
| $I_{DD\_HV\_ADCx}$[11] | ADC HV Operating current | $T_a$ = 125 °C[5]<br>ADC operating at 80 MHz<br>$V_{DD\_HV\_ADC}$ = 5.5 V | — | 1.2 | 2 | mA |
| | | $T_a$ = 25 °C<br>ADC operating at 80 MHz<br>$V_{DD\_HV\_ADC}$ = 3.6 V | — | 1 | 2 | |
| $I_{DD\_HV\_FLASH}$[12] | Flash Operating current during read access | $T_a$ = 125 °C[5]<br>3.3 V supplies<br>160 MHz frequency | — | 40 | 45 | mA |
| | | $T_a$ = 105 °C<br>3.3 V supplies<br>160 MHz frequency | — | 40 | 45 | |
| | | $T_a$ = 85 °C<br>3.3 V supplies<br>160 MHz frequency | — | 40 | 45 | |

1. The content of the Conditions column identifies the components that draw the specific current.
2. Single e200Z4 core cache disabled @80 MHz, no FlexRay, no ENET, 2 x CAN, 8 LINFlexD, 2 SPI, ADC0 and 1 used constantly, no HSM, Memory: 2M flash, 128K RAM RUN mode, Clocks: FIRC on, XOSC, PLL on, SIRC on for TOD, no 32KHz crystal (TOD runs off SIRC).
3. Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C. In case of internal ballast mode, it is expected that the external ballast is not mounted and BAL_SELECT_INT pin is tied to VDD_HV_A supply on board. Internal ballast can be used for all use cases with current consumption upto 150mA
4. The power consumption does not consider the dynamic current of I/Os
5. Tj=150°C. Assumes Ta=125°C
   - Assumes maximum θJA of 2s2p board. SeeThermal attributes
6. e200Z4 core, 160MHz, cache enabled; e200Z2 core , 80MHz, no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 256K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
7. e200Z4 core, 120MHz, cache enabled; e200Z2 core, 60MHz; no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 128K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal

**Table 17. DC electrical specifications @ 5 V Range (continued)**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Vil (pad_i_hv) | pad_i_hv Input Buffer Low Voltage | VDD_HV_x - 0.3 | 0.45*VDD_HV_x | V |
| Vhys (pad_i_hv) | pad_i_hv Input Buffer Hysteresis | 0.09*VDD_HV_x | | V |
| Vih_hys | CMOS Input Buffer High Voltage (with hysteresis enabled) | 0.65* VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil_hys | CMOS Input Buffer Low Voltage (with hysteresis enabled) | VDD_HV_x - 0.3 | 0.35*VDD_HV_x | V |
| Vih | CMOS Input Buffer High Voltage (with hysteresis disabled) | 0.55 * VDD_HV_x[1, 1] | VDD_HV_x[1] + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage (with hysteresis disabled) | VDD_HV_x - 0.3 | 0.40 * VDD_HV_x[1] | V |
| Vhys | CMOS Input Buffer Hysteresis | 0.09 * VDD_HV_x[1] | | V |
| Pull_IIH (pad_i_hv) | Weak Pullup Current[2, 2] Low | 23 | | µA |
| Pull_IIH (pad_i_hv) | Weak Pullup Current[3, 3] High | | 82 | µA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current[3] Low | 40 | | µA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current[2] High | | 130 | µA |
| Pull_Ioh | Weak Pullup Current[4] | 30 | 80 | µA |
| Pull_Iol | Weak Pulldown Current[5] | 30 | 80 | µA |
| Iinact_d | Digital Pad Input Leakage Current (weak pull inactive) | -2.5 | 2.5 | µA |
| Voh | Output High Voltage[6] | 0.8 * VDD_HV_x[1] | — | V |
| Vol | Output Low Voltage[7]<br>Output Low Voltage[8] | — | 0.2*VDD_HV_x<br>0.1*VDD_HV_x | V |
| Ioh_f | Full drive Ioh[9, 9] (SIUL2_MSCRn.SRC[1:0] = 11) | 18 | 70 | mA |
| Iol_f | Full drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 11) | 21 | 120 | mA |
| Ioh_h | Half drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 10) | 9 | 35 | mA |
| Iol_h | Half drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 10) | 10.5 | 60 | mA |

1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

## 5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

## 6.2 Clocks and PLL interfaces modules

### 6.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

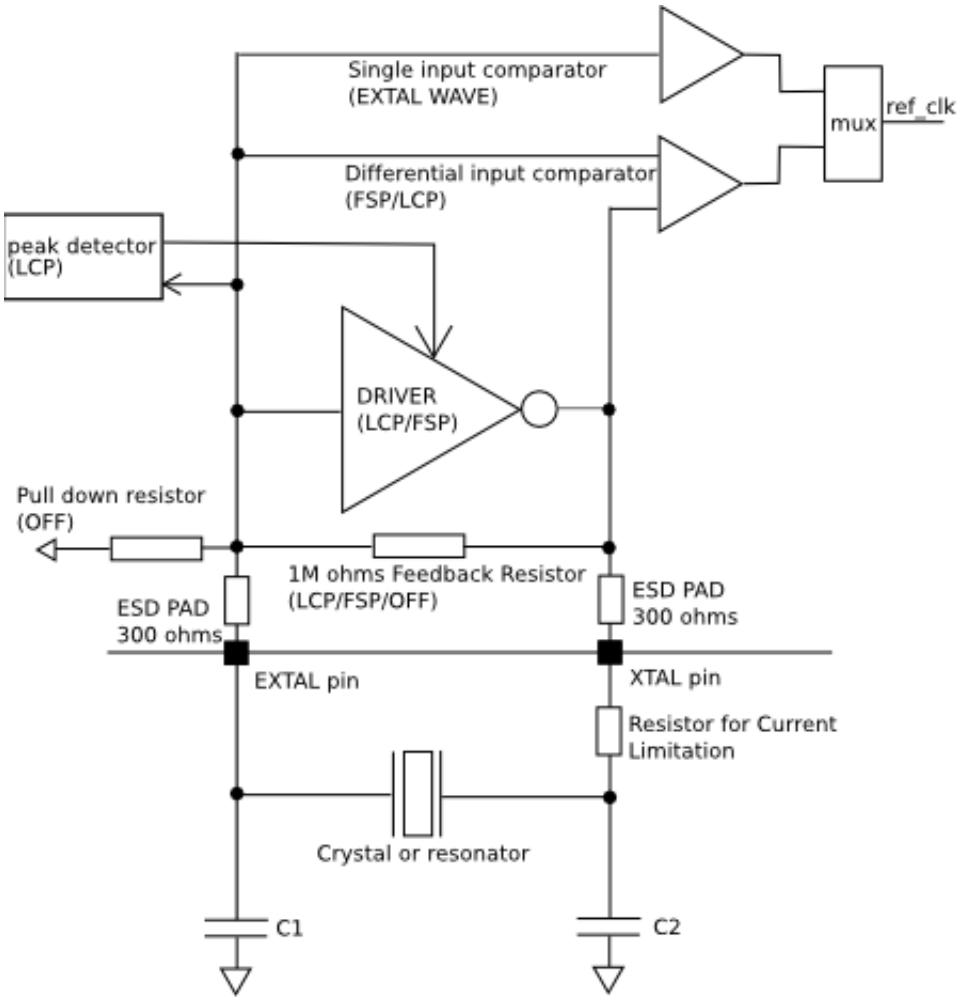
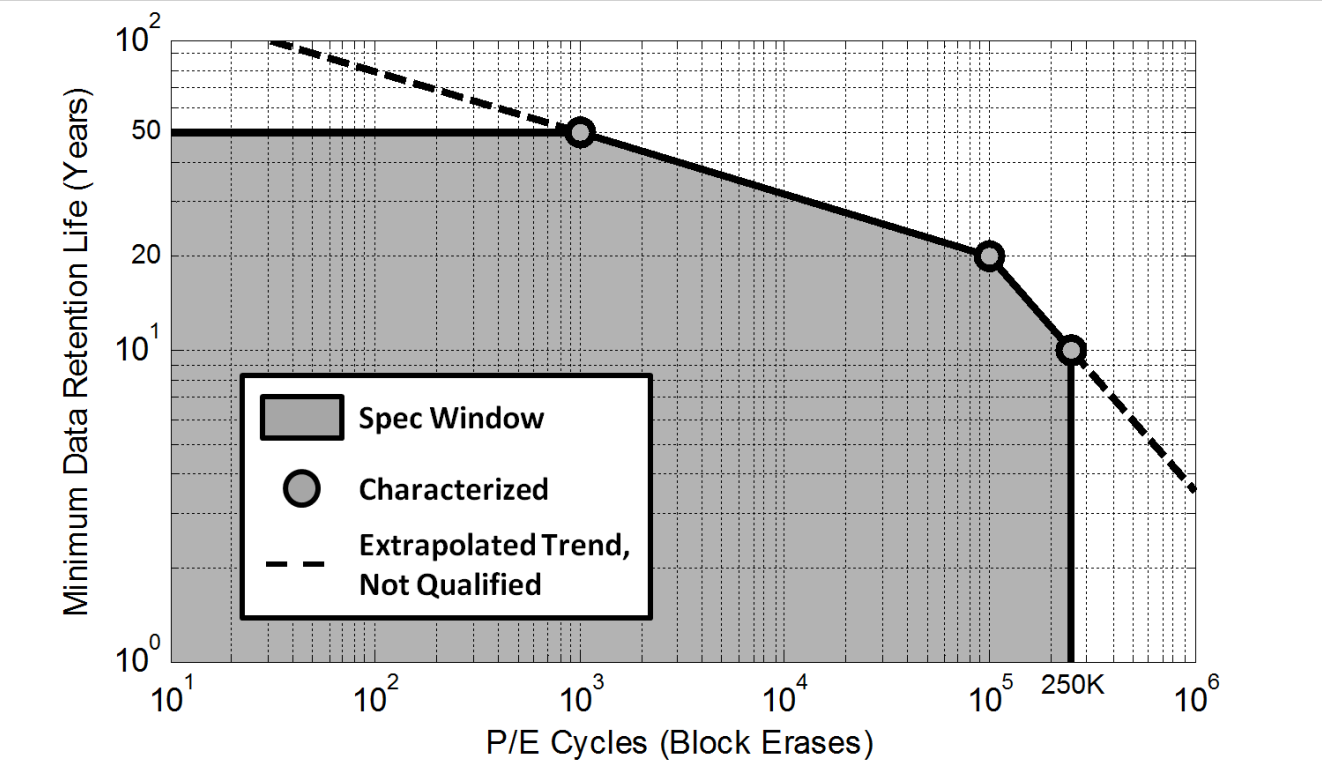



**Figure 7. Oscillator connections scheme**

## Table 23. Main oscillator electrical characteristics

| Symbol | Parameter | Mode | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{XOSCHS}$ | Oscillator frequency | FSP/LCP | | 8 | | 40 | MHz |
| $g_{mXOSCHS}$ | Driver Transconductance | LCP | | | 23 | | mA/V |
| | | FSP | | | 33 | | |
| $V_{XOSCHS}$ | Oscillation Amplitude | LCP[1, 2, 1, 2] | 8 MHz | | 1.0 | | $V_{PP}$ |
| | | | 16 MHz | | 1.0 | | |
| | | | 40 MHz | | 0.8 | | |
| $T_{XOSCHSSU}$ | Startup time | FSP/LCP[1] | 8 MHz | | 2 | | ms |
| | | | 16 MHz | | 1 | | |
| | | | 40 MHz | | 0.5 | | |

*Table continues on the next page...*




## 6.3.5 Flash memory AC timing specifications

**Table 33. Flash memory AC timing specifications**

| Symbol | Characteristic | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| $t_{psus}$ | Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1. | — | 9.4 plus four system clock periods | 11.5 plus four system clock periods | µs |
| $t_{esus}$ | Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1. | — | 16 plus four system clock periods | 20.8 plus four system clock periods | µs |
| $t_{res}$ | Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low. | — | — | 100 | ns |
| $t_{done}$ | Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared. | — | — | 5 | ns |
| $t_{dones}$ | Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1. | — | 16 plus four system clock periods | 20.8 plus four system clock periods | µs |

*Table continues on the next page...*

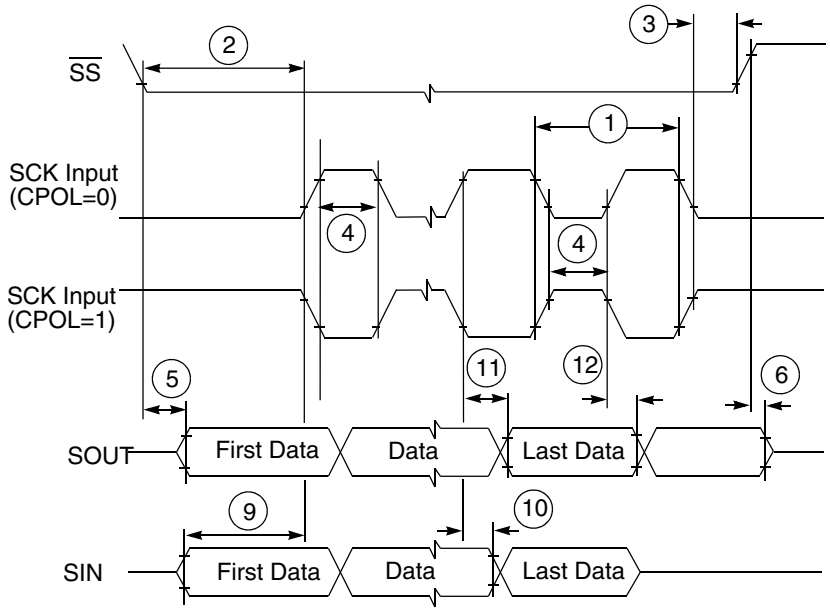



**Figure 14. DSPI modified transfer format timing – slave, CPHA = 0**

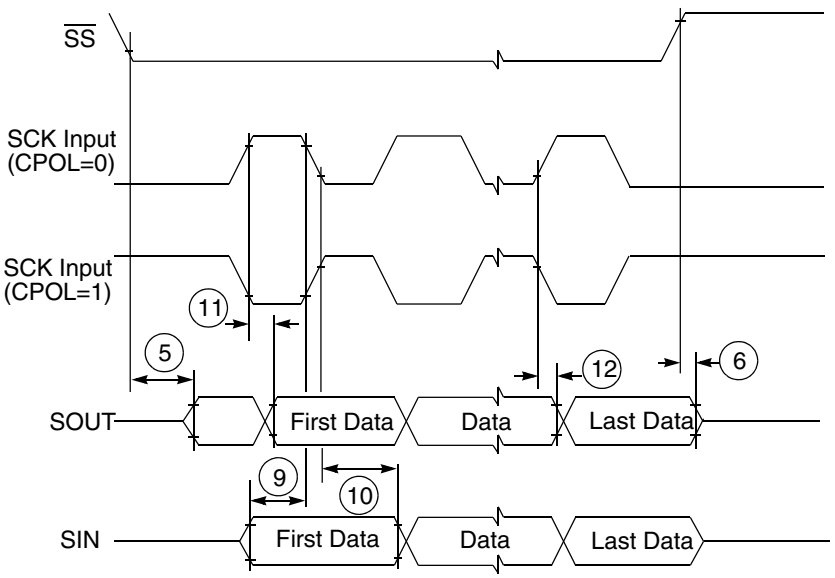



**Figure 15. DSPI modified transfer format timing — slave, CPHA = 1**

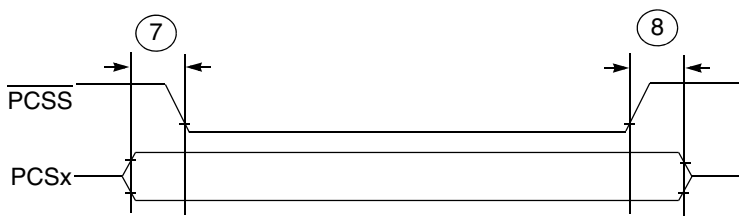



**Figure 16. DSPI PCS strobe (PCSS) timing**

## 6.4.2 FlexRay electrical specifications

### 6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

### 6.4.2.2 TxEN

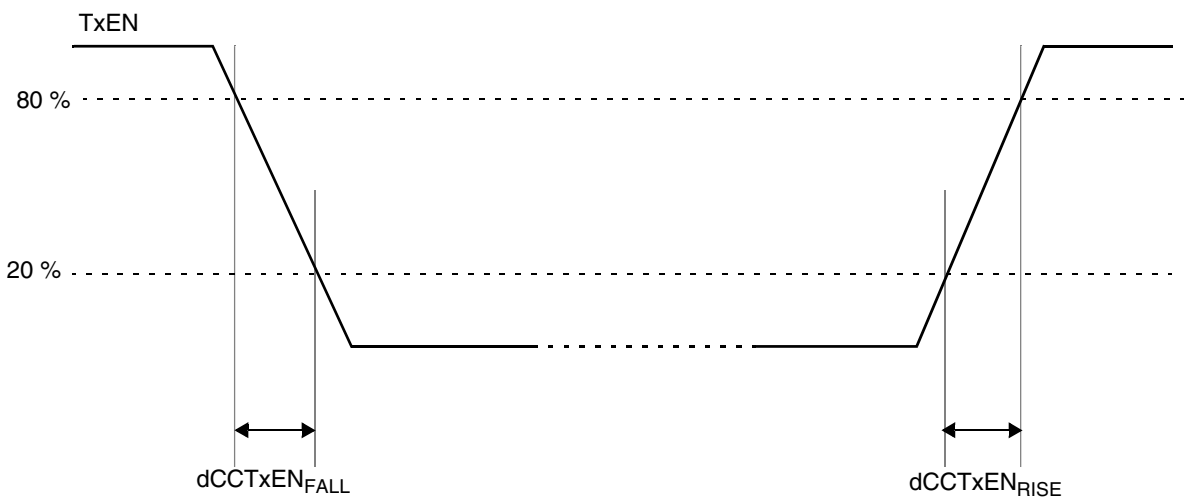



**Figure 17. TxEN signal**

**Table 38. TxEN output characteristics[1]**

| Name | Description | Min | Max | Unit |
|---|---|---|---|---|
| $dCCTxEN_{RISE25}$ | Rise time of TxEN signal at CC | — | 9 | ns |
| $dCCTxEN_{FALL25}$ | Fall time of TxEN signal at CC | — | 9 | ns |
| $dCCTxEN_{01}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | — | 25 | ns |
| $dCCTxEN_{10}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | — | 25 | ns |

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxEN pin load maximum 25 pF

## Table 43. Master mode SAI Timing (continued)

| no | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| S2 | SAI_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | SAI_BCLK cycle time | 80 | - | BCLK period |
| S4 | SAI_BCLK pulse width high/low | 45% | 55% | ns |
| S5 | SAI_BCLK to SAI_FS output valid | - | 15 | ns |
| S6 | SAI_BCLK to SAI_FS output invalid | 0 | - | ns |
| S7 | SAI_BCLK to SAI_TXD valid | - | 15 | ns |
| S8 | SAI_BCLK to SAI_TXD invalid | 0 | - | ns |
| S9 | SAI_RXD/SAI_FS input setup before SAI_BCLK | 28 | - | ns |
| S10 | SAI_RXD/SAI_FS input hold after SAI_BCLK | 0 | - | ns |

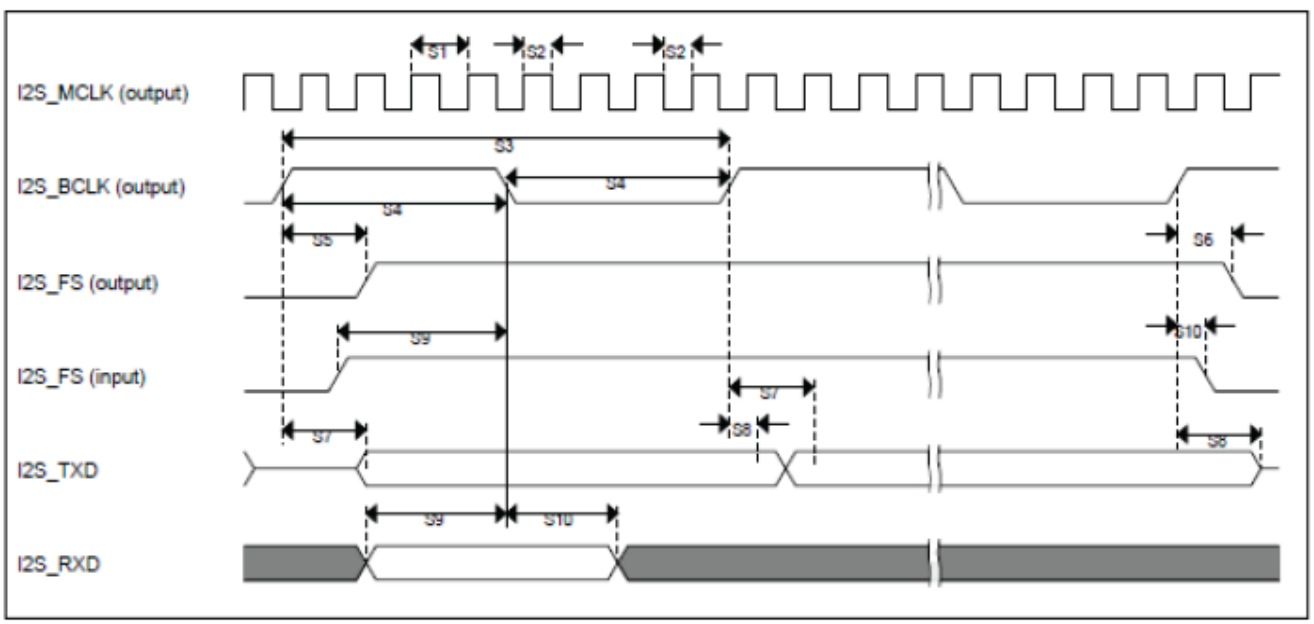



**Figure 23. Master mode SAI Timing**

## Table 44. Slave mode SAI Timing

| No | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| | Operating Voltage | 2.7 | 3.6 | V |
| S11 | SAI_BCLK cycle time (input) | 80 | - | ns |
| S12 | SAI_BCLK pulse width high/low (input) | 45% | 55% | BCLK period |
| S13 | SAI_FS input setup before SAI_BCLK | 10 | - | ns |
| S14 | SAI_FS input hold after SAI_BCLK | 2 | - | ns |

*Table continues on the next page...*

**Table 44. Slave mode SAI Timing (continued)**

| No | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| S15 | SAI_BCLK to SAI_TXD/SAI_FS output valid | - | 28 | ns |
| S16 | SAI_BCLK to SAI_TXD/SAI_FS output invalid | 0 | - | ns |
| S17 | SAI_RXD setup before SAI_BCLK | 10 | - | ns |
| S18 | SAI_RXD hold after SAI_BCLK | 2 | - | ns |

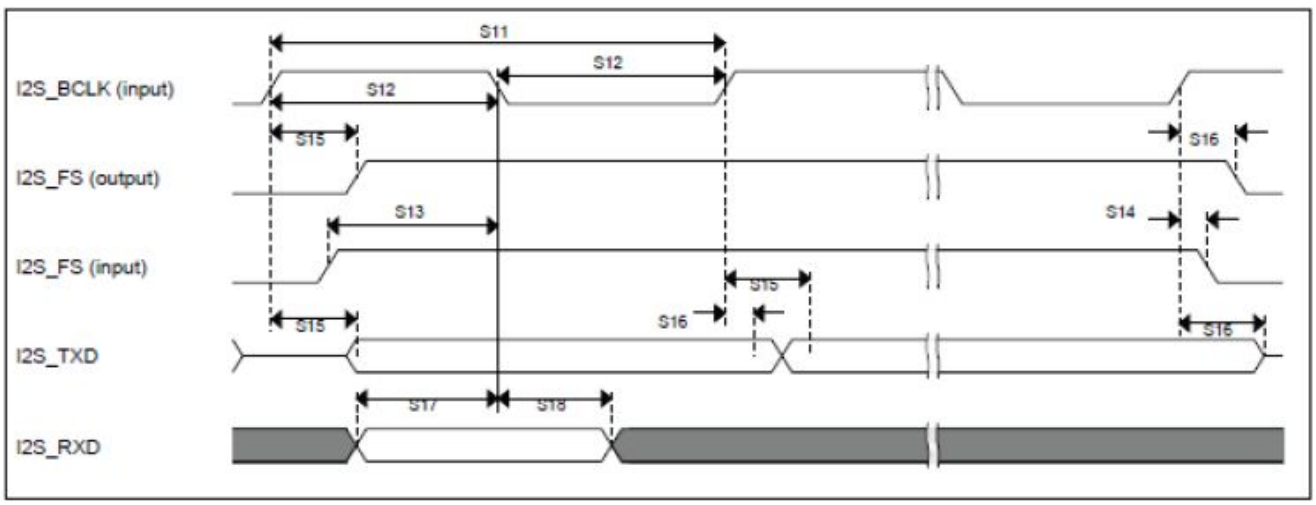



**Figure 24. Slave mode SAI Timing**

# 6.5 Debug specifications

## 6.5.1 JTAG interface timing

**Table 45. JTAG pin AC electrical characteristics [1]**

| # | Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | $t_{JCYC}$ | TCK Cycle Time [2, 2] | 62.5 | — | ns |
| 2 | $t_{JDC}$ | TCK Clock Pulse Width | 40 | 60 | % |
| 3 | $t_{TCKRISE}$ | TCK Rise and Fall Times (40% - 70%) | — | 3 | ns |
| 4 | $t_{TMSS}$, $t_{TDIS}$ | TMS, TDI Data Setup Time | 5 | — | ns |
| 5 | $t_{TMSH}$, $t_{TDIH}$ | TMS, TDI Data Hold Time | 5 | — | ns |
| 6 | $t_{TDOV}$ | TCK Low to TDO Data Valid | — | 20[3, 3] | ns |
| 7 | $t_{TDOI}$ | TCK Low to TDO Data Invalid | 0 | — | ns |
| 8 | $t_{TDOHZ}$ | TCK Low to TDO High Impedance | — | 15 | ns |
| 11 | $t_{BSDV}$ | TCK Falling Edge to Output Valid | — | 600[4, 4] | ns |

*Table continues on the next page...*

## Table 45. JTAG pin AC electrical characteristics [1] (continued)

| # | Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|---|
| 12 | $t_{BSDVZ}$ | TCK Falling Edge to Output Valid out of High Impedance | — | 600 | ns |
| 13 | $t_{BSDHZ}$ | TCK Falling Edge to Output High Impedance | — | 600 | ns |
| 14 | $t_{BSDST}$ | Boundary Scan Input Valid to TCK Rising Edge | 15 | — | ns |
| 15 | $t_{BSDHT}$ | TCK Rising Edge to Boundary Scan Input Invalid | 15 | — | ns |

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

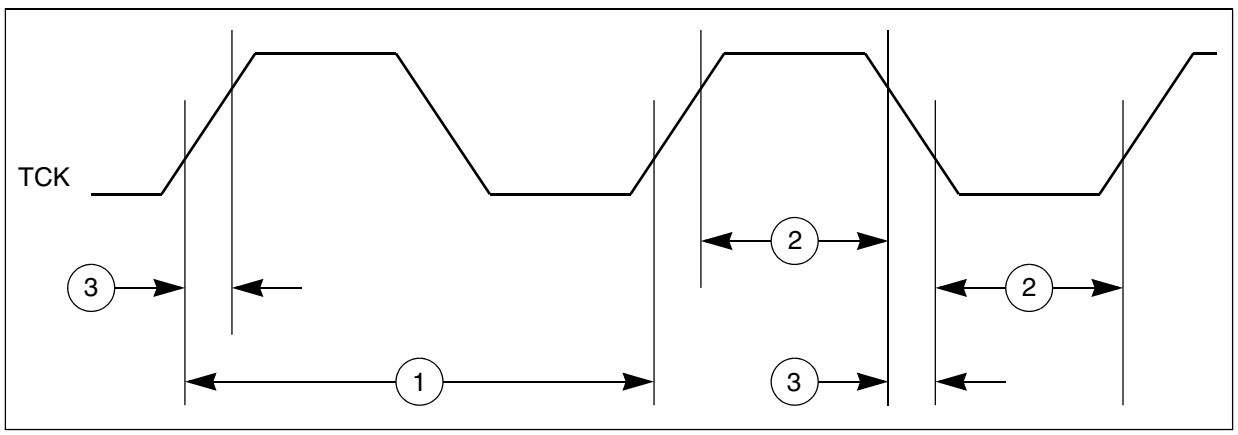



**Figure 25. JTAG test clock input timing**

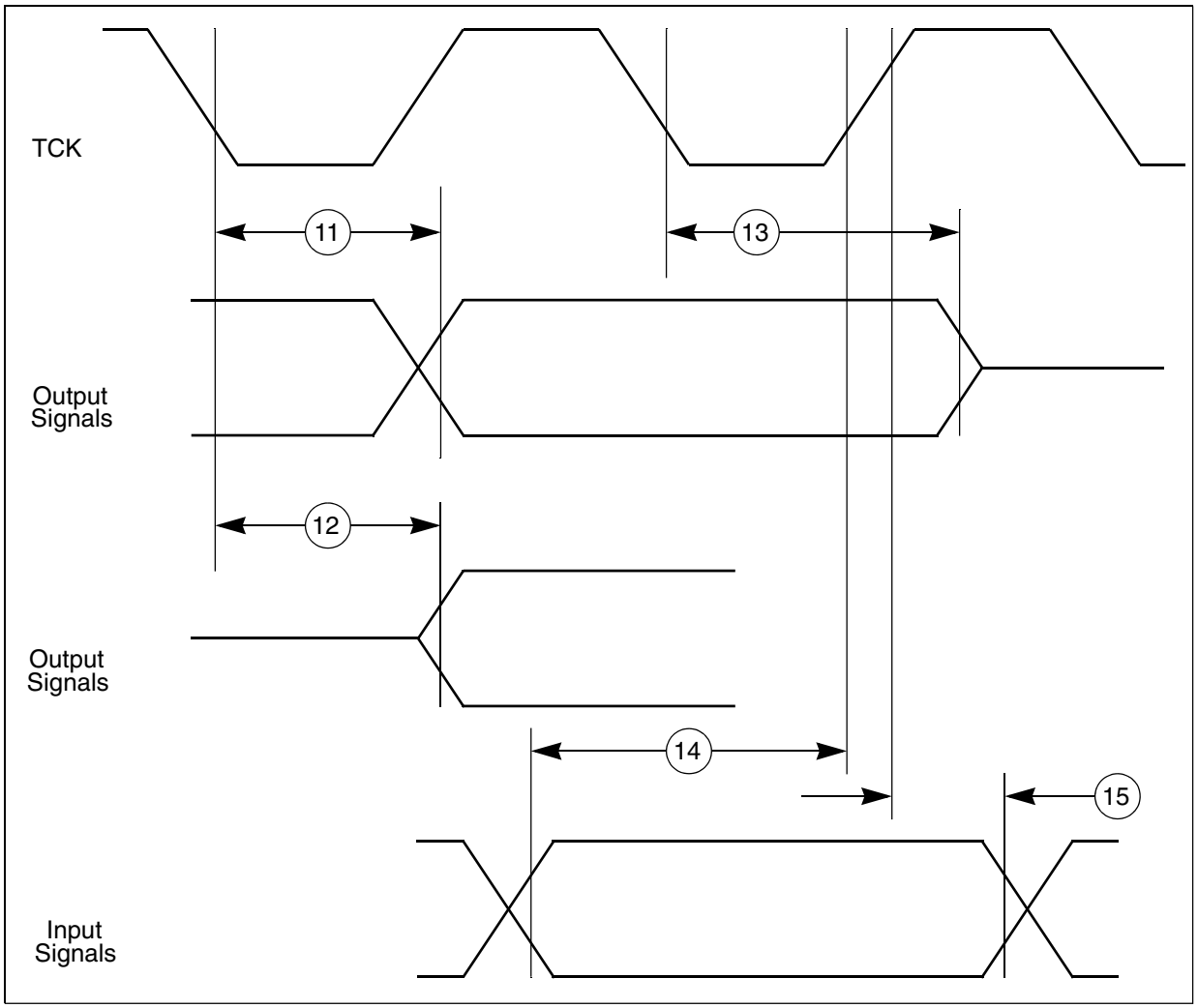



**Figure 27. JTAG boundary scan timing**

## 6.5.2 Nexus timing

### Table 46. Nexus debug port timing [1]

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | $t_{MCYC}$ | MCKO Cycle Time | — | 15.6 | — | ns |
| 2 | $t_{MDC}$ | MCKO Duty Cycle | — | 40 | 60 | % |
| 3 | $t_{MDOV}$ | MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2] | — | –0.1 | 0.25 | tMCYC |
| 4 | $t_{EVTIPW}$ | $\overline{\text{EVTI}}$ Pulse Width | — | 4 | — | tTCYC |
| 5 | $t_{EVTOPW}$ | $\overline{\text{EVTO}}$ Pulse Width | — | 1 | — | tMCYC |
| 6 | $t_{TCYC}$ | TCK Cycle Time[3] | — | 62.5 | — | ns |
| 7 | $t_{TDC}$ | TCK Duty Cycle | — | 40 | 60 | % |
| 8 | $t_{NTDIS}$, $t_{NTMSS}$ | TDI, TMS Data Setup Time | — | 8 | — | ns |

*Table continues on the next page...*

### 6.5.4 External interrupt timing (IRQ pin)

**Table 48. External interrupt timing specifications**

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | $t_{IPWL}$ | IRQ pulse width low | — | 3 | — | $t_{CYC}$ |
| 2 | $t_{IPWH}$ | IRQ pulse width high | — | 3 | — | $t_{CYC}$ |
| 3 | $t_{ICYC}$ | IRQ edge to edge time | — | 6 | — | $t_{CYC}$ |

These values applies when IRQ pins are configured for rising edge or falling edge events, but not both.

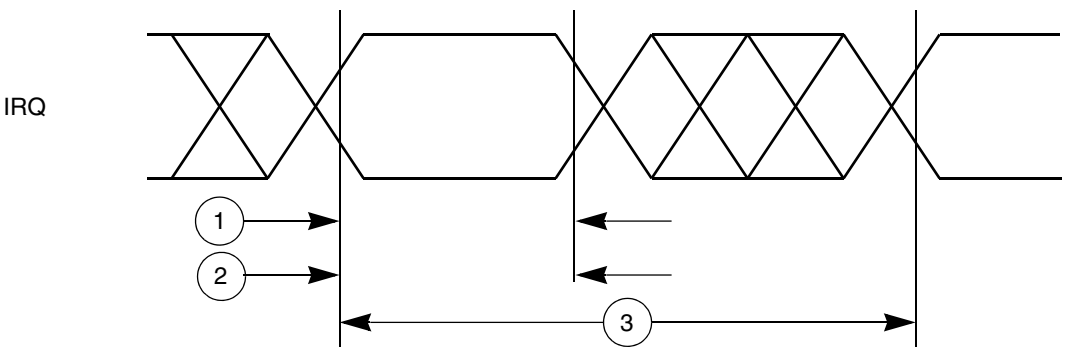



**Figure 31. External interrupt timing**

# 7 Thermal attributes

## 7.1 Thermal attributes

| Board type | Symbol | Description | 176LQFP | Unit | Notes |
|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 50.7 | °C/W | 11, 22 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 24.2 | °C/W | 1, 2, 33 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 38.1 | °C/W | 1, 3 |

*Table continues on the next page...*

| Package | NXP Document Number |
|---|---|
| 176-pin LQFP-EP | 98ASA00698D |
| 256 MAPBGA | 98ASA00346D |
| 324 MAPBGA | 98ASA10582D |

# 9 Pinouts

## 9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

# 10 Reset sequence

## 10.1 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

### 10.1.1 Reset sequence duration

Table 49 specifies the reset sequence duration for the five different reset sequences described in Reset sequence description.

**Table 49. RESET sequences**

| No. | Symbol | Parameter | $T_{Reset}$ | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ [1, 1] | Max | |
| 1 | $T_{DRB}$ | Destructive Reset Sequence, BIST enabled | 6.2 | 7.3 | - | ms |
| 2 | $T_{DR}$ | Destructive Reset Sequence, BIST disabled | 110 | 182 | - | us |
| 3 | $T_{ERLB}$ | External Reset Sequence Long, Unsecure Boot | 6.2 | 7.3 | - | ms |
| 4 | $T_{FRL}$ | Functional Reset Sequence Long, Unsecure Boot | 110 | 182 | - | us |
| 5 | $T_{FRS}$ | Functional Reset Sequence Short, Unsecure Boot | 7 | 9 | - | us |

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

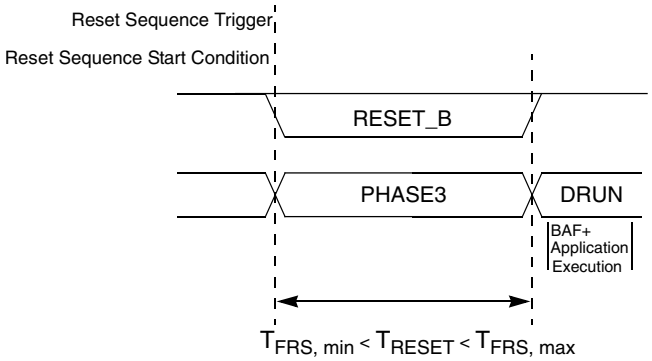



**Figure 36. Functional reset sequence short**

The reset sequences shown in Figure 35 and Figure 36 are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

# 11 Revision History

## 11.1 Revision History

The following table provides a revision history for this document.

**Table 51. Revision History**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| Rev 1 | 14 March 2013 | Initial Release |

*Table continues on the next page...*

## Table 51. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| Rev 5.1 | 22 May 2017 | • Removed the Introduction section from Section 4 "General".<br>• In AC Specifications@3.3V section, removed note related to Cz results and added two notes.<br>• In AC Specifications@5V section, added two notes.<br>• In ADC Electrical Specifications section, added spec value of "ADC Analog Pad" at Max leakage (standard channel)@ 105 C $T_A$ in "ADC conversion characteristics (for 10-bit)" table.<br>• In PLL Electrical Specifications section, updated the first footnote of "Jitter calculation" table.<br>• In Analog Comparator Electrical Specifications section, updated the TDLS (propagation delay, low power mode) max value in "Comparator and 6-bit DAC electrical specifications" table to 21 us.<br>• In Recommended Operating Conditions section, updated the footnote link to $T_A$ in "Recommended operating conditions (V DD_HV_x = 5V)" table. |