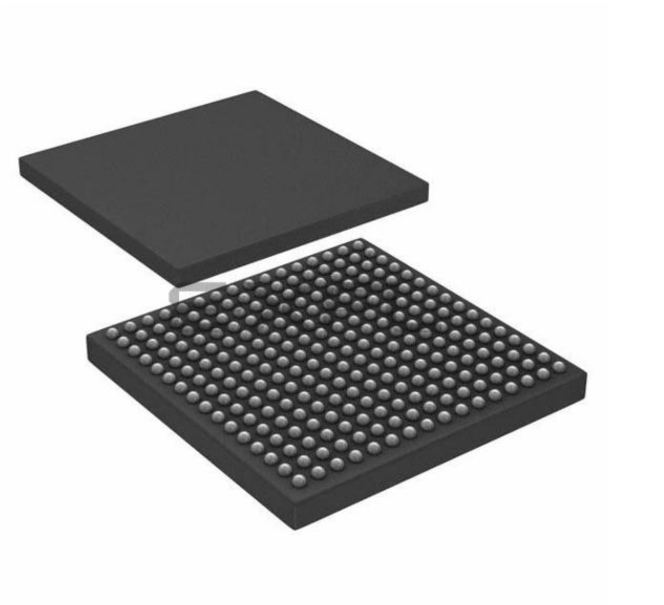

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	178
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746chk1acmj6

- Debug functionality
  - e200z2 core:NDI per IEEE-ISTO 5001-2008 Class3+
  - e200z4 core: NDI per IEEE-ISTO 5001-2008 Class 3+
- Timer
  - 16 Periodic Interrupt Timers (PITs)
  - Two System Timer Modules (STM)
  - Three Software Watchdog Timers (SWT)
  - 64 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels
- Device/board boundary Scan testing supported with Joint Test Action Group (JTAG) of IEEE 1149.1 and IEEE 1149.7 (CJTAG)
- Security
  - Hardware Security Module (HSMv2)
  - Password and Device Security (PASS) supporting advanced censorship and life-cycle management
  - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Functional Safety
  - ISO26262 ASIL-B compliance
- Multiple operating modes
  - Includes enhanced low power operation

Table of Contents

1 Block diagram

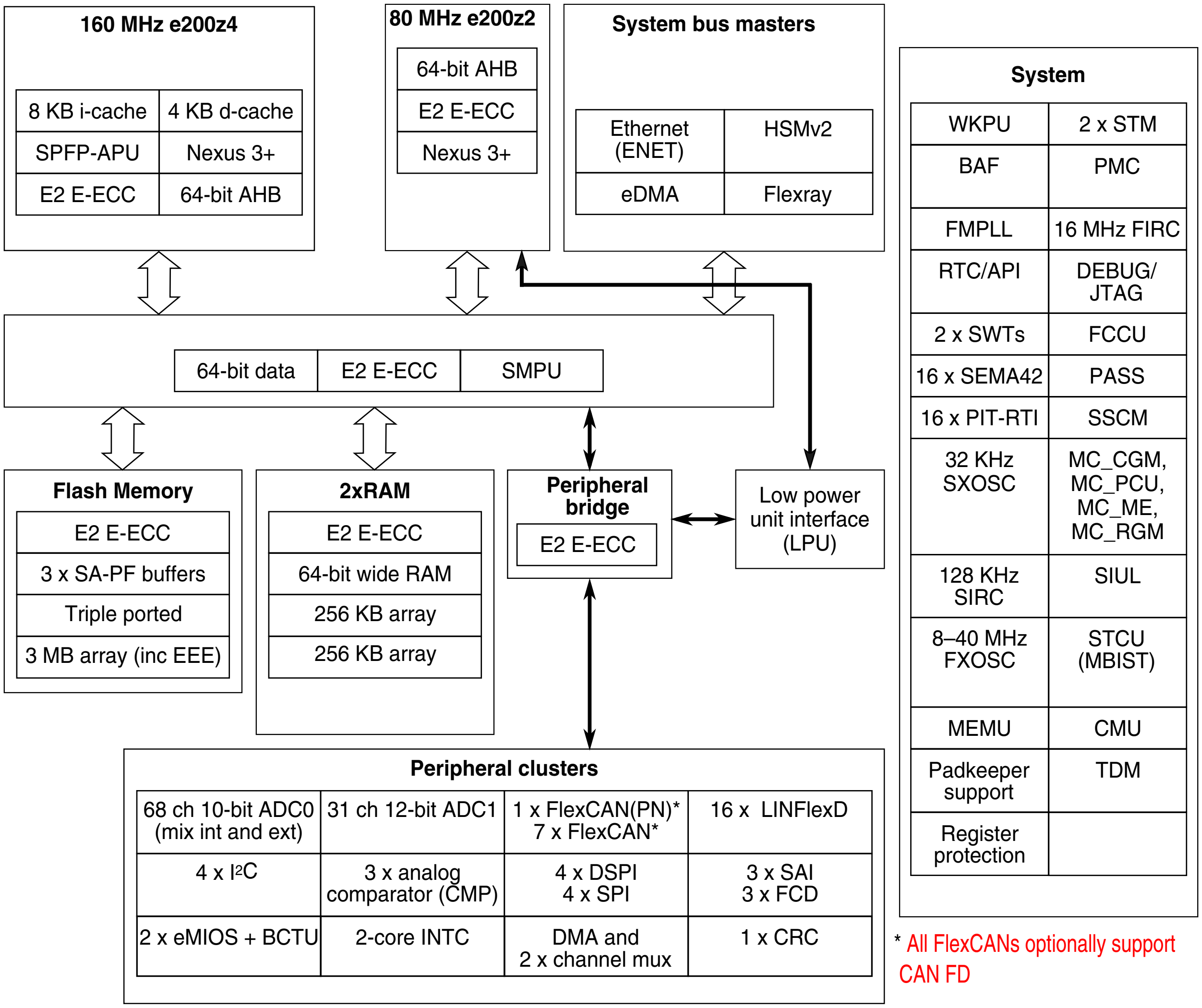

Figure 1. MPC5746C block diagram

2 Family comparison

The following table provides a summary of the different members of the MPC5746C family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest number or address (e.g., FlexCAN0) and end at highest available number or address (e.g., MPC574xB/C have 6 CAN, ending with FlexCAN5).

Table 1. MPC5746C Family Comparison[1]

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C
CPUs	e200z4	e200z4	e200z4	e200z4 e200z2	e200z4 e200z2	e200z4 e200z2
FPU	e200z4	e200z4	e200z4	e200z4	e200z4	e200z4
Maximum Operating Frequency[2]	160MHz (Z4)	160MHz (Z4)	160MHz (Z4)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)
Flash memory	2 MB	1.5 MB	3 MB	1.5 MB	2 MB	3 MB
EEPROM support	Emulated up to 64K			Emulated up to 64K		
RAM	256 KB	192 KB	384 KB (Optional 512KB)[3, 3]	192 KB	256 KB	384 KB (Optional 512KB)[3]
ECC	End to End					
SMPU	16 entry					
DMA	32 channels					
10-bit ADC	36 Standard channels 32 External channels					
12-bit ADC	15 Precision channels 16 Standard channels					
Analog Comparator	3					
BCTU	1					
SWT	1, SWT[0][4]			2[4]		
STM	1, STM[0]			2		
PIT-RTI	16 channels PIT 1 channels RTI					
RTC/API	1					
Total Timer I/O[5]	64 channels 16-bits					
LINFlexD	1 Master and Slave (LINFlexD[0], 11 Master (LINFlexD[1:11])			1 Master and Slave (LINFlexD[0], 15 Master (LINFlexD[1:15])		
FlexCAN	6 with optional CAN FD support (FlexCAN[0:5])			8 with optional CAN FD support (FlexCAN[0:7])		
DSPI/SPI	4 x DSPI 4 x SPI					

Table continues on the next page...

Table 1. MPC5746C Family Comparison[1] (continued)

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C
I²C	4	4	4	4		
SAI/I²S	3	3	3	3		
FXOSC	8 - 40 MHz					
SXOSC	32 KHz					
FIRC	16 MHz					
SIRC	128 KHz					
FMPLL	1					
Low Power Unit (LPU)	Yes					
FlexRay 2.1 (dual channel)	Yes, 128 MB	Yes, 128 MB	Yes, 128 MB	Yes, 128 MB		
Ethernet (RMII, MII + 1588, Muti queue AVB support)	1	1	1	1		
CRC	1					
MEMU	2					
STCU2	1					
HSM-v2 (security)	Optional					
Censorship	Yes					
FCCU	1					
Safety level	Specific functions ASIL-B certifiable					
User MBIST	Yes					
I/O Retention in Standby	Yes					
GPIO[6]	Up to 264 GPI and up to 246 GPIO					
Debug	JTAGC, cJTAG					
Nexus	Z4 N3+ (Only available on 324BGA (development only)) Z2 N3+ (Only available on 324BGA (development only))					
Packages	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA, 324 BGA (development only) 100 BGA

1. Feature set dependent on selected peripheral multiplexing, table shows example. Peripheral availability is package dependent.
2. Based on 125°C ambient operating temperature and subject to full device characterization.
3. Contact NXP representative for part number
4. Additional SWT included when HSM option selected
5. See device datasheet and reference manual for information on to timer channel configuration and functions.
6. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

Table 2. MPC5746C Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW partition	MPC5744	MPC5745	MPC5746
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	not available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	7	not available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	7	not available	not available	available
0x011C0000	0x011FFFFF	256 KB code Flash block 7	7	not available	not available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	not available	not available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	not available	not available	not available

Table 3. MPC5746C Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW partition	MPC5744B MPC5745B MPC5746B	MPC5744C MPC5745C MPC5746C
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	not available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	not available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	not available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	not available	available

Table 4. MPC5746C Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40000000	0x40001FFF	8 KB	SRAM0	available	available	available
0x40002000	0x4000FFFF	56 KB	SRAM1	available	available	available
0x40010000	0x4001FFFF	64 KB	SRAM2	available	available	available
0x40020000	0x4002FFFF	64 KB	SRAM3	available	available	available

Table continues on the next page...

Table 4. MPC5746C Family Comparison - RAM Memory Map (continued)

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40030000	0x4003FFFF	64 KB	SRAM4	not available	available	available
0x40040000	0x4004FFFF	64 KB	SRAM5	not available	not available	available
0x40050000	0x4005FFFF	64 KB	SRAM6	not available	not available	available
0x40060000	0x4006FFFF	64 KB	SRAM7	not available	not available	optional
0x40070000	0x4007FFFF	64 KB	SRAM8	not available	not available	optional

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5746C.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 5. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$[2, 3]	3.3 V - 5. 5V input/output supply voltage	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$[4, 5]	3.3 V flash supply voltage (when supplying from an external source in bypass mode)	—	–0.3	3.63	V
$V_{DD\_LP\_DEC}$[6]	Decoupling pin for low power regulators[7]	—	–0.3	1.32	V
$V_{DD\_HV\_ADC1\_REF}$[8]	3.3 V / 5.0 V ADC1 high reference voltage	—	–0.3	6	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	3.3 V to 5.5V ADC supply voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	3.3V to 5.5V ADC supply ground	—	–0.1	0.1	V
V_{DD_LV}[9, 10, 10, 11, 11, 12]	Core logic supply voltage	—	–0.3	1.32	V
V_{INA}	Voltage on analog pin with respect to ground (V_{SS_HV})	—	–0.3	Min ($V_{DD\_HV\_x}$, $V_{DD\_HV\_ADCx}$, $V_{DD\_ADCx\_REF}$) +0.3	V
V_{IN}	Voltage on any digital pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$	–0.3	$V_{DD\_HV\_x}$ + 0.3	V
I_{INJPAD}	Injected input current on any pin during overload condition	Always	–5	5	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{ramp}	Supply ramp rate	—	0.5 V / min	100V/ms	—
T_A[13]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	–55	165	°C

1. All voltages are referred to VSS_HV unless otherwise specified
2. VDD_HV_B and VDD_HV_C are common together on the 176 LQFP-EP package.
3. Allowed $V_{DD\_HV\_x}$ = 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J= 150 °C, remaining time at or below 5.5 V.
4. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
5. VDD_HV_FLA must be disconnected from ANY power sources when VDD_HV_A = 5V
6. This pin should be decoupled with low ESR 1 µF capacitor.
7. Not available for input voltage, only for decoupling internal regulators
8. 10-bit ADC does not have dedicated reference and its reference is bonded to 10-bit ADC supply(VDD_HV_ADC0) inside the package.
9. Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C, remaining time as defined in footnotes 10 and 11.
10. Allowed 1.38 – 1.45 V– for 10 hours cumulative time at maximum T_J = 150 °C, remaining time as defined in footnote 11.
11. 1.32 – 1.38 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.326 V at maximum T_J = 150 °C.
12. If HVD on core supply ($V_{HVD\_LV\_x}$) is enabled, it will generate a reset when supply goes above threshold.
13. T_J=150°C. Assumes T_A=125°C
    - Assumes maximum θJA for 2s2p board. See Thermal attributes

8. e200Z4 core, 160MHz, cache enabled; e200Z4 core, 80MHz; HSM fully operational (Z0 core @80MHz) FlexRay, 5x CAN, 5x LINFlexD, 2x SPI, 1x ADC used constantly, 1xeMIOS (5 ch), Memory: 3M flash, 384K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
9. Assuming Ta=Tj, as the device is in Stop mode. Assumes maximum θJA of 2s2p board. See Thermal attributes.
10. Internal structures hold the input voltage less than $V_{DD\_HV\_ADC\_REF}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
11. This value is the total current for two ADCs.Each ADC might consume upto 2mA at max.
12. This assumes the default configuration of flash controller register. For more details, refer to Flash memory program and erase specifications

Table 11. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
LPU_RUN	with 256K RAM	T_a = 25 °C SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF	—	10	—	mA
		T_a = 85 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	10.5	—	
		T_a = 105 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	11	—	
		T_a = 125 °C[2, 2] SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	—	26	
LPU_STOP	with 256K RAM	T_a = 25 °C	—	0.18	—	mA
		T_a = 85 °C	—	0.60	—	
		T_a = 105 °C	—	1.00	—	
		T_a = 125 °C [2]	—	—	10.6	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. See Thermal attributes

Table 12. STANDBY Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
STANDBY0	STANDBY with 8K RAM	T_a = 25 °C	—	71	—	μA
		T_a = 85 °C	—	125	700	
		T_a = 105 °C	—	195	1225	
		T_a = 125 °C [2, 2]	—	314	2100	
STANDBY1	STANDBY with 64K RAM	T_a = 25 °C	—	72	—	μA
		T_a = 85 °C	—	140	715	
		T_a = 105 °C	—	225	1275	
		T_a = 125 °C [2]	—	358	2250	

Table continues on the next page...

5.3 AC specifications @ 5 V Range

Table 16. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		4.5/4.5		1.3/1.2	25	11
		6/6		2.5/2	50	
		13/13		9/9	200	
		5.25/5.25		3/2	25	10
		9/8		5/4	50	
		22/22		18/16	200	
		27/27		13/13	50	01[2, 2]
		40/40		24/24	200	
		40/40		24/24	50	00[2]
		65/65		40/40	200	
pad_i_hv/ pad_sr_hv (input)		1.5/1.5		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V

Table continues on the next page...

Table 17. DC electrical specifications @ 5 V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Vil (pad_i_hv)	pad_i_hv Input Buffer Low Voltage	VDD_HV_x - 0.3	0.45*VDD_HV_x	V
Vhys (pad_i_hv)	pad_i_hv Input Buffer Hysteresis	0.09*VDD_HV_x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65* VDD_HV_x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VDD_HV_x - 0.3	0.35*VDD_HV_x	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * VDD_HV_x[1, 1]	VDD_HV_x[1] + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VDD_HV_x - 0.3	0.40 * VDD_HV_x[1]	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x[1]		V
Pull_IIH (pad_i_hv)	Weak Pullup Current[2, 2] Low	23		µA
Pull_IIH (pad_i_hv)	Weak Pullup Current[3, 3] High		82	µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[3] Low	40		µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[2] High		130	µA
Pull_Ioh	Weak Pullup Current[4]	30	80	µA
Pull_Iol	Weak Pulldown Current[5]	30	80	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[6]	0.8 * VDD_HV_x[1]	—	V
Vol	Output Low Voltage[7] Output Low Voltage[8]	—	0.2*VDD_HV_x 0.1*VDD_HV_x	V
Ioh_f	Full drive Ioh[9, 9] (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

Table 20. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
R_{AD}[6]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity (precise channel)	—	–2	—	2	LSB
INL	Integral non-linearity (standard channel)	—	–3	—	3	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (precision channel)	150 °C	—	—	250	nA
	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C $_{TA}$	—	5	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{precision\ channels}$	Total unadjusted error for precision channels	Without current injection	–6	+/-4	6	LSB
		With current injection[7, 7]		+/-5		LSB
$TUE_{standard/extended\ channels}$	Total unadjusted error for standard/ extended channels	Without current injection	–8	+/-6	8	LSB
		With current injection[7]		+/-8		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	μs

1. Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 6.
7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

6.2.4 128 KHz Internal RC oscillator Electrical specifications

Table 26. 128 KHz Internal RC oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{oscu}[1]	Oscillator frequency	Calibrated	119	128	136.5	KHz
	Temperature dependence				600	ppm/C
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	µA
		Clock stopped			200	nA

1. Vdd=1.2 V, 1.32V, T_a=-40 C, 125 C

6.2.5 PLL electrical specifications

Table 27. PLL electrical specifications

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 28	ps	NON SSCG mode
TIE			See Table 28		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	µs	Calibration mode

Table 28. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN}[1]	Jitter due to Fractional Mode (ps) J_{SDM}[2]	Jitter due to Fractional Mode J_{SSCG} (ps) [3]	1 Sigma Random Jitter J_{RJ} (ps) [4]	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	$+/-(J_{SN}+J_{SDM}+J_{SSCG}+N^{[4]} \times J_{RJ})$

Table continues on the next page...

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	μs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	μs

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 34. Flash Read Wait State and Address Pipeline Control Combinations

Flash frequency	RWSC setting	APC setting
0 MHz < fFlash <= 33 MHz	0	0
33 MHz < fFlash <= 100 MHz	2	1
100 MHz < fFlash <= 133 MHz	3	1
133 MHz < fFlash <= 160 MHz	4	1

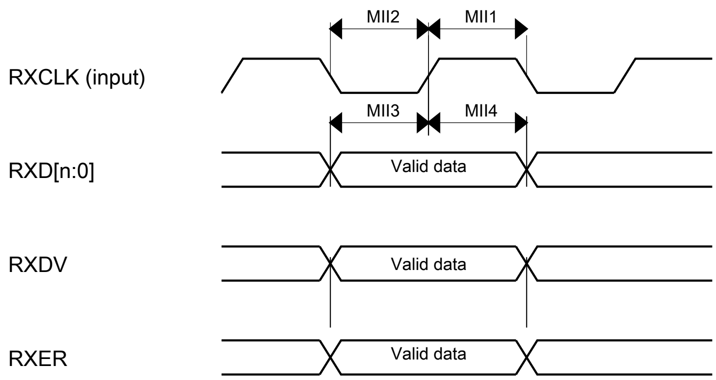

Figure 22. RMII/MII receive signal timing diagram

6.4.3.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 42. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

6.4.4 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 43. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns

Table continues on the next page...

Table 43. Master mode SAI Timing (continued)

no	Parameter	Value		Unit
		Min	Max	
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	-	BCLK period
S4	SAI_BCLK pulse width high/low	45%	55%	ns
S5	SAI_BCLK to SAI_FS output valid	-	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	-	ns
S7	SAI_BCLK to SAI_TXD valid	-	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	-	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	28	-	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	-	ns

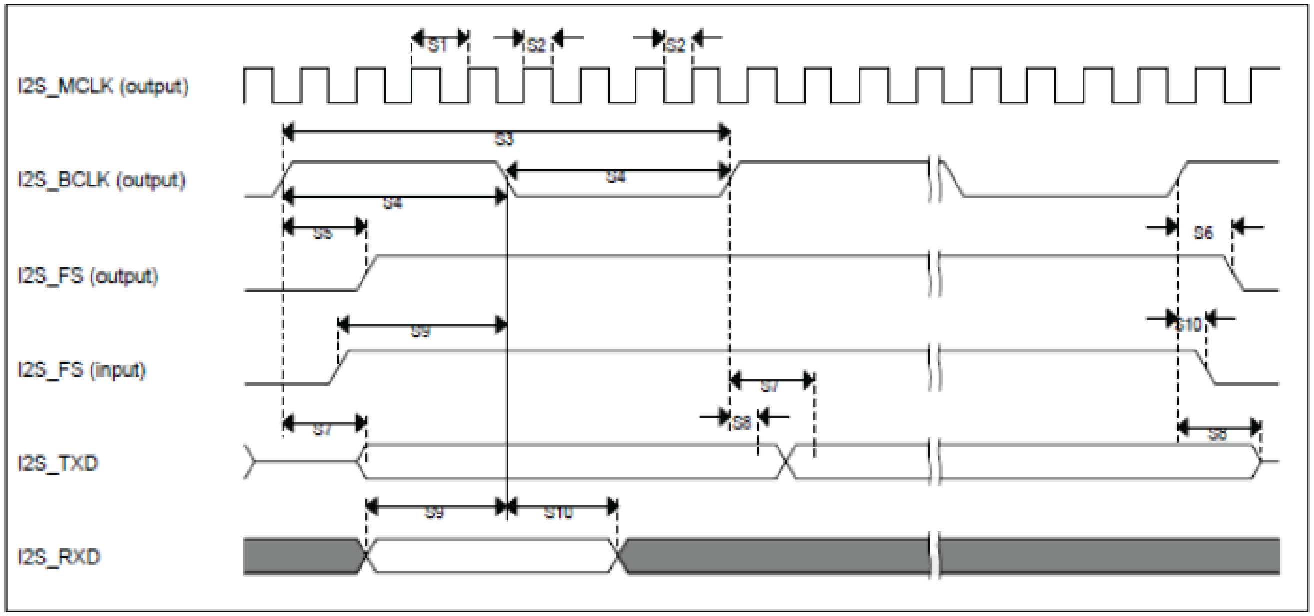

Figure 23. Master mode SAI Timing

Table 44. Slave mode SAI Timing

No	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S11	SAI_BCLK cycle time (input)	80	-	ns
S12	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	-	ns
S14	SAI_FS input hold after SAI_BCLK	2	-	ns

Table continues on the next page...

Table 44. Slave mode SAI Timing (continued)

No	Parameter	Value		Unit
		Min	Max	
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

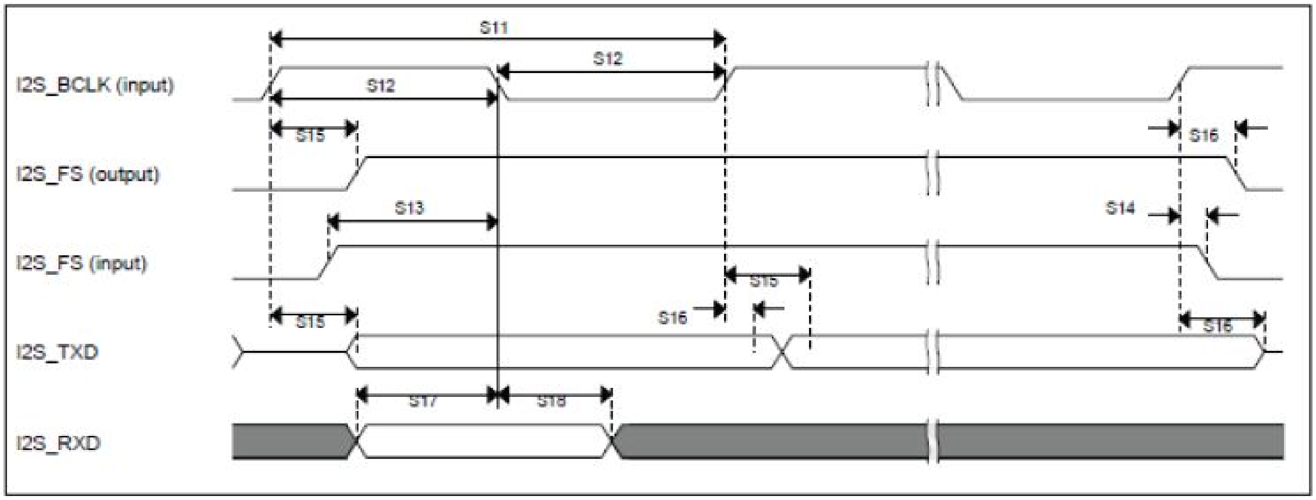

Figure 24. Slave mode SAI Timing

6.5 Debug specifications

6.5.1 JTAG interface timing

Table 45. JTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time [2, 2]	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20[3, 3]	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600[4, 4]	ns

Table continues on the next page...

Board type	Symbol	Description	100 MAPBGA	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.8	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.2	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center (natural convection)	7.8	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

Package	NXP Document Number
100 MAPBGA	98ASA00802D

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev 5.1	22 May 2017	• Removed the Introduction section from Section 4 "General". • In AC Specifications@3.3V section, removed note related to Cz results and added two notes. • In AC Specifications@5V section, added two notes. • In ADC Electrical Specifications section, added spec value of "ADC Analog Pad" at Max leakage (standard channel)@ 105 C T_A in "ADC conversion characteristics (for 10-bit)" table. • In PLL Electrical Specifications section, updated the first footnote of "Jitter calculation" table. • In Analog Comparator Electrical Specifications section, updated the TDLS (propagation delay, low power mode) max value in "Comparator and 6-bit DAC electrical specifications" table to 21 us. • In Recommended Operating Conditions section, updated the footnote link to T_A in "Recommended operating conditions (V DD_HV_x = 5V)" table.

How to Reach Us:

Home Page:
www.nxp.com

Web Support:
www.nxp.com/support

Document Number: MPC5746C
Rev. 5.1, 05/2017