Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz, 160MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SAI, SPI
Peripherals	DMA, I²S, LVD/HVD, POR, WDT
Number of I/O	65
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	128K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 68x10b, 31x12b SAR
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LBGA
Supplier Device Package	100-MAPBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746chk1ammh6

4. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. VIN1_CMP_REF ≤ VDD_HV_A
6. This supply is shorted VDD_HV_A on lower packages.
7. T_J=150°C. Assumes T_A=125°C
    - Assumes maximum θJA of 2s2p board. See Thermal attributes

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
    - Control of external NPN ballast transistor
    - Generating core supply using internal ballast transistor
    - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector (LVD_FLASH) for 3.3 V flash supply (VDD_HV_FLA)
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

1. BCP56, MCP68 and MJD31are guaranteed ballasts.

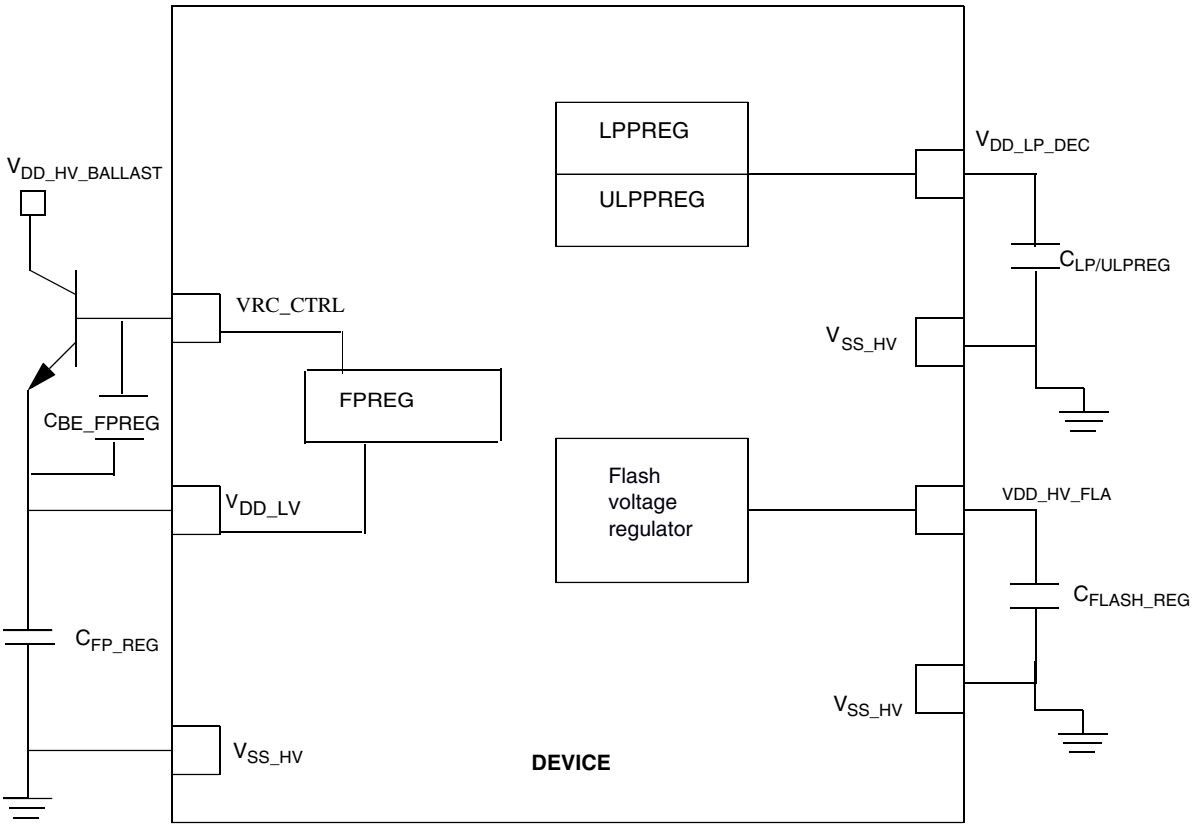


Figure 2. Voltage regulator capacitance connection

NOTE

On BGA, VSS_LV and VSS_HV have been joined on substrate and renamed as VSS.

Table 8. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{fp_reg}[1]	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2[2]	3	µF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
C_{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	µF
	Combined ESR of external capacitor	—	0.001	—	0.1	Ohm
C_{be_fpreg}[3]	Capacitor in parallel to base-emitter	BCP68 and BCP56		3.3		nF
		MJD31		4.7		

Table continues on the next page...

4.4 Voltage monitor electrical characteristics

Table 9. Voltage monitor electrical characteristics

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt[2, 2]	Reset Type	Min	Typ	Max	V
V_{POR_LV}	LV supply power on reset detector	Fall	Untrimmed	Yes	No	Destructive	0.930	0.979	1.028	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				0.980	1.029	1.078	V
			Trimmed				-	-	-	V
$V_{HVD\_LV\_cold}$	LV supply high voltage monitoring, detecting at device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.325	1.345	1.375	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.345	1.365	1.395	V
$V_{LVD\_LV\_PD2\_hot}$	LV supply low voltage monitoring, detecting on the PD2 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1250	1.1425	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1450	1.1625	1.1800	V
$V_{LVD\_LV\_PD1\_hot\ (BGFP)}$	LV supply low voltage monitoring, detecting on the PD1 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.140	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
$V_{LVD\_LV\_PD0\_hot\ (BGFP)}$	LV supply low voltage monitoring, detecting on the PD0 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
V_{POR_HV}	HV supply power on reset detector	Fall	Untrimmed	Yes	No	Destructive	2.7000	2.8500	3.0000	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				2.7500	2.9000	3.0500	V
			Trimmed				-	-	-	V
$V_{LVD\_IO\_A\_LO}$[3, 3]	HV IO_A supply low voltage monitoring - low range	Fall	Untrimmed	Yes	No	Destructive	2.7500	2.9230	3.0950	V
			Trimmed				2.9780	3.0390	3.1000	V
		Rise	Untrimmed				2.7800	2.9530	3.1250	V
			Trimmed				3.0080	3.0690	3.1300	V
$V_{LVD\_IO\_A\_HI}$[3]	HV IO_A supply low voltage monitoring - high range	Fall	Trimmed	No	Yes	Destructive	Disabled at Start			
							4.0600	4.151	4.2400	V
		Rise	Trimmed				Disabled at Start			
							4.1150	4.2010	4.3000	V

Table continues on the next page...

5.3 AC specifications @ 5 V Range

Table 16. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		4.5/4.5		1.3/1.2	25	11
		6/6		2.5/2	50	
		13/13		9/9	200	
		5.25/5.25		3/2	25	10
		9/8		5/4	50	
		22/22		18/16	200	
		27/27		13/13	50	01[2, 2]
		40/40		24/24	200	
		40/40		24/24	50	00[2]
		65/65		40/40	200	
pad_i_hv/ pad_sr_hv (input)		1.5/1.5		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V

Table continues on the next page...

Table 18. Functional reset pad electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{HYS}	CMOS Input Buffer hysterisis	—	300	—	—	mV
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current [1, 1]	Device under power-on reset $V_{DD\_HV\_A}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD\_HV\_A}$	0.2	—	—	mA
		Device under power-on reset $V_{DD\_HV\_A}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD\_HV\_IO}$	11	—	—	mA
W_{FRST}	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	$\overline{\text{RESET}}$ input not filtered pulse	—	2000	—	—	ns
$\|I_{WPU}\|$	Weak pull-up current absolute value	RESET pin V_{IN} = V_{DD}	23	—	82	µA

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{\text{PORST}}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{\text{PORST}}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	0.65 x $V_{DD\_HV\_A}$	—	—	V
V_{IL}	Input low level	—	—	0.35 x $V_{DD\_HV\_A}$	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

Table 20. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
R_{AD}[6]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity (precise channel)	—	–2	—	2	LSB
INL	Integral non-linearity (standard channel)	—	–3	—	3	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (precision channel)	150 °C	—	—	250	nA
	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C $_{TA}$	—	5	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{precision\ channels}$	Total unadjusted error for precision channels	Without current injection	–6	+/-4	6	LSB
		With current injection[7, 7]		+/-5		LSB
$TUE_{standard/extended\ channels}$	Total unadjusted error for standard/ extended channels	Without current injection	–8	+/-6	8	LSB
		With current injection[7]		+/-8		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	µs

1. Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 6.
7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

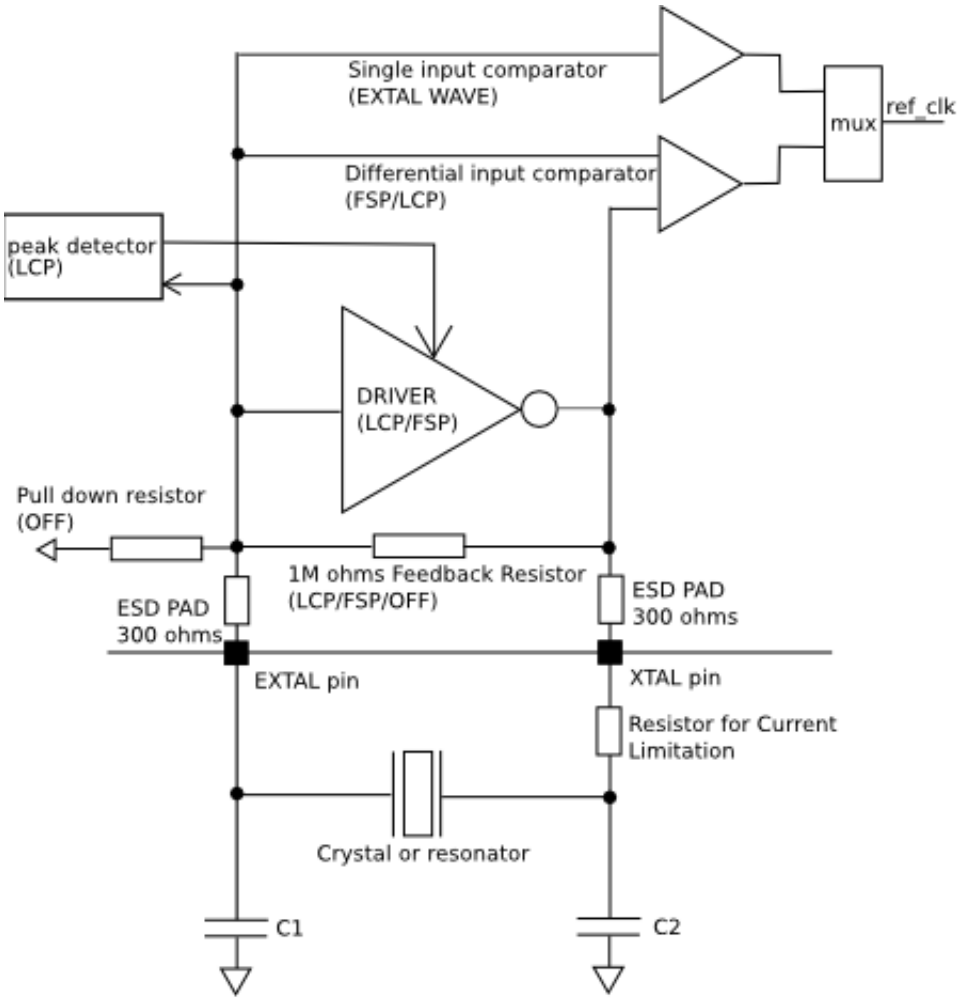


Figure 7. Oscillator connections scheme

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	LCP			23		mA/V
		FSP			33		
V_{XOSCHS}	Oscillation Amplitude	LCP[1, 2, 1, 2]	8 MHz		1.0		V_{PP}
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP[1]	8 MHz		2		ms
			16 MHz		1		
			40 MHz		0.5		

Table continues on the next page...

Table 23. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
	Oscillator Analog Circuit supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		
		LCP	8 MHz		141		uA
			16 MHz		252		
			40 MHz		518		
V_{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3	1.95			V
V_{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3			1.25	V

1. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board.
2. Typ value for oscillator supply 3.3 V@27 °C

6.2.2 32 kHz Oscillator electrical specifications

Table 24. 32 kHz oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{osc_lo}	Oscillator crystal or resonator frequency		32		40	KHz
t_{cst}	Crystal Start-up Time[1, 2]				2	s

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 16 MHz RC Oscillator electrical specifications

Table 25. 16 MHz RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F_{Target}	IRC target frequency	—	—	16	—	MHz
PTA	IRC frequency variation after trimming	—	-5	—	5	%
$T_{startup}$	Startup time	—		—	1.5	us
T_{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T_{LTJIT}	Long term jitter		—	—	0.2	%

Table 28. Jitter calculation (continued)

Type of jitter	Jitter due to Supply Noise (ps) J_{SN}[1]	Jitter due to Fractional Mode (ps) J_{SDM}[2]	Jitter due to Fractional Mode J_{SSCG} (ps) [3]	1 Sigma Random Jitter J_{RJ} (ps) [4]	Total Period Jitter (ps)
Long Term Jitter (Integer Mode)				40	+/-(N x J_{RJ})
Long Term jitter (Fractional Mode)				100	+/-(N x J_{RJ})

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on VDD_LV and VSS_LV.
2. This jitter component is added when the PLL is working in the fractional mode.
3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.
4. The value of N is dependent on the accuracy requirement of the application. See Table 29

Table 29. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27
4	6.30 × 1e-03
5	5.63 × 1e-05
6	2.00 × 1e-07
7	2.82 × 1e-10

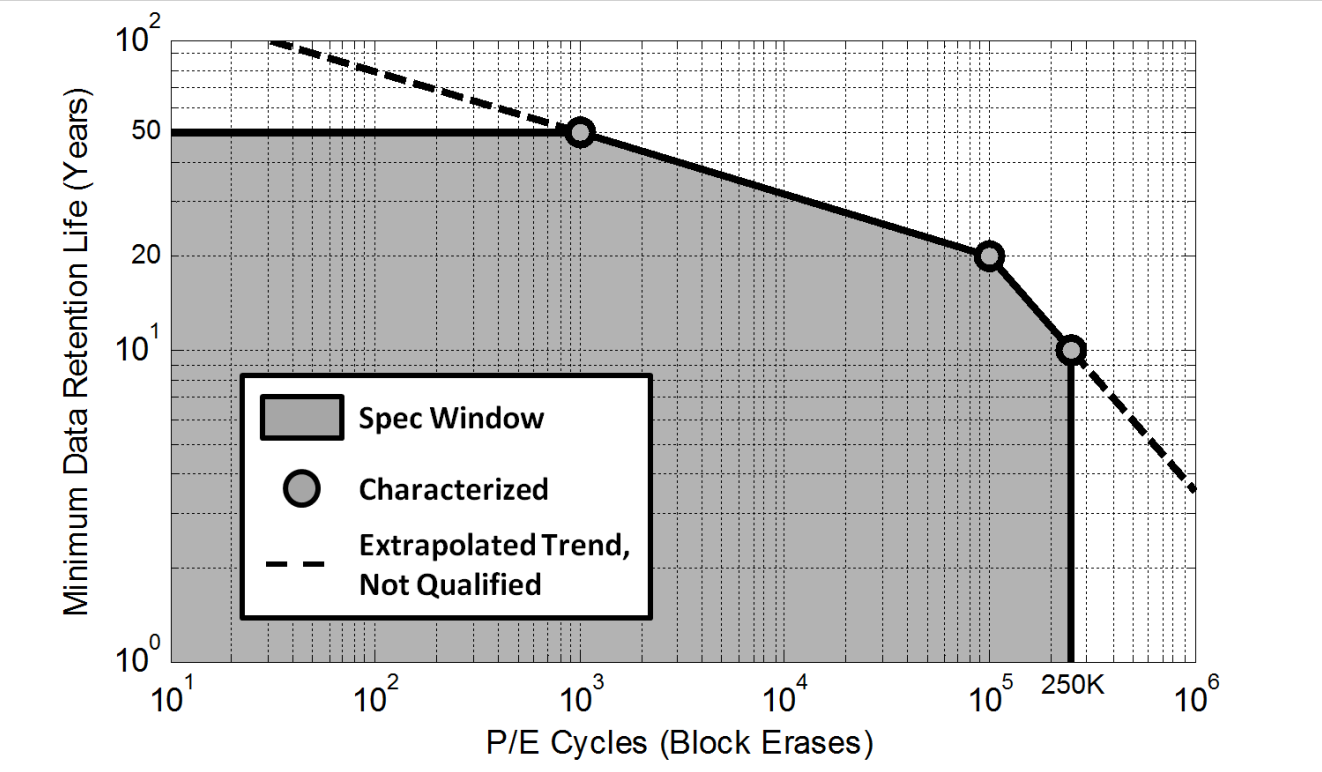
6.3 Memory interfaces

6.3.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.



6.3.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs

Table continues on the next page...

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 34. Flash Read Wait State and Address Pipeline Control Combinations

Flash frequency	RWSC setting	APC setting
0 MHz < fFlash <= 33 MHz	0	0
33 MHz < fFlash <= 100 MHz	2	1
100 MHz < fFlash <= 133 MHz	3	1
133 MHz < fFlash <= 160 MHz	4	1

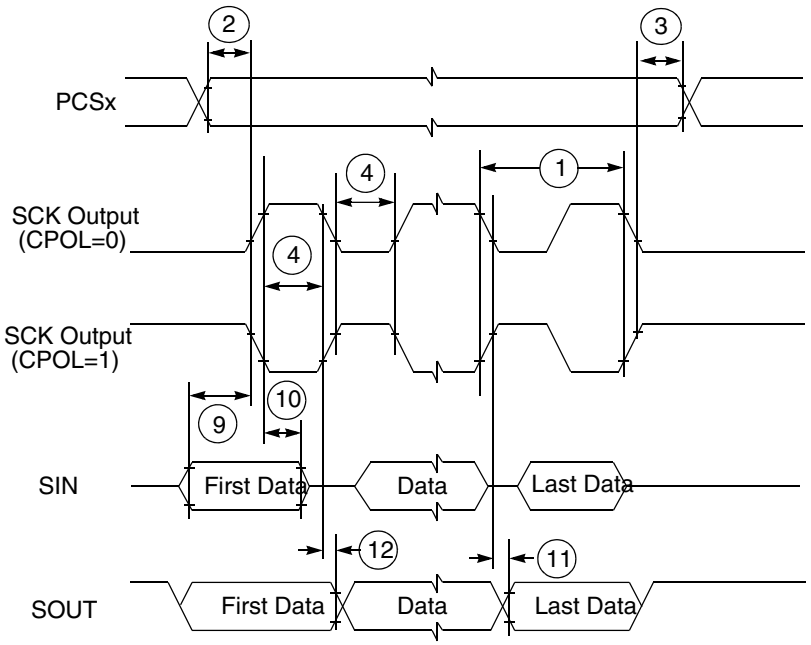


Figure 8. DSPI classic SPI timing — master, CPHA = 0

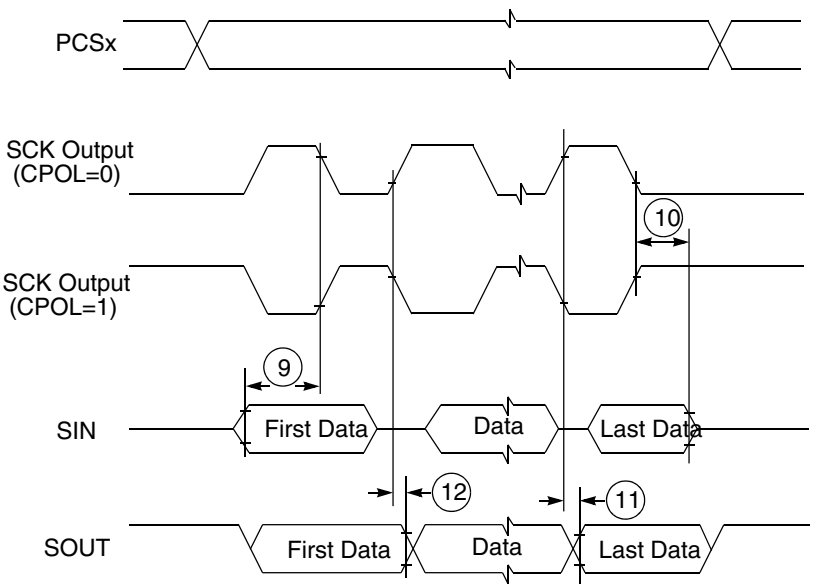


Figure 9. DSPI classic SPI timing — master, CPHA = 1

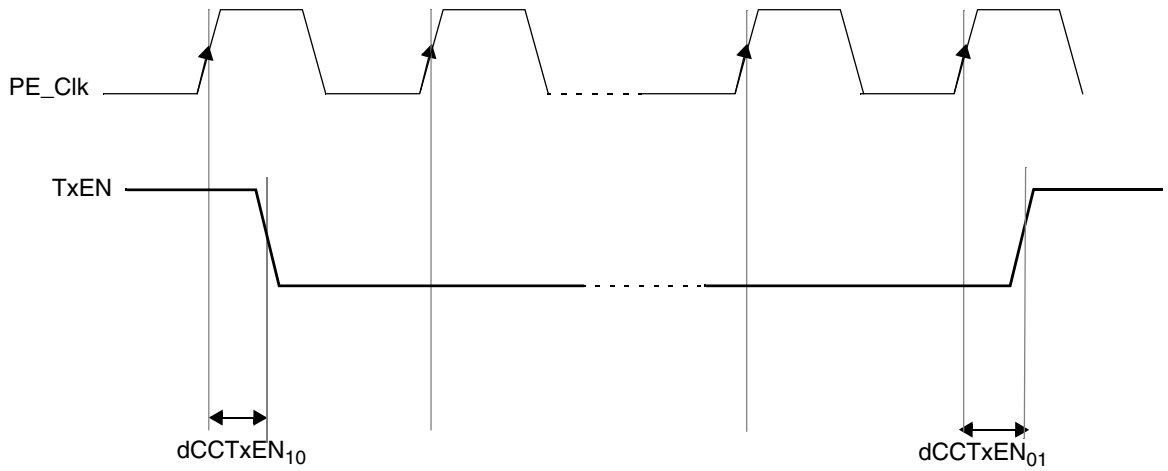


Figure 18. TxEN signal propagation delays

6.4.2.3 TxD

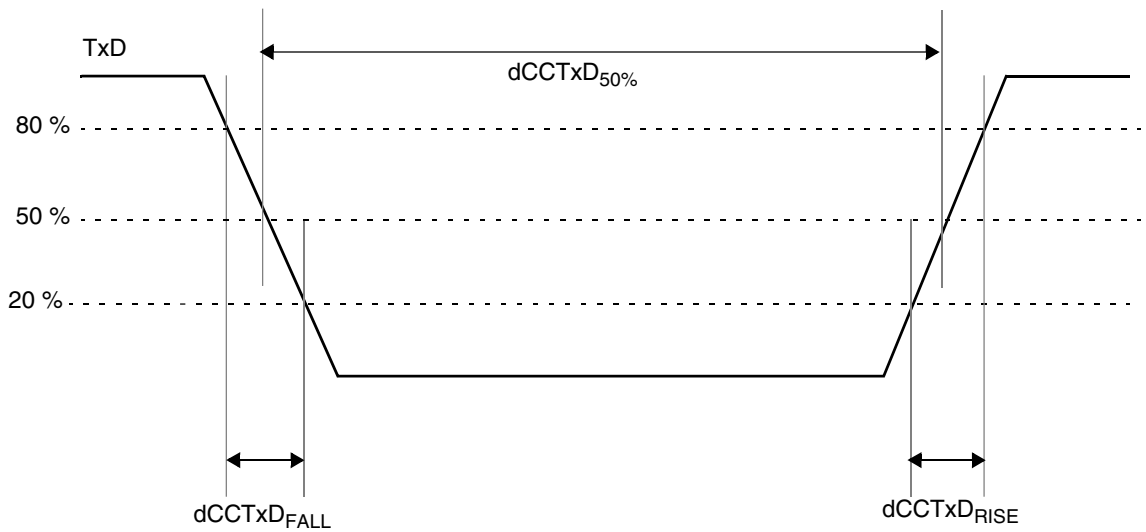


Figure 19. TxD Signal

Table 39. TxD output characteristics

Name	Description[1]	Min	Max	Unit
$dCCT_{xAsym}$	Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	Sum of Rise and Fall time of TxD signal at the output	—	9[2]	ns

Table continues on the next page...

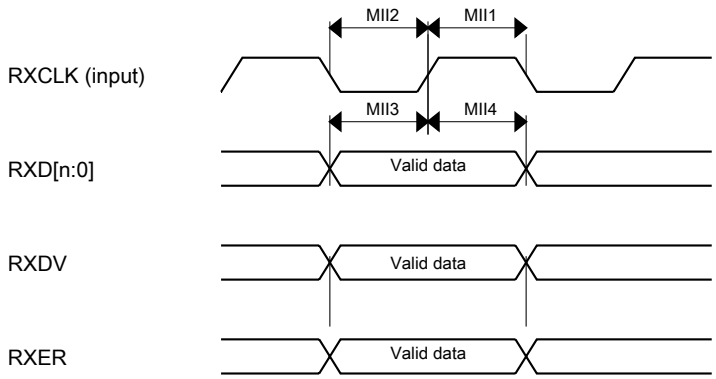


Figure 22. RMII/MII receive signal timing diagram

6.4.3.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 42. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

6.4.4 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 43. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns

Table continues on the next page...

Table 45. JTAG pin AC electrical characteristics [1] (continued)

#	Symbol	Characteristic	Min	Max	Unit
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

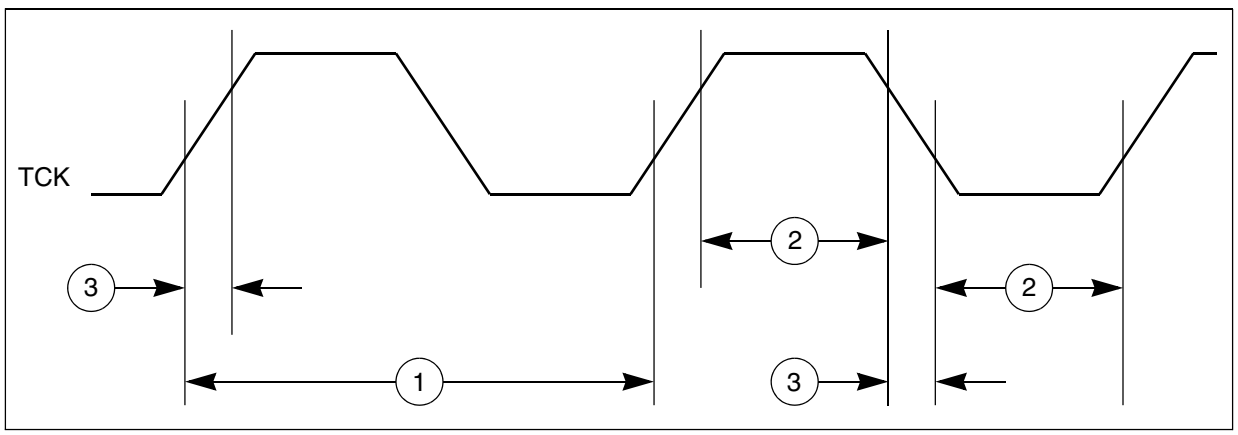


Figure 25. JTAG test clock input timing

Board type	Symbol	Description	100 MAPBGA	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.8	°C/W	44
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.2	°C/W	55
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	66
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center (natural convection)	7.8	°C/W	77

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

Package	NXP Document Number
100 MAPBGA	98ASA00802D

Table continues on the next page...

10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

Table 50. BAF execution duration

BAF execution duration	Min	Typ	Max	Unit
BAF execution time (boot header at first location)	—	200	—	µs
BAF execution time (boot header at last location)	—	—	320	µs

10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

Rev 2	7 August 2015	• In features:
		  • Updated BAF feature with sentence, Boot Assist Flash (BAF) supports internal flash programming via a serial link (SCI)
		  • Updated FlexCAN3 with FD support
		  • Updated number of STMs to two.
		• In Block diagram:
		  • Updated SRAM size from 128 KB to 256 KB.
		• In Family Comparison:
		  • Added note: All optional features (Flash memory, RAM, Peripherals) start with lowest number or address (e.g. FlexCAN0) and end at highest available number or address (e.g. MPC574xB/D have 6 CAN, ending with FlexCAN5).
		  • Revised MPC5746C Family Comparison table.
		• In Ordering parts:
		  • Updated ordering parts diagram to include 100 MAPBGA information and optional fields.
		• In table: Absolute maximum ratings
		  • Removed entry: 'V_{SS_HV}'
		  • Added spec for 'V_{DD12}'
		  • Updated 'Max' column for 'V_{INA}'
		  • Updated footnote for $V_{DD\_HV\_ADC1\_REF}$.
		  • Added footnote to 'Conditions', All voltages are referred to V_{SS_HV} unless otherwise specified
		  • Removed footnote from 'Max', Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
		• In section: Recommended operating conditions
		  • Added opening text: "The following table describes the operating conditions ... "
		  • Added note: "$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ are all ... "
		  • In table: Recommended operating conditions (VDD_HV_x = 3.3 V) and (VDD_HV_x = 5 V)
		  • Added footnote to 'Conditions' cloumn, (All voltages are referred to V_{SS_HV} unless otherwise specified).
		  • Updated footnote for 'Min' column to Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
		  • Removed footnote for '$V_{DD\_HV\_A}$', '$V_{DD\_HV\_B}$', and '$V_{DD\_HV\_C}$' entry and updated the parameter column.
		  • Removed entry : 'V_{SS_HV}'
		  • Updated 'Parameter' column for '$V_{DD\_HV\_FLA}$', '$V_{DD\_HV\_ADC1\_REF}$', 'V_{DD_LV}'
		  • Updated 'Min' column for '$V_{DD\_HV\_ADC0}$' '$V_{DD\_HV\_ADC1}$'
		  • Updated 'Parameter' 'Min' 'Max' columns for '$V_{SS\_HV\_ADC0}$' and '$V_{SS\_HV\_ADC1}$'
		  • Updated footnote for 'V_{DD_LV} ' to V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
		  • Removed row for symbol 'V_{SS_LV}'
		  • Removed footnote from 'Max' column of '$V_{DD\_HV\_ADC0}$' and '$V_{DD\_HV\_ADC1}$', (PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1).
		  • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)
		  • Removed footnote from '$V_{IN1\_CMP\_REF}$', (Only applicable when supplying from external source).
		  • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 5 V)
		  • Added spec for '$V_{IN1\_CMP\_REF}$' and corresponding footnotes.

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In section: Voltage monitor electrical characteristics
		  • Updated description for Low Voltage detector block.
		  • Added note, BCP56, MCP68 and MJD31 are guaranteed ballasts.
		  • In table: Voltage regulator electrical specifications
		  • Added footnote, Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
		  • Revised table, Voltage monitor electrical characteristics

		• In section: Supply current characteristics
		  • In table: Current consumption characteristics
		  • $I_{DD\_BODY\_4}$: Updated SYS_CLK to 120 MHz.
		  • $I_{DD\_BODY\_4}$: Updated Max for T_a= 105 °C fand 85 °C)
		  • I_{dd_STOP}: Added condition for T_a= 105 °C and removed Max value for T_a= 85 °C.
		  • $I_{DD\_HV\_ADC\_REF}$: Added condition for T_a= 105 °C and 85 °C and removed Max value for T_a= 25 °C.
		  • $I_{DD\_HV\_FLASH}$: Added condition for T_a= 105 °C and 85 °C
		  • In table: Low Power Unit (LPU) Current consumption characteristics
		  • LPU_RUN and LPU_STOP: Added condition for T_a= 105 °C and 85 °C
		  • In table: STANDBY Current consumption characteristics
		  • Added condition for T_a= 105 °C and 85 °C for all entries.
		
		• In section: I/O parameters
		  • In table: Functional Pad AC Specifications @ 3.3 V Range
		  • Updated values for 'pad_sr_hv (output)'
		  • In table: DC electrical specifications @ 3.3V Range
		  • Updateded Min and Max values for Vih and Vil respectively.
		  • In table: Functional Pad AC Specifications @ 5 V Range
		  • Updated values for 'pad_sr_hv (output)'
		  • In table DC electrical specifications @ 5 V Range
		  • Updated Min value for Vhys

Table continues on the next page...

How to Reach Us:

Home Page:
www.nxp.com

Web Support:
www.nxp.com/support

Document Number: MPC5746C
Rev. 5.1, 05/2017