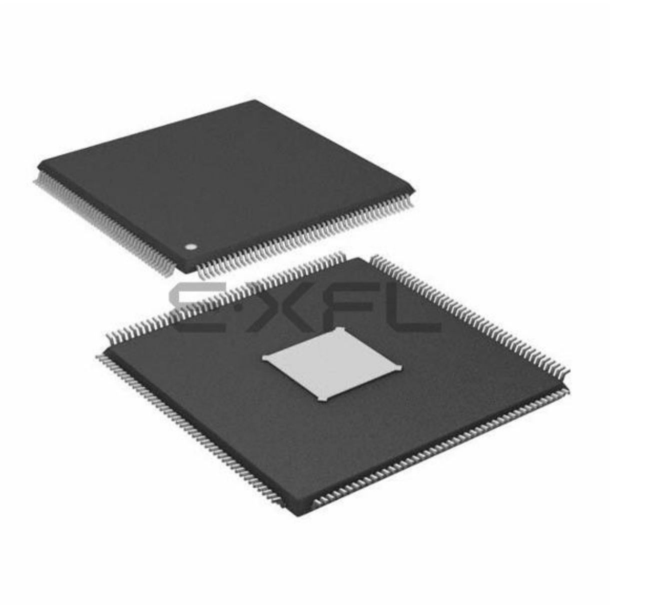

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z2, e200z4 |
| Core Size | 32-Bit Dual-Core |
| Speed | 80MHz/160MHz |
| Connectivity | CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG |
| Peripherals | DMA, LVD, POR, WDT |
| Number of I/O | 129 |
| Program Memory Size | 3MB (3M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 80x10b, 64x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP Exposed Pad |
| Supplier Device Package | 176-LQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746chk1avku6 |

# Table of Contents

# 1 Block diagram

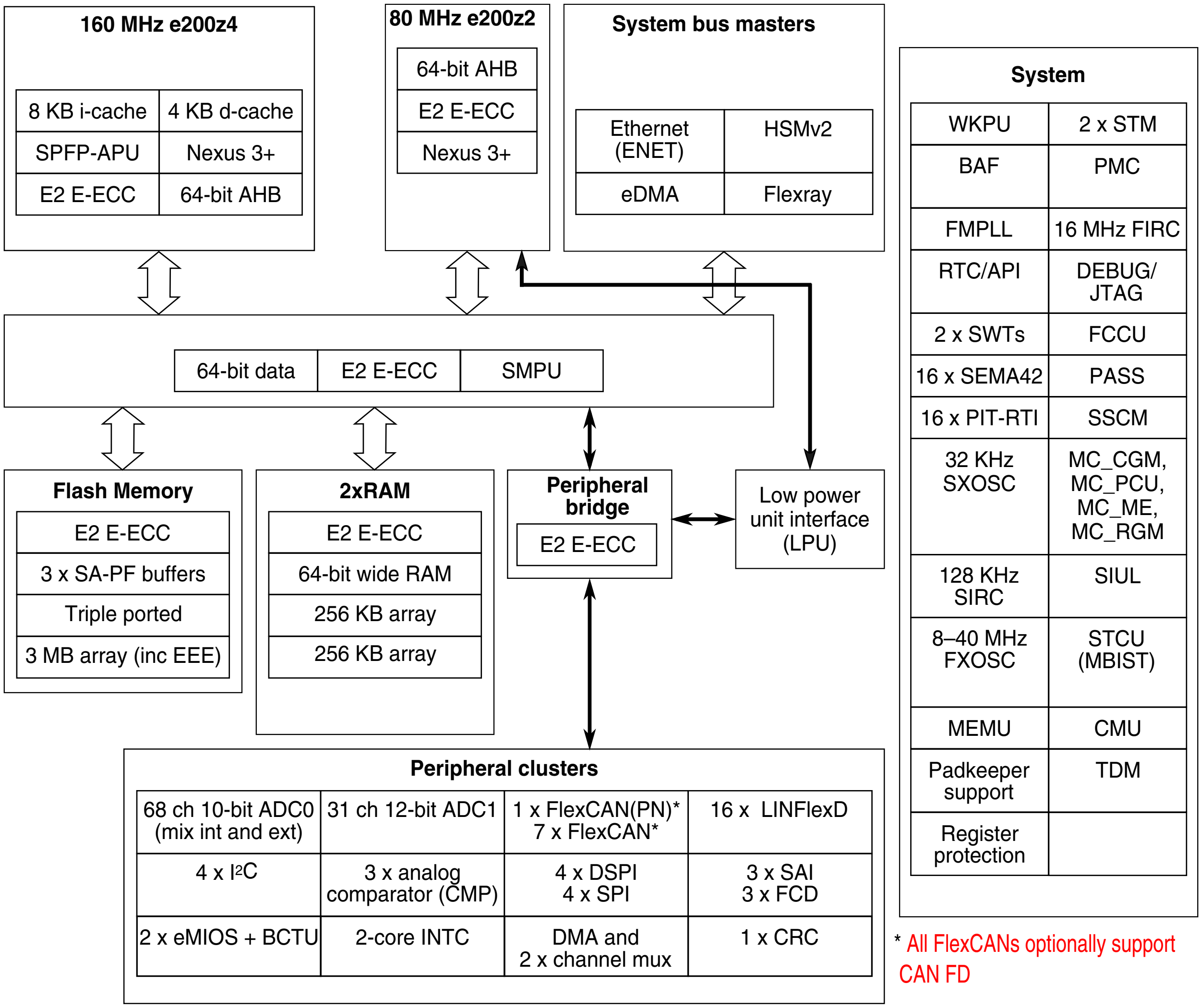



**Figure 1. MPC5746C block diagram**

# 2 Family comparison

The following table provides a summary of the different members of the MPC5746C family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

## Table 8. Voltage regulator electrical specifications (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{flash\_reg}$ [4] | External decoupling / stability capacitor for internal Flash regulators | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1.32 | 2.2 | 3 | µF |
| | Combined ESR of external capacitor | — | 0.001 | — | 0.03 | Ohm |
| $C_{HV\_VDD\_A}$ | VDD_HV_A supply capacitor [5, 5] | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | µF |
| $C_{HV\_VDD\_B}$ | VDD_HV_B supply capacitor[5] | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | µF |
| $C_{HV\_VDD\_C}$ | VDD_HV_C supply capacitor[5] | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | µF |
| $C_{HV\_ADC0}$ $C_{HV\_ADC1}$ | HV ADC supply decoupling capacitances | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | µF |
| $C_{HV\_ADR}$ [6] | HV ADC SAR reference supply decoupling capacitances | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 0.47 | — | — | µF |
| $V_{DD\_HV\_BALLAST}$ [7] | FPREG Ballast collector supply voltage | When collector of NPN ballast is directly supplied by an on board supply source (not shared with VDD_HV_A supply pin) without any series resistance, that is, $R_{C\_BALLAST}$ less than 0.01 Ohm. | 2.25 | — | 5.5 | V |
| $R_{C\_BALLAST}$ | Series resistor on collector of FPREG ballast | When VDD_HV_BALLAST is shorted to VDD_HV_A on the board | — | — | 0.1 | Ohm |
| $t_{SU}$ | Start-up time with external ballastafter main supply (VDD_HV_A) stabilization | Cfp_reg = 3 µF | — | 74 | — | µs |
| $t_{SU\_int}$ | Start-up time with internal ballast after main supply (VDD_HV_A) stabilization | Cfp_reg = 3 µF | — | 103 | — | µs |
| $t_{ramp}$ | Load current transient | Iload from 15% to 55%<br>$C_{fp\_reg}$ = 3 µF | | 1.0 | | µs |

1. Split capacitance on each pair VDD_LV pin should sum up to a total value of $C_{fp\_reg}$
2. Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.
3. Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
4. It is required to minimize the board parasitic inductance from decoupling capacitor to VDD_HV_FLA pin and the routing inductance should be less than 1nH.

## 5.2 DC electrical specifications @ 3.3V Range

**Table 15. DC electrical specifications @ 3.3V Range**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Vih (pad_i_hv) | Pad_I_HV Input Buffer High Voltage | 0.72*VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil (pad_i_hv) | Pad_I_HV Input Buffer Low Voltage | VDD_HV_x - 0.3 | 0.45*VDD_HV_x | V |
| Vhys (pad_i_hv) | Pad_I_HV Input Buffer Hysteresis | 0.11*VDD_HV_x | | V |
| Vih_hys | CMOS Input Buffer High Voltage (with hysteresis enabled) | 0.67*VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil_hys | CMOS Input Buffer Low Voltage (with hysteresis enabled) | VDD_HV_x - 0.3 | 0.35*VDD_HV_x | V |
| Vih | CMOS Input Buffer High Voltage (with hysteresis disabled) | 0.57 * VDD_HV_x[1, 1] | VDD_HV_x[1] + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage (with hysteresis disabled) | VDD_HV_x - 0.3 | 0.4 * VDD_HV_x[1] | V |
| Vhys | CMOS Input Buffer Hysteresis | 0.09 * VDD_HV_x[1] | | V |
| Pull_IIH (pad_i_hv) | Weak Pullup Current[2, 2] Low | 15 | | µA |
| Pull_IIH (pad_i_hv) | Weak Pullup Current[3, 3] High | | 55 | µA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current[3] Low | 28 | | µA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current[2] High | | 85 | µA |
| Pull_Ioh | Weak Pullup Current[4] | 15 | 50 | µA |
| Pull_Iol | Weak Pulldown Current[5] | 15 | 50 | µA |
| Iinact_d | Digital Pad Input Leakage Current (weak pull inactive) | -2.5 | 2.5 | µA |
| Voh | Output High Voltage[6] | 0.8 *VDD_HV_x[1] | — | V |
| Vol | Output Low Voltage[7]<br>Output Low Voltage[8] | — | 0.2 *VDD_HV_x[1]<br>0.1 *VDD_HV_x | V |
| Ioh_f | Full drive Ioh[9, 9] (SIUL2_MSCRn.SRC[1:0] = 11) | 18 | 70 | mA |
| Iol_f | Full drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 11) | 21 | 120 | mA |
| Ioh_h | Half drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 10) | 9 | 35 | mA |
| Iol_h | Half drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 10) | 10.5 | 60 | mA |

1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

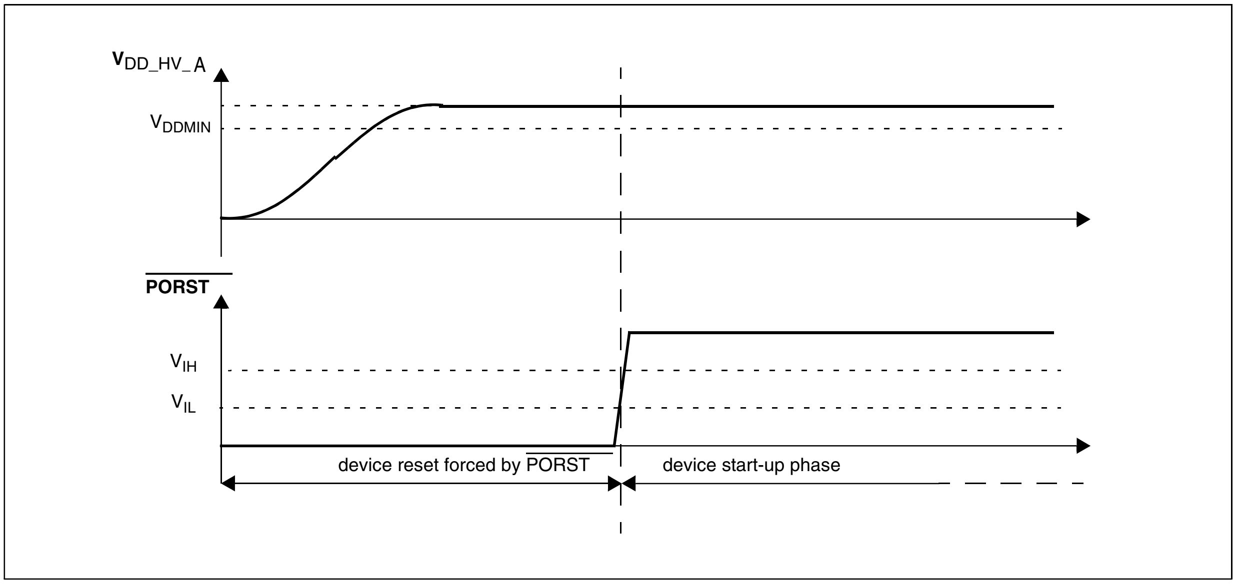



**Figure 3. Start-up reset requirements**

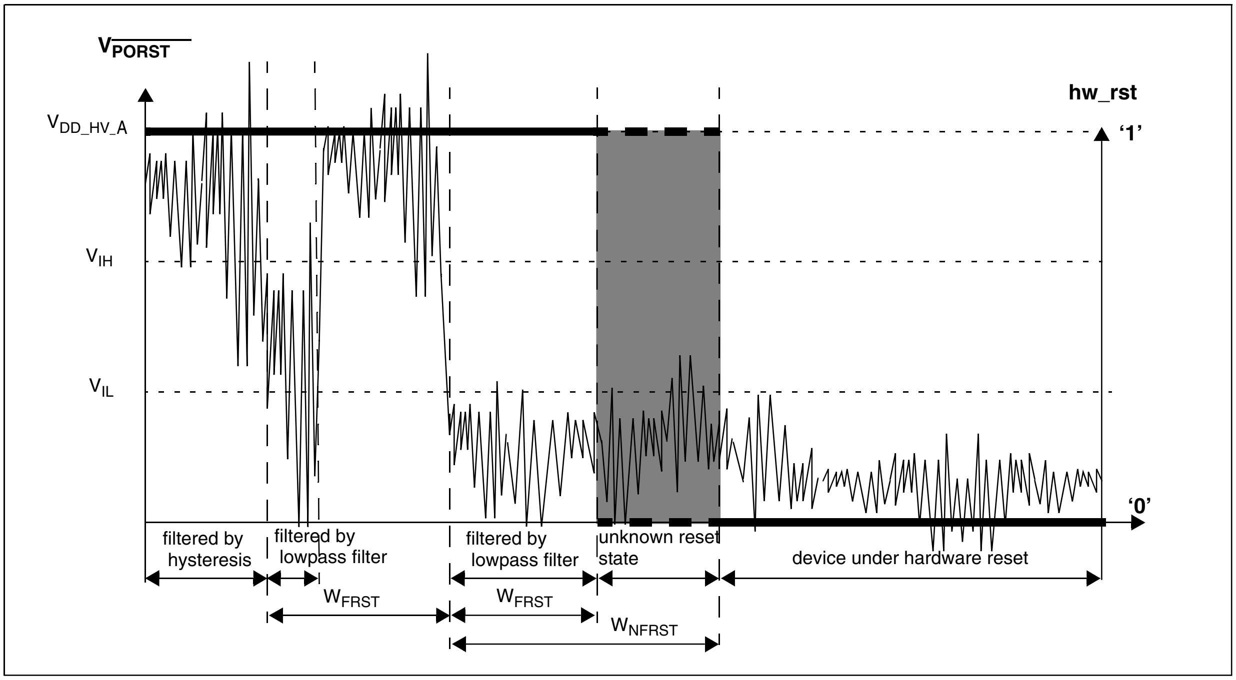


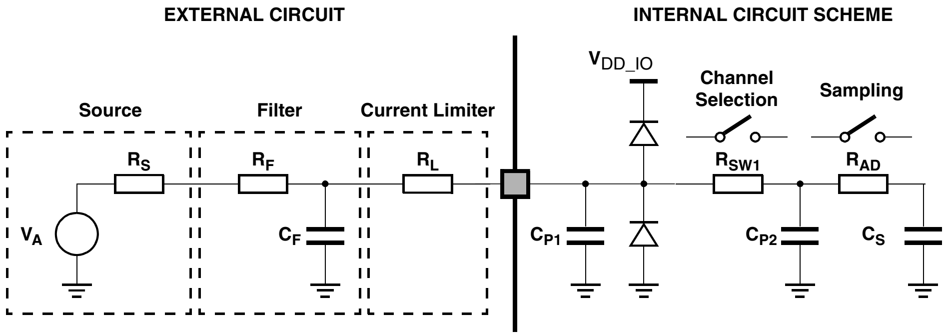

**Figure 4. Noise filtering on reset signal**

**Table 18. Functional reset pad electrical specifications**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | CMOS Input Buffer High Voltage | — | $0.65 * V_{DD\_HV\_x}$ | — | $V_{DD\_HV\_x} + 0.3$ | V |
| $V_{IL}$ | CMOS Input Buffer Low Voltage | — | $V_{DD\_HV\_x} - 0.3$ | — | $0.35 * V_{DD\_HV\_x}$ | V |

*Table continues on the next page...*

### 6.1.1.1 Input equivalent circuit and ADC conversion characteristics




$R_S$ Source Impedance
$R_F$ Filter Resistance
$C_F$ Filter Capacitance
$R_L$ Current Limiter Resistance
$R_{SW1}$ Channel Selection Switch Impedance
$R_{AD}$ Sampling Switch Impedance
$C_P$ Pin Capacitance (two contributions, $C_{P1}$ and $C_{P2}$)
$C_S$ Sampling Capacitance

**Figure 6. Input equivalent circuit**

**NOTE**

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

**Table 20. ADC conversion characteristics (for 12-bit)**

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}$ | ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency) | — | 15.2 | 80 | 80 | MHz |
| $f_s$ | Sampling frequency | 80 MHz | — | — | 1.00 | MHz |
| $t_{sample}$ | Sample time[3] | 80 MHz@ 100 ohm source impedance | 250 | — | — | ns |
| $t_{conv}$ | Conversion time[4] | 80 MHz | 700 | — | — | ns |
| $t_{total\_conv}$ | Total Conversion time $t_{sample}$ + $t_{conv}$ (for standard and extended channels) | 80 MHz | 1.5[5] | — | — | µs |
| | Total Conversion time $t_{sample}$ + $t_{conv}$ (for precision channels) | | 1 | — | — | |
| $C_S$[6, 6] | ADC input sampling capacitance | — | — | 3 | 5 | pF |
| $C_{P1}$[6] | ADC input pin capacitance 1 | — | — | — | 5 | pF |
| $C_{P2}$[6] | ADC input pin capacitance 2 | — | — | — | 0.8 | pF |
| $R_{SW1}$[6] | Internal resistance of analog source | $V_{REF}$ range = 4.5 to 5.5 V | — | — | 0.3 | kΩ |
| | | $V_{REF}$ range = 3.15 to 3.6 V | — | — | 875 | Ω |

*Table continues on the next page...*

## Table 20. ADC conversion characteristics (for 12-bit) (continued)

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{AD}$[6] | Internal resistance of analog source | — | — | — | 825 | Ω |
| INL | Integral non-linearity (precise channel) | — | –2 | — | 2 | LSB |
| INL | Integral non-linearity (standard channel) | — | –3 | — | 3 | LSB |
| DNL | Differential non-linearity | — | –1 | — | 1 | LSB |
| OFS | Offset error | — | –6 | — | 6 | LSB |
| GNE | Gain error | — | –4 | — | 4 | LSB |
| ADC Analog Pad (pad going to one ADC) | Max leakage (precision channel) | 150 °C | — | — | 250 | nA |
| | Max leakage (standard channel) | 150 °C | — | — | 2500 | nA |
| | Max leakage (standard channel) | 105 °C $_{TA}$ | — | 5 | 250 | nA |
| | Max positive/negative injection | | –5 | — | 5 | mA |
| $TUE_{precision\ channels}$ | Total unadjusted error for precision channels | Without current injection | –6 | +/-4 | 6 | LSB |
| | | With current injection[7, 7] | | +/-5 | | LSB |
| $TUE_{standard/extended\ channels}$ | Total unadjusted error for standard/ extended channels | Without current injection | –8 | +/-6 | 8 | LSB |
| | | With current injection[7] | | +/-8 | | LSB |
| $t_{recovery}$ | STOP mode to Run mode recovery time | | | | < 1 | μs |

1. Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_{sample}$. After the end of the sample time $t_{sample}$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_{sample}$ depend on programming.
4. This parameter does not include the sample time $t_{sample}$, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 6.
7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

## Table 21. ADC conversion characteristics (for 10-bit)

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}$ | ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.) | — | 15.2 | 80 | 80 | MHz |
| $f_s$ | Sampling frequency | — | — | — | 1.00 | MHz |
| $t_{sample}$ | Sample time[3] | 80 MHz@ 100 ohm source impedance | 275 | — | — | ns |

*Table continues on the next page...*

## 6.2 Clocks and PLL interfaces modules

### 6.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

**NOTE**

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

### 6.2.4 128 KHz Internal RC oscillator Electrical specifications

**Table 26. 128 KHz Internal RC oscillator electrical specifications**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{oscu}$[1] | Oscillator frequency | Calibrated | 119 | 128 | 136.5 | KHz |
| | Temperature dependence | | | | 600 | ppm/C |
| | Supply dependence | | | | 18 | %/V |
| | Supply current | Clock running | | | 2.75 | µA |
| | | Clock stopped | | | 200 | nA |

1. Vdd=1.2 V, 1.32V, $T_a$=-40 C, 125 C

### 6.2.5 PLL electrical specifications

**Table 27. PLL electrical specifications**

| Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Input Frequency | 8 | | 40 | MHz | |
| VCO Frequency Range | 600 | | 1280 | MHz | |
| Duty Cycle at pllclkout | 48% | | 52% | | This specification is guaranteed at PLL IP boundary |
| Period Jitter | | | See Table 28 | ps | NON SSCG mode |
| TIE | | | See Table 28 | | at 960 M Integrated over 1MHz offset not valid in SSCG mode |
| Modulation Depth (Center Spread) | +/- 0.25% | | +/- 3.0% | | |
| Modulation Frequency | | | 32 | KHz | |
| Lock Time | | | 60 | µs | Calibration mode |

**Table 28. Jitter calculation**

| Type of jitter | Jitter due to Supply Noise (ps) $J_{SN}$[1] | Jitter due to Fractional Mode (ps) $J_{SDM}$[2] | Jitter due to Fractional Mode $J_{SSCG}$ (ps) [3] | 1 Sigma Random Jitter $J_{RJ}$ (ps) [4] | Total Period Jitter (ps) |
|---|---|---|---|---|---|
| Period Jitter | 60 ps | 3% of pllclkout1,2 | Modulation depth | 0.1% of pllclkout1,2 | +/-($J_{SN}$+$J_{SDM}$+$J_{SSCG}$+N[4] ×$J_{RJ}$) |

*Table continues on the next page...*

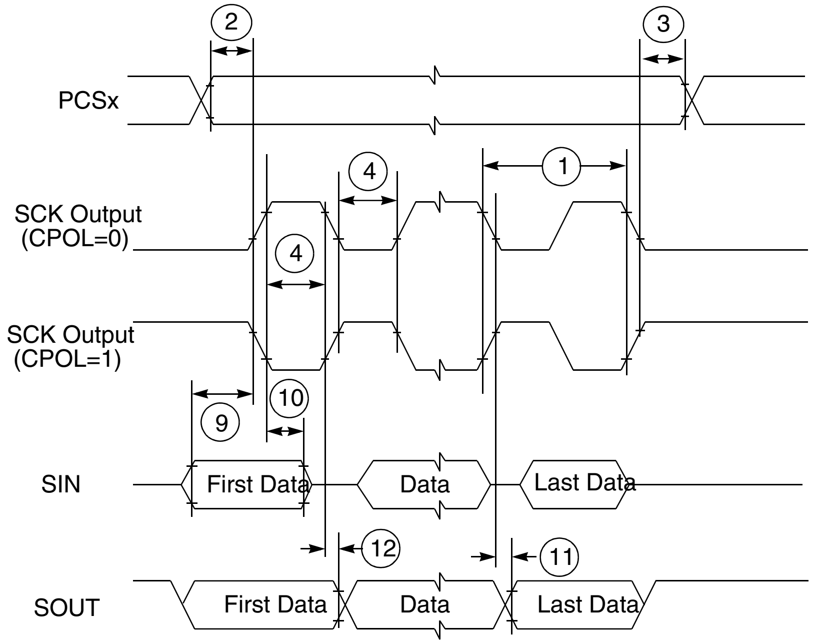



**Figure 8. DSPI classic SPI timing — master, CPHA = 0**

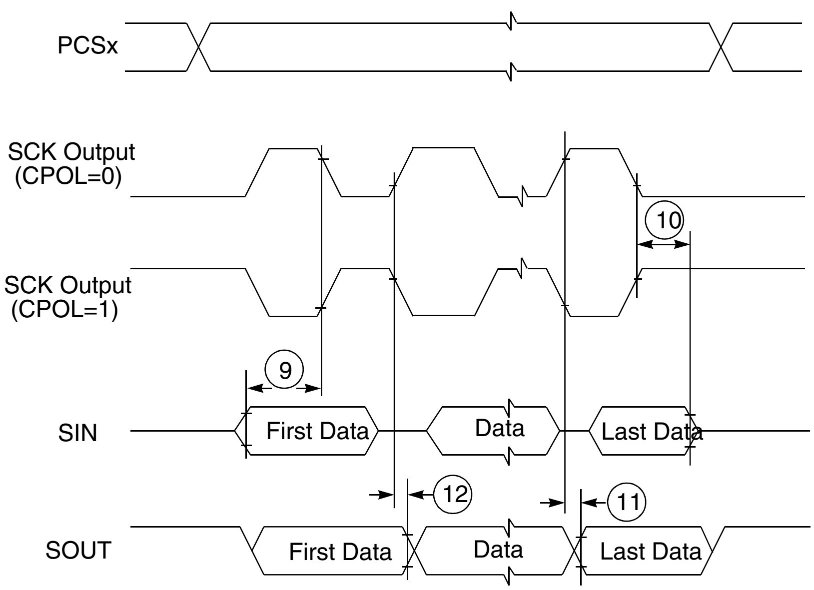



**Figure 9. DSPI classic SPI timing — master, CPHA = 1**

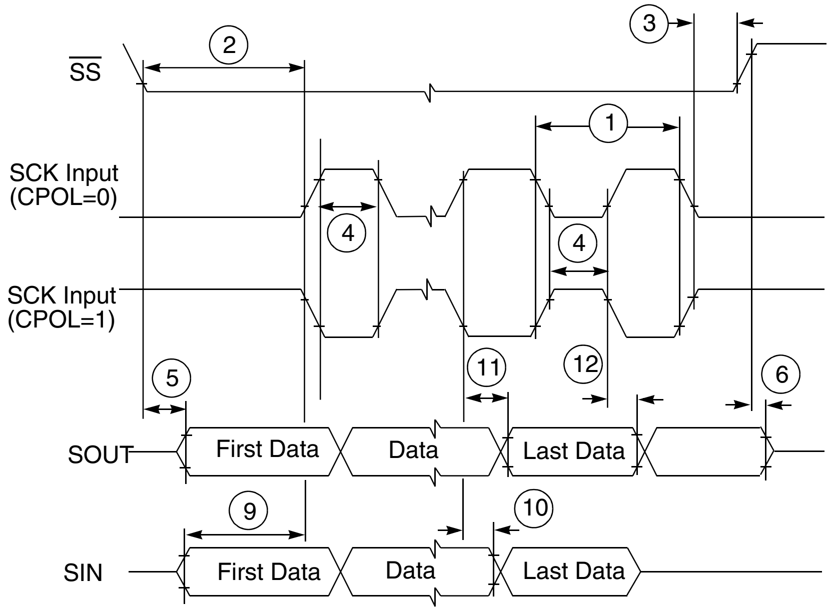



**Figure 14. DSPI modified transfer format timing – slave, CPHA = 0**

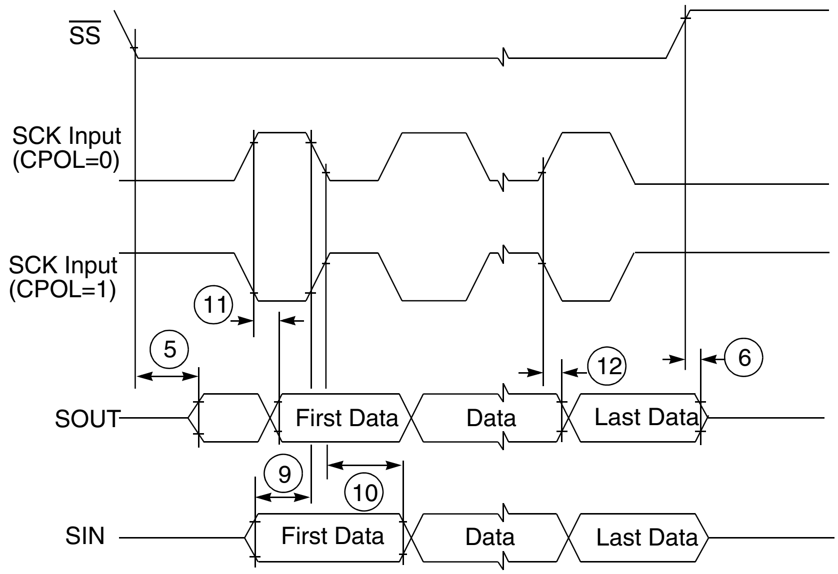



**Figure 15. DSPI modified transfer format timing — slave, CPHA = 1**

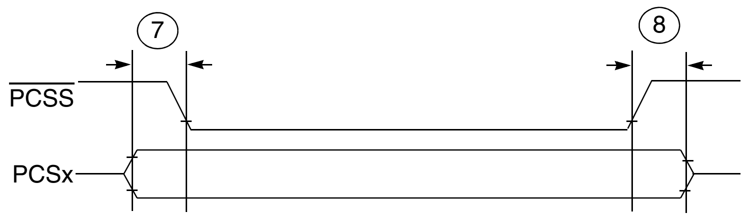



**Figure 16. DSPI PCS strobe (PCSS) timing**

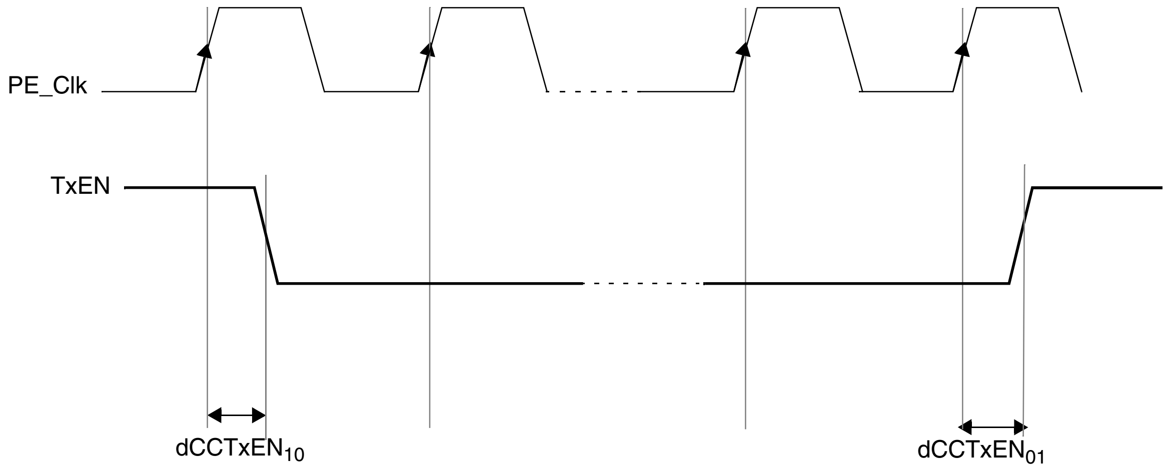



**Figure 18. TxEN signal propagation delays**

### 6.4.2.3 TxD

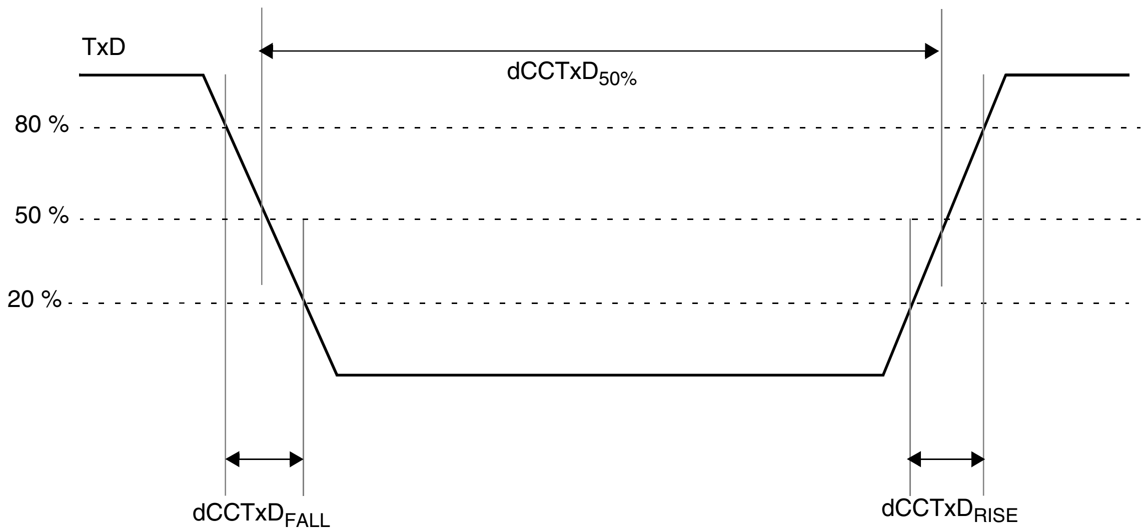



**Figure 19. TxD Signal**

**Table 39. TxD output characteristics**

| Name | Description[1] | Min | Max | Unit |
|---|---|---|---|---|
| $dCCT_{xAsym}$ | Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns) | –2.45 | 2.45 | ns |
| $dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$ | Sum of Rise and Fall time of TxD signal at the output | — | 9[2] | ns |

*Table continues on the next page...*

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = –40 oC / 150 oC.

## 6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

### 6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

**Table 41. MII signal switching specifications**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| — | RXCLK frequency | — | 25 | MHz |
| MII1 | RXCLK pulse width high | 35% | 65% | RXCLK period |
| MII2 | RXCLK pulse width low | 35% | 65% | RXCLK period |
| MII3 | RXD[3:0], RXDV, RXER to RXCLK setup | 5 | — | ns |
| MII4 | RXCLK to RXD[3:0], RXDV, RXER hold | 5 | — | ns |
| — | TXCLK frequency | — | 25 | MHz |
| MII5 | TXCLK pulse width high | 35% | 65% | TXCLK period |
| MII6 | TXCLK pulse width low | 35% | 65% | TXCLK period |
| MII7 | TXCLK to TXD[3:0], TXEN, TXER invalid | 2 | — | ns |
| MII8 | TXCLK to TXD[3:0], TXEN, TXER valid | — | 25 | ns |

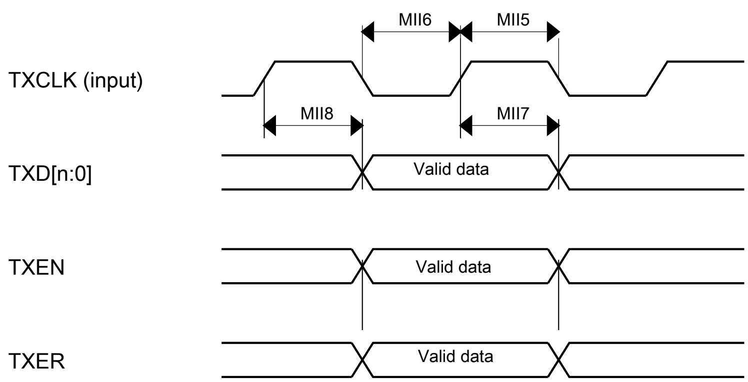



**Figure 21. RMII/MII transmit signal timing diagram**

## Table 46. Nexus debug port timing [1] (continued)

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 9 | $t_{NTDIH}$, $t_{NTMSH}$ | TDI, TMS Data Hold Time | — | 5 | — | ns |
| 10 | $t_{JOV}$ | TCK Low to TDO/RDY Data Valid | — | 0 | 25 | ns |

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

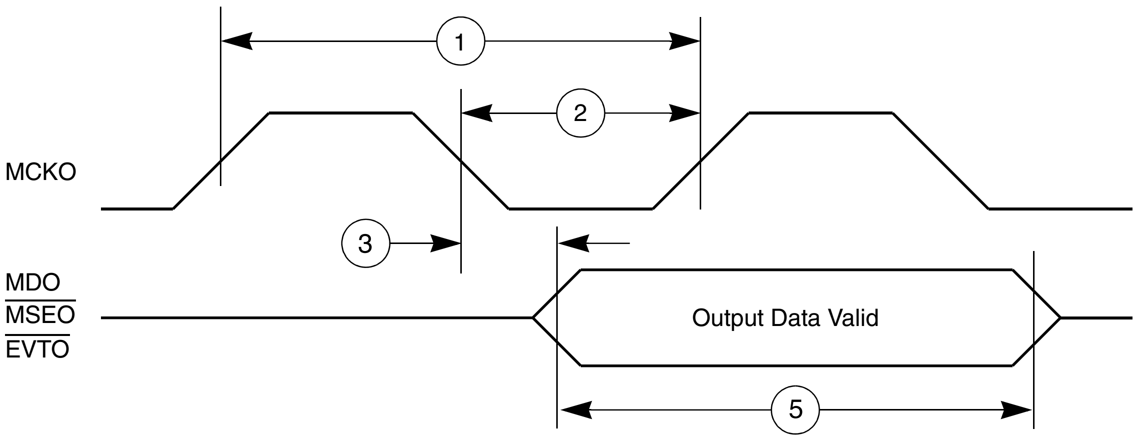



**Figure 28. Nexus output timing**

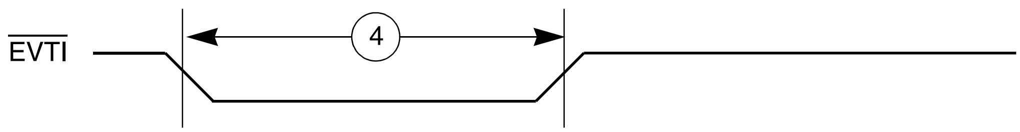



**Figure 29. Nexus EVTI Input Pulse Width**

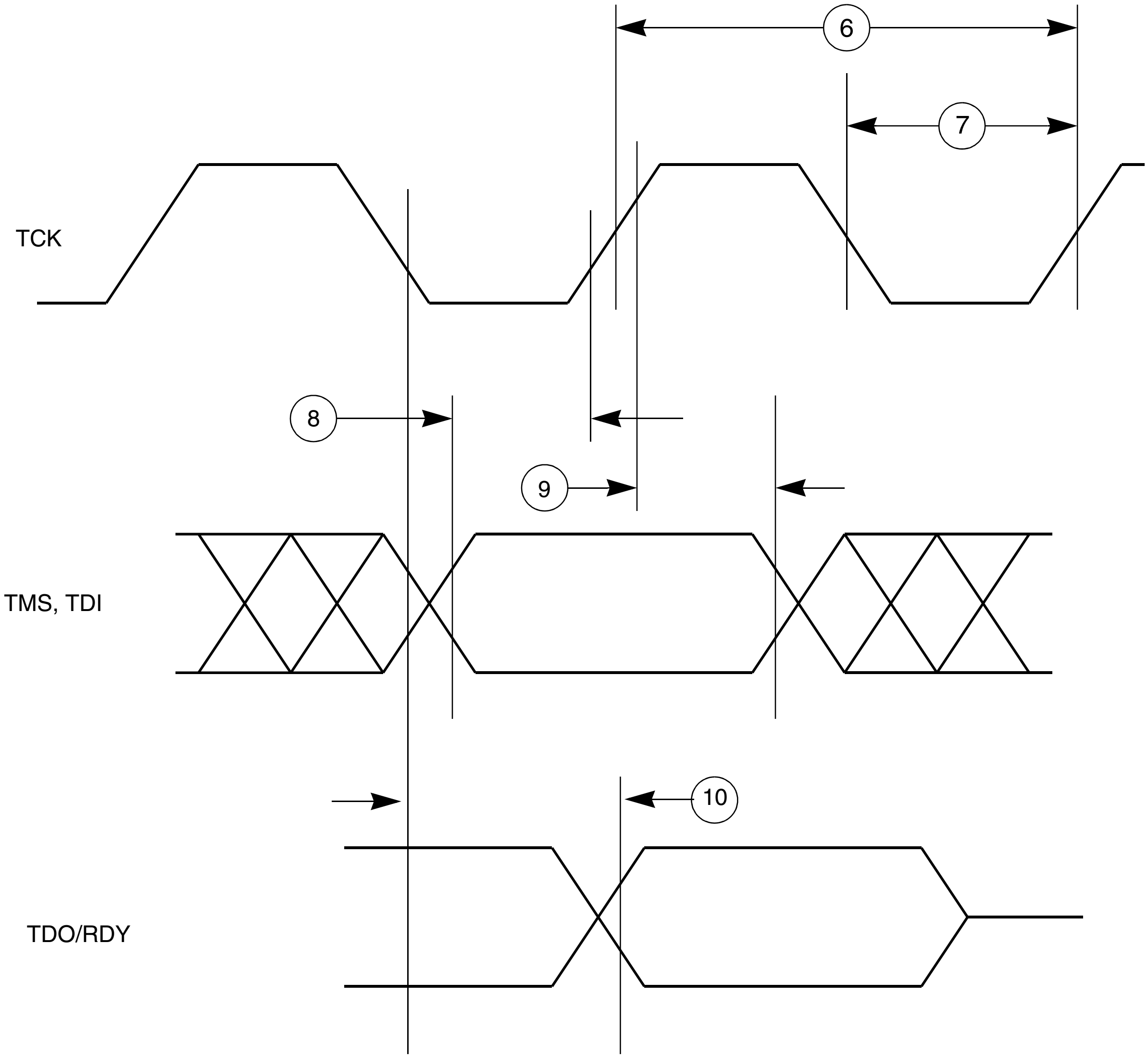



**Figure 30. Nexus TDI, TMS, TDO timing**

## 6.5.3 WKPU/NMI timing

**Table 47. WKPU/NMI glitch filter**

| No. | Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | $W_{FNMI}$ | NMI pulse width that is rejected | — | — | 20 | ns |
| 2 | $W_{NFNMI}D$ | NMI pulse width that is passed | 400 | — | — | ns |

| Board type | Symbol | Description | 324 MAPBGA | Unit | Notes |
|---|---|---|---|---|---|
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 16.8 | °C/W | 44 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 7.4 | °C/W | 55 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top natural convection | 0.2 | °C/W | 66 |
| — | $\Psi_{JB}$ | Thermal characterization parameter, junction to package bottom natural convection | 7.3 | °C/W | 77 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

| Board type | Symbol | Description | 256 MAPBGA | Unit | Notes |
|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 42.6 | °C/W | 11, 22 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 26.0 | °C/W | 1,2,33 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 31.0 | °C/W | 1,3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 21.3 | °C/W | 1,3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 12.8 | °C/W | 44 |

*Table continues on the next page...*

### 10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

**Table 50. BAF execution duration**

| BAF execution duration | Min | Typ | Max | Unit |
|---|---|---|---|---|
| BAF execution time (boot header at first location) | — | 200 | — | μs |
| BAF execution time (boot header at last location) | — | — | 320 | μs |

### 10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

**NOTE**

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

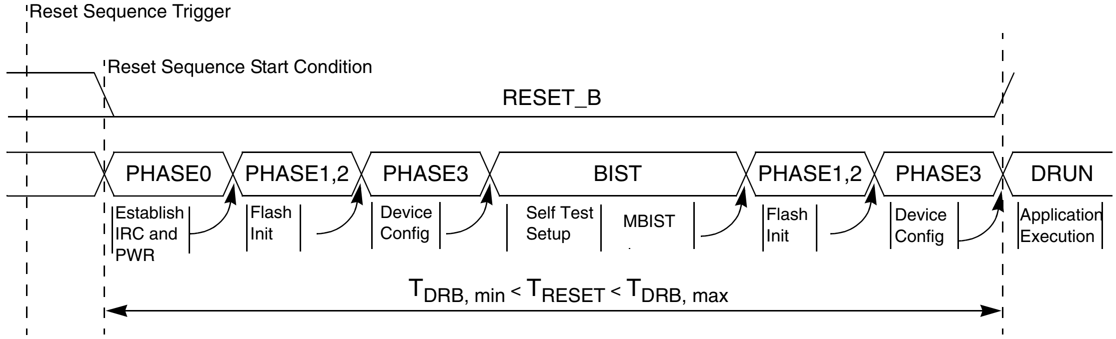



**Figure 32. Destructive reset sequence, BIST enabled**

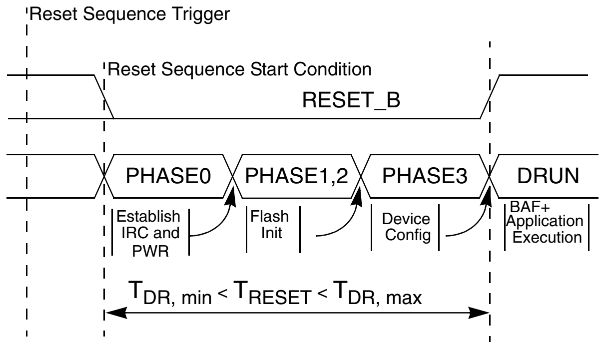



**Figure 33. Destructive reset sequence, BIST disabled**

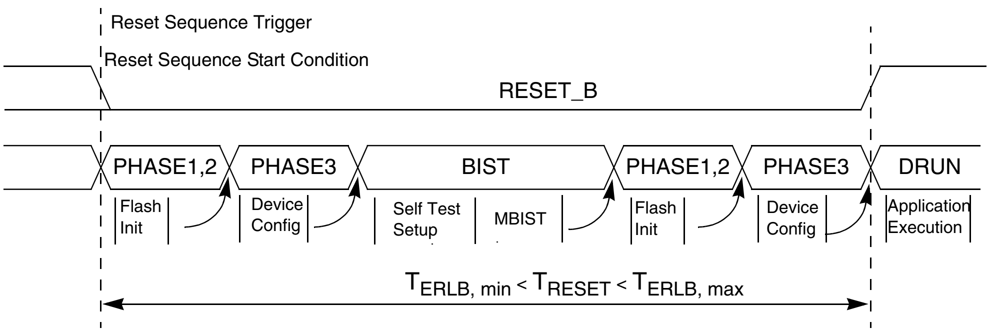



**Figure 34. External reset sequence long, BIST enabled**

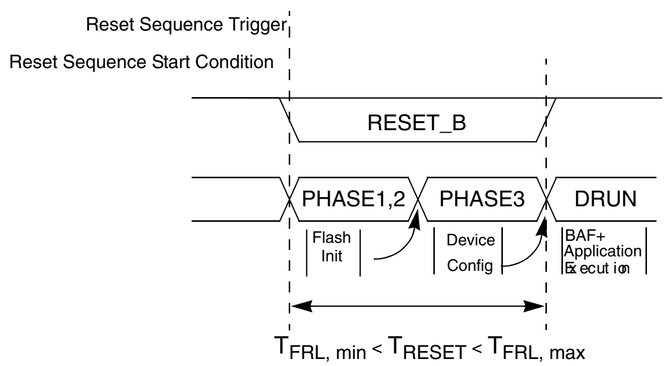



**Figure 35. Functional reset sequence long**

## Table 51. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • In section: Voltage monitor electrical characteristics<br>  • Updated description for Low Voltage detector block.<br>  • Added note, BCP56, MCP68 and MJD31 are guaranteed ballasts.<br>  • In table: Voltage regulator electrical specifications<br>    • Added footnote, Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.<br>  • Revised table, Voltage monitor electrical characteristics |
| | | • In section: Supply current characteristics<br>  • In table: Current consumption characteristics<br>    • $I_{DD\_BODY\_4}$: Updated SYS_CLK to 120 MHz.<br>    • $I_{DD\_BODY\_4}$: Updated Max for $T_a$= 105 °C fand 85 °C )<br>    • $I_{dd\_STOP}$: Added condition for $T_a$= 105 °C and removed Max value for $T_a$= 85 °C.<br>    • $I_{DD\_HV\_ADC\_REF}$: Added condition for $T_a$= 105 °C and 85 °C and removed Max value for $T_a$= 25 °C.<br>    • $I_{DD\_HV\_FLASH}$: Added condition for $T_a$= 105 °C and 85 °C<br>  • In table: Low Power Unit (LPU) Current consumption characteristics<br>    • LPU_RUN and LPU_STOP: Added condition for $T_a$= 105 °C and 85 °C<br>  • In table: STANDBY Current consumption characteristics<br>    • Added condition for $T_a$= 105 °C and 85 °C for all entries.<br><br>• In section: I/O parameters<br>  • In table: Functional Pad AC Specifications @ 3.3 V Range<br>    • Updated values for 'pad_sr_hv (output)'<br>  • In table: DC electrical specifications @ 3.3V Range<br>    • Updateded Min and Max values for Vih and Vil respectively.<br>  • In table: Functional Pad AC Specifications @ 5 V Range<br>    • Updated values for 'pad_sr_hv (output)'<br>  • In table DC electrical specifications @ 5 V Range<br>    • Updated Min value for Vhys |

*Table continues on the next page...*

## Table 51. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
| --- | --- | --- |
| Rev 3 | 2 March 2016 | • In section, Recommended operating conditions<br>• Added a new Note<br><br>• In section, Voltage regulator electrical characteristics<br>• In table, Voltage regulator electrical specifications:<br>• Added a new row for $C_{HV\_VDD\_B}$<br>• Added a footnote on $V_{DD\_HV\_BALLAST}$<br>• Added a new Note at the end of this section<br><br>• In section, Voltage monitor electrical characteristics<br>• In table, Voltage monitor electrical characteristics:<br>• Removed "$V_{LVD\_FLASH}$" and "$V_{LVD\_FLASH}$ during low power mode using LPBG as reference" rows<br>• Updated Fall and Rise trimmed Minimum values for $V_{HVD\_LV\_cold}$<br><br>• In section, Supply current characteristics<br>• In table, Current consumption characteristics:<br>• Updated the footnote mentioned in the Condition column of $I_{DD\_STOP}$ row<br>• Updated all TBD values<br>• In table, Low Power Unit (LPU) Current consumption characteristics:<br>• Updated the typical value of LPU_STOP to 0.18 mA<br>• Updated all TBD values<br>• In table, STANDBY Current consumption characteristics:<br>• Updated all TBD values<br><br>• In section, AC specifications @ 3.3 V Range<br>• In table, Functional Pad AC Specifications @ 3.3 V Range:<br>• Updated Rise/Fall Edge values<br><br>• In section, DC electrical specifications @ 3.3V Range<br>• In table, DC electrical specifications @ 3.3V Range:<br>• Updated Max value for Vol to 0.1 * VDD_HV_x<br><br>• In section, AC specifications @ 5 V Range<br>• In table, Functional Pad AC Specifications @ 5 V Range:<br>• Updated Rise/Fall Edge values<br><br>• In section, DC electrical specifications @ 5 V Range<br>• In table, DC electrical specifications @ 5 V Range:<br>• Updated Min and Max values for Pull_Ioh and Pull_Iol rows<br>• Updated Max value for Vol to 0.1 * VDD_HV_x<br><br>• In section, Reset pad electrical characteristics<br>• In table, Functional reset pad electrical specifications:<br>• Updated parameter column for $V_{IH}$, $V_{IL}$ and $V_{HYS}$ rows<br>• Updated Min and Max values for $V_{IH}$ and $V_{IL}$ rows<br><br>• In section, PORST electrical specifications<br>• In table, PORST electrical specifications:<br>• Updated Unit and Min/Max values for $V_{IH}$ and $V_{IL}$ rows<br><br>• In section, Input equivalent circuit and ADC conversion characteristics<br>• In table, ADC conversion characteristics (for 12-bit):<br>• Updated "ADC Analog Pad (pad going to one ADC)" row<br>• In table, ADC conversion characteristics (for 10-bit):<br>• Updated "ADC Analog Pad (pad going to one ADC)" row<br><br>• In section, Analog Comparator (CMP) electrical specifications<br>• In table, Comparator and 6-bit DAC electrical specifications:<br>• Updated Min and Max values for $V_{AIO}$ to ±47 mV<br>• Updated Max value for $t_{DLS}$ to 21 µs<br><br>• In section, Main oscillator electrical characteristics<br>• In table, Main oscillator electrical characteristics: |