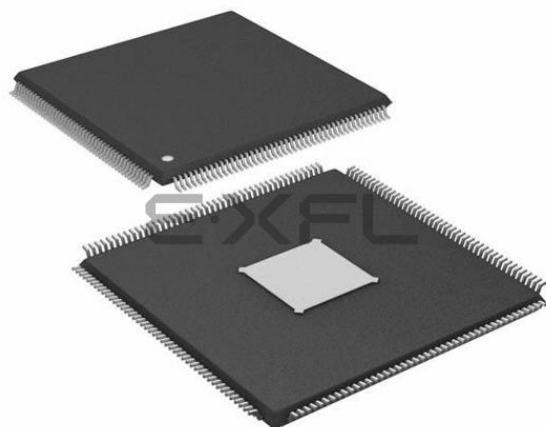




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746ck1amku2r

NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest number or address (e.g., FlexCAN0) and end at highest available number or address (e.g., MPC574xB/C have 6 CAN, ending with FlexCAN5).

Table 1. MPC5746C Family Comparison¹

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C
CPU	e200z4	e200z4	e200z4	e200z4 e200z2	e200z4 e200z2	e200z4 e200z2
FPU	e200z4	e200z4	e200z4	e200z4	e200z4	e200z4
Maximum Operating Frequency ²	160MHz (Z4)	160MHz (Z4)	160MHz (Z4)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)
Flash memory	2 MB	1.5 MB	3 MB	1.5 MB	2 MB	3 MB
EEPROM support	Emulated up to 64K			Emulated up to 64K		
RAM	256 KB	192 KB	384 KB (Optional 512KB) ^{3, 3}	192 KB	256 KB	384 KB (Optional 512KB) ³
ECC	End to End					
SMPU	16 entry					
DMA	32 channels					
10-bit ADC	36 Standard channels 32 External channels					
12-bit ADC	15 Precision channels 16 Standard channels					
Analog Comparator	3					
BCTU	1					
SWT	1, SWT[0] ⁴			2 ⁴		
STM	1, STM[0]			2		
PIT-RTI	16 channels PIT 1 channels RTI					
RTC/API	1					
Total Timer I/O ⁵	64 channels 16-bits					
LINFlexD	1 Master and Slave (LINFlexD[0], 11 Master (LINFlexD[1:11]))			1 Master and Slave (LINFlexD[0], 15 Master (LINFlexD[1:15]))		
FlexCAN	6 with optional CAN FD support (FlexCAN[0:5])			8 with optional CAN FD support (FlexCAN[0:7])		
DSPI/SPI	4 x DSPI 4 x SPI					

Table continues on the next page...

Table 2. MPC5746C Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW partition	MPC5744	MPC5745	MPC5746
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	not available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	7	not available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	7	not available	not available	available
0x011C0000	0x011FFFFFFF	256 KB code Flash block 7	7	not available	not available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	not available	not available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	not available	not available	not available

Table 3. MPC5746C Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW partition	MPC5744B MPC5745B MPC5746B	MPC5744C MPC5745C MPC5746C
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	not available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	not available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	not available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	not available	available

Table 4. MPC5746C Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40000000	0x40001FFF	8 KB	SRAM0	available	available	available
0x40002000	0x4000FFFF	56 KB	SRAM1	available	available	available
0x40010000	0x4001FFFF	64 KB	SRAM2	available	available	available
0x40020000	0x4002FFFF	64 KB	SRAM3	available	available	available

Table continues on the next page...

3.2 Ordering Information

Example Code	P	PC	57	4	6	C	S	K0	M	MJ	6	R
Qualification Status												
Power Architecture												
Automotive Platform												
Core Version												
Flash Size (core dependent)												
Product												
Optional fields												
Fab and mask indicator												
Temperature spec.												
Package Code												
CPU Frequency												
R = Tape & Reel (blank if Tray)												

Qualification Status P = Engineering samples S = Automotive qualified PC = Power Architecture	Product Version B = Single core C = Dual core	Fab and mask version indicator K = TSMC Fab #(0,1,etc.) = Version of the maskset, like rev. 0=0N65H	Package Code KU = 176 LQFP EP MJ = 256 MAPBGA MN = 324 MAPBGA MH = 100MAPBGA
Automotive Platform 57 = Power Architecture in 55nm	Optional fields Blank = No optional feature S = HSM (Security Module) F = CAN FD B = HSM + CAN FD R = 512K RAM T = HSM + 512K RAM G* = CAN FD + 512K RAM H* = HSM + CAN FD + 512K RAM * G and H for 5746 B/C only	Temperature spec. C = -40.C to +85.C Ta V = -40.C to +105.C Ta M = -40.C to +125.C Ta	CPU Frequency 2 = Z4 operates upto 120 MHz 6 = Z4 operates upto 160 MHz
Core Version 4 = e200z4 Core Version (highest core version in the case of multiple cores)			Shipping Method R = Tape and reel Blank = Tray
Flash Memory Size 4 = 1.5 MB 5 = 2 MB 6 = 3 MB			

Note: Not all part number combinations are available as production product

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in [Table 5](#) for specific conditions

Table 6. Recommended operating conditions ($V_{DD_HV_x} = 3.3\text{ V}$) (continued)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
T_A ⁸	Ambient temperature under bias	$f_{CPU} \leq 160\text{ MHz}$	-40	125	°C
T_J	Junction temperature under bias	—	-40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. $V_{DD_HV_FLA}$ must be connected to $V_{DD_HV_A}$ when $V_{DD_HV_A} = 3.3\text{ V}$
4. Only applicable when supplying from external source.
5. V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
6. $V_{IN1_CMP_REF} \leq V_{DD_HV_A}$
7. This supply is shorted $V_{DD_HV_A}$ on lower packages.
8. $T_J = 150^\circ\text{C}$. Assumes $T_A = 125^\circ\text{C}$
 - Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#)

NOTE

If $V_{DD_HV_A}$ is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. $V_{DD_HV_FLA}$ should not be supplied externally and should only have decoupling capacitor.

Table 7. Recommended operating conditions ($V_{DD_HV_x} = 5\text{ V}$)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
$V_{DD_HV_A}$ $V_{DD_HV_B}$ $V_{DD_HV_C}$	HV IO supply voltage	—	4.5	5.5	V
$V_{DD_HV_FLA}$ ³	HV flash supply voltage	—	3.15	3.6	V
$V_{DD_HV_ADC1_REF}$	HV ADC1 high reference voltage	—	3.15	5.5	V
$V_{DD_HV_ADC0}$ $V_{DD_HV_ADC1}$	HV ADC supply voltage	—	$\max(V_{DD_H_V_A}, V_{DD_H_V_B}, V_{DD_H_V_C}) - 0.05$	5.5	V
$V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV} ⁴	Core supply voltage	—	1.2	1.32	V
$V_{IN1_CMP_REF}$ ^{5, 6}	Analog Comparator DAC reference voltage	—	3.15	5.5 ⁵	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_A ⁷	Ambient temperature under bias	$f_{CPU} \leq 160\text{ MHz}$	-40	125	°C
T_J	Junction temperature under bias	—	-40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. When V_{DD_HV} is in 5 V range, $V_{DD_HV_FLA}$ cannot be supplied externally. This pin is decoupled with C_{flash_reg} .

Table 8. Voltage regulator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{\text{flash_reg}}$ ⁴	External decoupling / stability capacitor for internal Flash regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2	3	μF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
$C_{\text{HV_VDD_A}}$	VDD_HV_A supply capacitor ^{5, 5}	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_VDD_B}}$	VDD_HV_B supply capacitor ⁵	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_VDD_C}}$	VDD_HV_C supply capacitor ⁵	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_ADC0}}$ $C_{\text{HV_ADC1}}$	HV ADC supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_ADR}}$ ⁶	HV ADC SAR reference supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.47	—	—	μF
$V_{\text{DD_HV_BALLAST}}^{\text{AST}}$ ⁷	FPREG Ballast collector supply voltage	When collector of NPN ballast is directly supplied by an on board supply source (not shared with VDD_HV_A supply pin) without any series resistance, that is, $R_{\text{C_BALLAST}}$ less than 0.01 Ohm.	2.25	—	5.5	V
$R_{\text{C_BALLAST}}$	Series resistor on collector of FPREG ballast	When VDD_HV_BALLAST is shorted to VDD_HV_A on the board	—	—	0.1	Ohm
t_{SU}	Start-up time with external ballast after main supply (VDD_HV_A) stabilization	$C_{\text{fp_reg}} = 3 \mu\text{F}$	—	74	—	μs
$t_{\text{SU_int}}$	Start-up time with internal ballast after main supply (VDD_HV_A) stabilization	$C_{\text{fp_reg}} = 3 \mu\text{F}$	—	103	—	μs
t_{ramp}	Load current transient	Iload from 15% to 55% $C_{\text{fp_reg}} = 3 \mu\text{F}$		1.0		μs

1. Split capacitance on each pair VDD_LV pin should sum up to a total value of $C_{\text{fp_reg}}$
2. Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.
3. Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
4. It is required to minimize the board parasitic inductance from decoupling capacitor to VDD_HV_FL A pin and the routing inductance should be less than 1nH.

5.2 DC electrical specifications @ 3.3V Range

Table 15. DC electrical specifications @ 3.3V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	Pad_I_HV Input Buffer High Voltage	$0.72 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil (pad_i_hv)	Pad_I_HV Input Buffer Low Voltage	$VDD_HV_x - 0.3$	$0.45 \cdot VDD_HV_x$	V
Vhys (pad_i_hv)	Pad_I_HV Input Buffer Hysteresis	$0.11 \cdot VDD_HV_x$		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	$0.67 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	$VDD_HV_x - 0.3$	$0.35 \cdot VDD_HV_x$	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	$0.57 \cdot VDD_HV_x^{1,1}$	$VDD_HV_x^{1,1} + 0.3$	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	$VDD_HV_x - 0.3$	$0.4 \cdot VDD_HV_x^{1,1}$	V
Vhys	CMOS Input Buffer Hysteresis	$0.09 \cdot VDD_HV_x^{1,1}$		V
Pull_IH (pad_i_hv)	Weak Pullup Current ^{2,2} Low	15		μA
Pull_IH (pad_i_hv)	Weak Pullup Current ^{3,3} High		55	μA
Pull_IL (pad_i_hv)	Weak Pulldown Current ³ Low	28		μA
Pull_IL (pad_i_hv)	Weak Pulldown Current ² High		85	μA
Pull_Ioh	Weak Pullup Current ⁴	15	50	μA
Pull_Iol	Weak Pulldown Current ⁵	15	50	μA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	μA
Voh	Output High Voltage ⁶	$0.8 \cdot VDD_HV_x^{1,1}$	—	V
Vol	Output Low Voltage ⁷ Output Low Voltage ⁸	—	$0.2 \cdot VDD_HV_x^{1,1}$ $0.1 \cdot VDD_HV_x$	V
Ioh_f	Full drive Ioh ^{9,9} (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol ⁹ (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh ⁹ (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol ⁹ (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

1. $VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C$

2. Measured when pad = $0.69 \cdot VDD_HV_x$

3. Measured when pad = $0.49 \cdot VDD_HV_x$

4. Measured when pad = 0 V

5. Measured when pad = VDD_HV_x

6. Measured when pad is sourcing 2 mA

7. Measured when pad is sinking 2 mA

8. Measured when pad is sinking 1.5 mA

9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

Table 18. Functional reset pad electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{HYS}	CMOS Input Buffer hysteresis	—	300	—	—	mV
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current ^{1, 1}	Device under power-on reset $V_{DD_HV_A} = V_{DD_POR}$ $V_{OL} = 0.35 \times V_{DD_HV_A}$	0.2	—	—	mA
		Device under power-on reset $V_{DD_HV_A} = V_{DD_POR}$ $V_{OL} = 0.35 \times V_{DD_HV_IO}$	11	—	—	mA
W_{FRST}	RESET input filtered pulse	—	—	—	500	ns
W_{NFRST}	RESET input not filtered pulse	—	2000	—	—	ns
I_{WPUL}	Weak pull-up current absolute value	RESET pin $V_{IN} = V_{DD}$	23	—	82	μA

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	PORST input filtered pulse	—	—	200	ns
$W_{NFPORST}$	PORST input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	0.65 x $V_{DD_HV_A}$	—	—	V
V_{IL}	Input low level	—	—	0.35 x $V_{DD_HV_A}$	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

6.1.1.1 Input equivalent circuit and ADC conversion characteristics

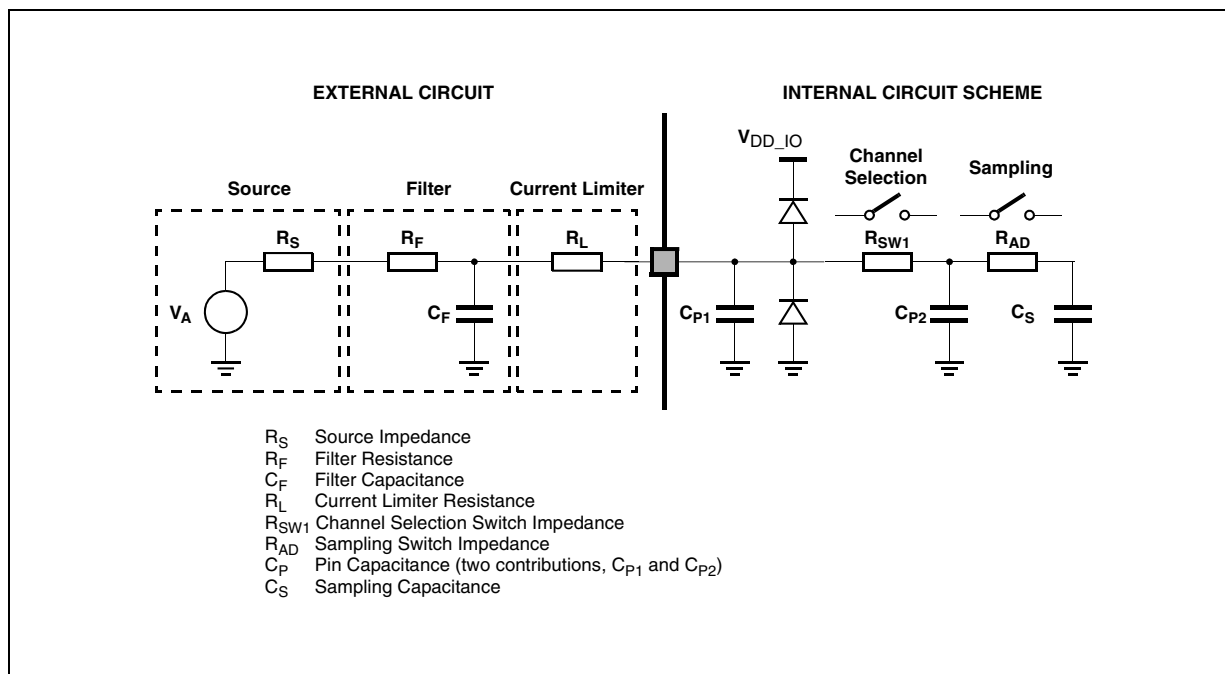


Figure 6. Input equivalent circuit

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

Table 20. ADC conversion characteristics (for 12-bit)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK ² frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1.00	MHz
t_{sample}	Sample time ³	80 MHz @ 100 ohm source impedance	250	—	—	ns
t_{conv}	Conversion time ⁴	80 MHz	700	—	—	ns
t_{total_conv}	Total Conversion time $t_{sample} + t_{conv}$ (for standard and extended channels)	80 MHz	1.5 ⁵	—	—	μs
	Total Conversion time $t_{sample} + t_{conv}$ (for precision channels)		1	—	—	
$C_S^{6, 6}$	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}^6	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}^6	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}^6	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	k Ω
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω

Table continues on the next page...

6.1.2 Analog Comparator (CMP) electrical specifications

Table 22. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	μA
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	μA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1_CMP_REF}$	V
V_{AIO}	Analog input offset voltage ^{1, 1}	-47	—	47	mV
V_H	Analog comparator hysteresis ^{2, 2} - CR0[HYSTCTR] = 00 - CR0[HYSTCTR] = 01 - CR0[HYSTCTR] = 10 - CR0[HYSTCTR] = 11	—	1	25	mV
		—	20	50	mV
		—	40	70	mV
		—	60	105	mV
		—	—	—	—
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) ^{1, 3, 3}	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) ^{1, 3}	—	5	21	μs
	Analog comparator initialization delay, High speed mode ^{4, 4}	—	4		μs
	Analog comparator initialization delay, Low speed mode ⁴	—	100		μs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	μA
	5V Reference Voltage	—	10	16	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ⁵
DNL	6-bit DAC differential non-linearity	-0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD_HV_A}-0.6V$
3. Full swing = V_{IH} , V_{IL}
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

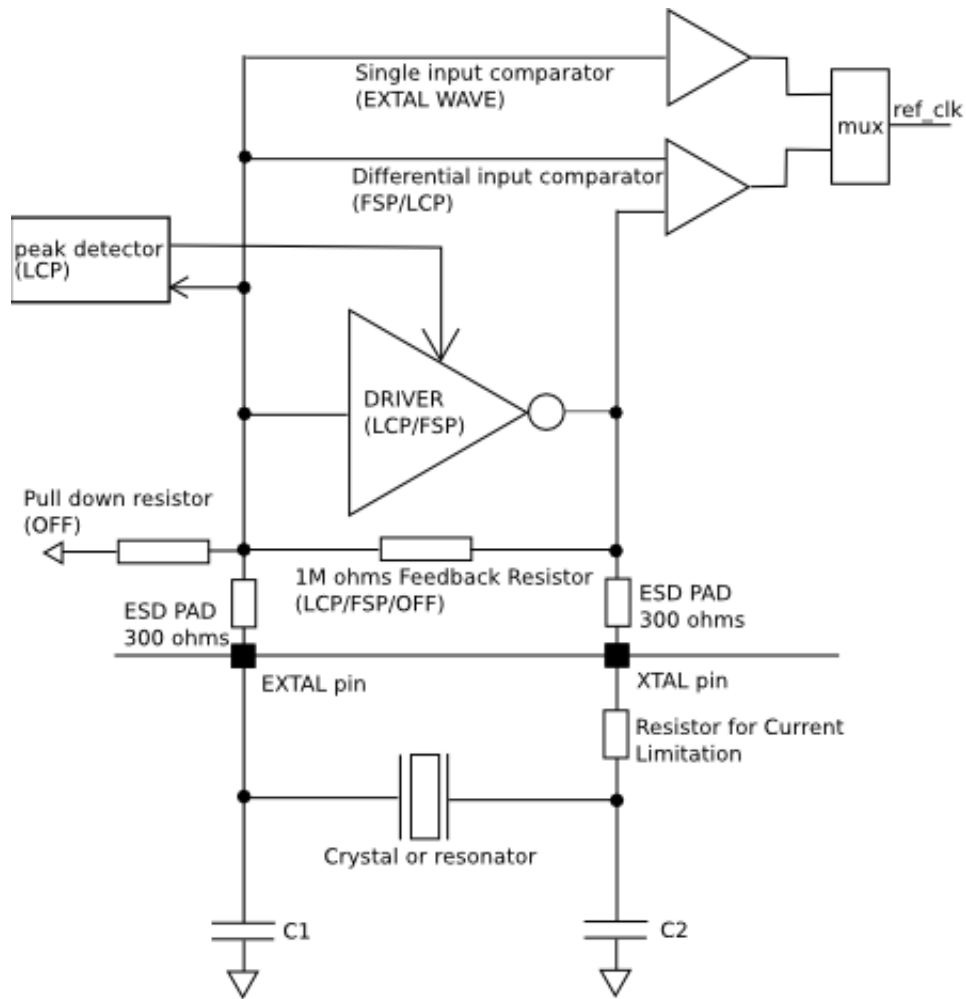


Figure 7. Oscillator connections scheme

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	LCP			23		mA/V
		FSP			33		
V_{XOSCHS}	Oscillation Amplitude	LCP ^{1, 2, 1, 2}	8 MHz		1.0		V_{PP}
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP ¹	8 MHz		2		ms
			16 MHz		1		
			40 MHz		0.5		

Table continues on the next page...

Table 30. Flash memory program and erase specifications

Symbol	Characteristic ¹	Typ ²	Factory Programming ^{3, 4}		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life ⁵	Lifetime Max ⁶		
						20°C ≤T _A ≤30°C	-40°C ≤T _J ≤150°C	
t _{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		μs
t _{ppgm}	Page (256 bits) program time	73	200	300	108	500		μs
t _{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		μs
t _{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t _{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t _{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t _{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t _{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t _{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
t _{256kers}	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
t _{256kpgm}	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programming times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max ^{1, 1}	Units ^{2, 2}
t _{ai16kseq}	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x T _{period} x N _{read}	—
t _{ai32kseq}	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x T _{period} x N _{read}	—
t _{ai64kseq}	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x T _{period} x N _{read}	—

Table continues on the next page...

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	μs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	μs

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 34. Flash Read Wait State and Address Pipeline Control Combinations

Flash frequency	RWSC setting	APC setting
0 MHz < fFlash <= 33 MHz	0	0
33 MHz < fFlash <= 100 MHz	2	1
100 MHz < fFlash <= 133 MHz	3	1
133 MHz < fFlash <= 160 MHz	4	1

Table 35. DSPI electrical specifications (continued)

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	NA	—	-2	—	ns
			Slave	4	—	6	—	
			Master (MTFE = 1, CPHA = 0)	-2	—	10 ¹	—	
			Master (MTFE = 1, CPHA = 1)	-2	—	-2	—	

1. SMPL_PTR should be set to 1

NOTE

Restriction For High Speed modes

- DSPI2, DSPI3, SPI1 and SPI2 will support 40MHz Master mode SCK
- DSPI2, DSPI3, SPI1 and SPI2 will support 25MHz Slave SCK frequency
- Only one {SIN,SOUT and SCK} group per DSPI/SPI will support high frequency mode
- For Master mode MTFE will be 1 for high speed mode
- For high speed slaves, their master have to be in MTFE=1 mode or should be able to support 15ns tSUO delay

NOTE

For numbers shown in the following figures, see [Table 35](#)

Table 36. Continuous SCK timing

Spec	Characteristics	Pad Drive/Load	Value	
			Min	Max
tSCK	SCK cycle timing	strong/50 pF	100 ns	-
-	PCS valid after SCK	strong/50 pF	-	15 ns
-	PCS valid after SCK	strong/50 pF	-4 ns	-

Table 37. DSPI high speed mode I/Os

DSPI	High speed SCK	High speed SIN	High speed SOUT
DSPI2	GPIO[78]	GPIO[76]	GPIO[77]
DSPI3	GPIO[100]	GPIO[101]	GPIO[98]
SPI1	GPIO[173]	GPIO[175]	GPIO[176]
SPI2	GPIO[79]	GPIO[110]	GPIO[111]

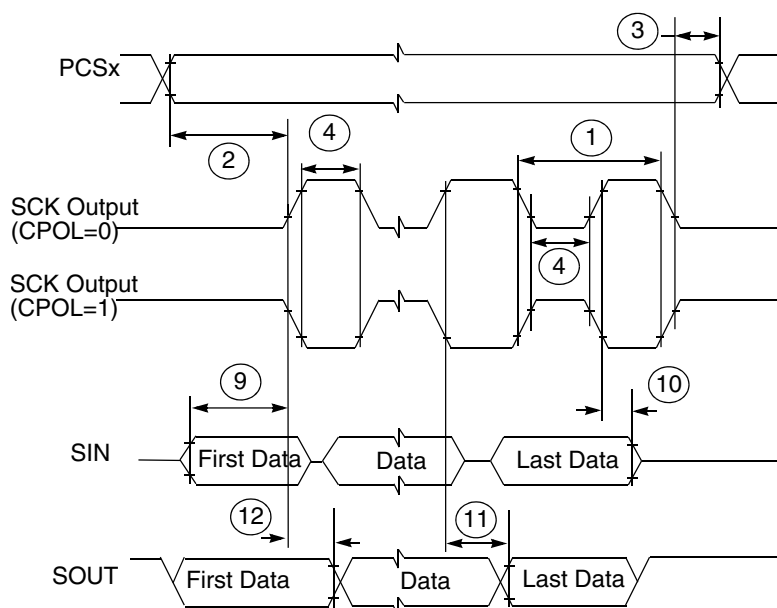


Figure 12. DSPI modified transfer format timing — master, CPHA = 0

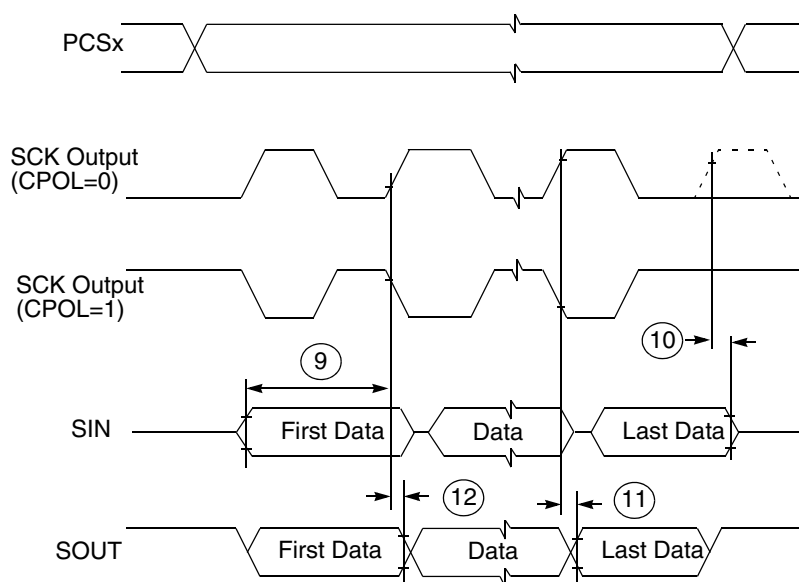


Figure 13. DSPI modified transfer format timing — master, CPHA = 1

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = -40 oC / 150 oC.

6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 41. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

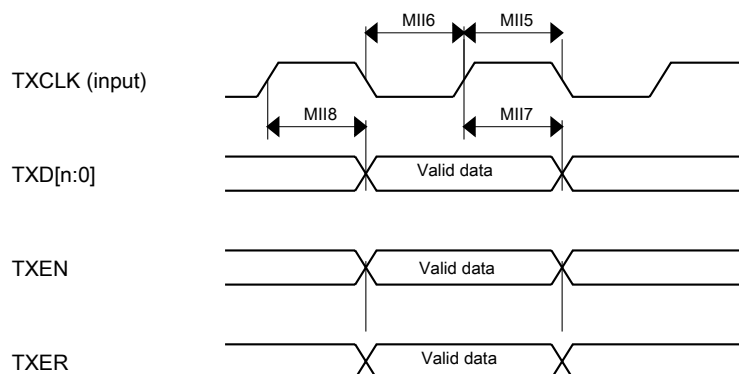


Figure 21. RMII/MII transmit signal timing diagram

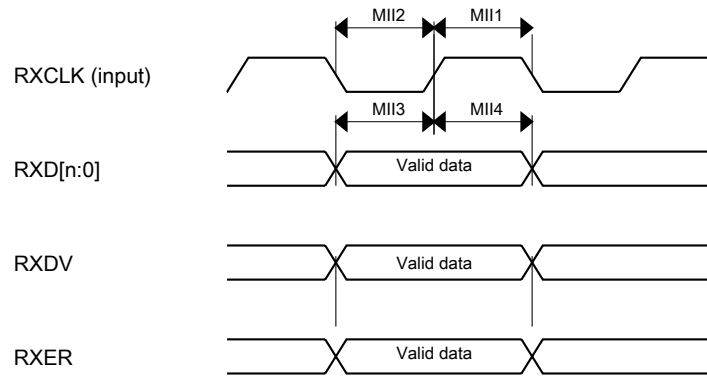


Figure 22. RMII/MII receive signal timing diagram

6.4.3.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 42. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

6.4.4 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 43. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns

Table continues on the next page...

Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	17.8	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.9	°C/W	44
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.4	°C/W	55
—	Ψ_{JT}	Thermal resistance, junction to package top	0.5	°C/W	66
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom	0.3	°C/W	77

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	31.0	°C/W	11, 22
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	24.3	°C/W	1,2,33
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	23.5	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	20.1	°C/W	1,3

Table continues on the next page...

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	16.8	°C/W	44
—	$R_{\theta JC}$	Thermal resistance, junction to case	7.4	°C/W	55
—	Ψ_{JT}	Thermal characterization parameter, junction to package top natural convection	0.2	°C/W	66
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom natural convection	7.3	°C/W	77

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	42.6	°C/W	11, 22
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	26.0	°C/W	1,2,33
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	31.0	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	21.3	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	12.8	°C/W	44

Table continues on the next page...

Reset sequence

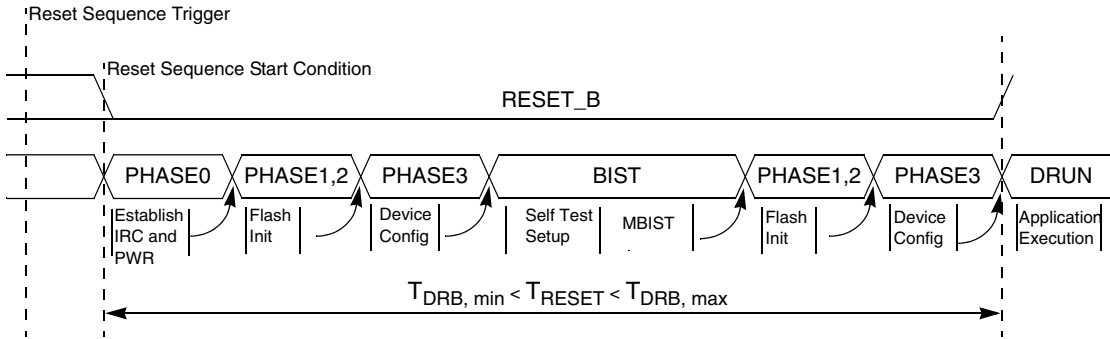


Figure 32. Destructive reset sequence, BIST enabled

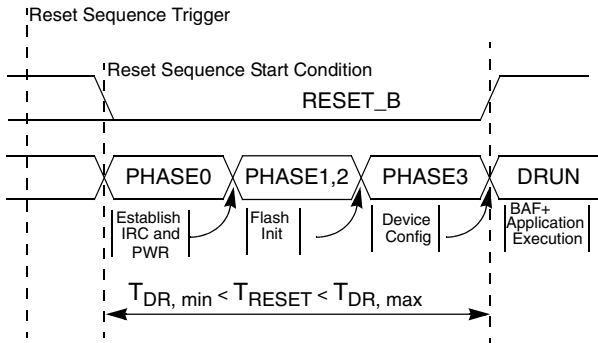


Figure 33. Destructive reset sequence, BIST disabled

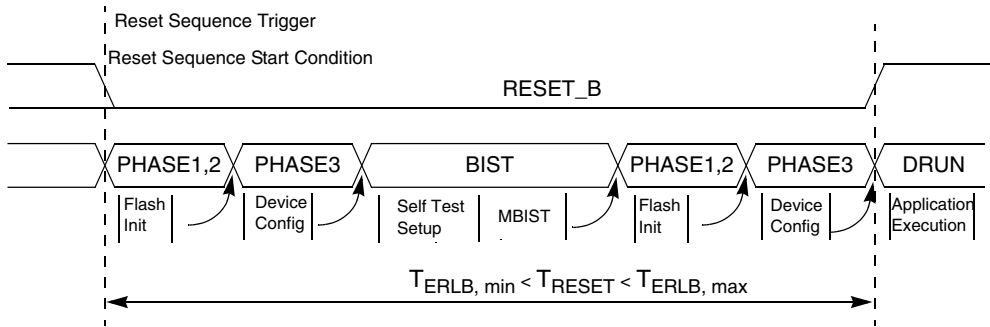


Figure 34. External reset sequence long, BIST enabled

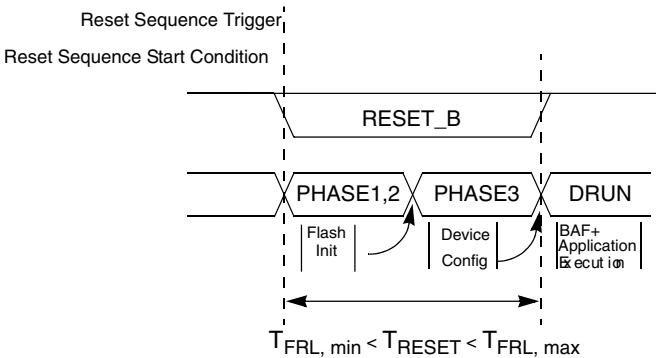


Figure 35. Functional reset sequence long

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev 4	9 March 2016	- In section, Voltage regulator electrical characteristics - In table, Voltage regulator electrical specifications: - Updated the footnote on $V_{DD_HV_BALLAST}$
Rev 5	27 February 2017	- In Family Comparison section: - Updated the "MPC5746C Family Comparison" table. - added "NVM Memory Map 1", "NVM Memory Map 2", and "RAM Memory Map" tables. - Updated the product version, flash memory size and optional fields information in Ordering Information section. - In Recommended Operating Conditions section, removed the note related to additional crossover current. - VDD_HV_C row added in "Voltage regulator electrical specifications" table in Voltage regulator electrical characteristics section. - In Voltage Monitor Electrical Characteristics section, updated the "Trimmed" Fall and Rise specs of VHVD_LV_cold parameter in "Voltage Monitor Electrical Characteristics" table. - In AC Electrical Specifications: 3.3 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. - In DC Electrical Specifications: 3.3 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" and updated "Vol min and max" values in the table. - In AC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. - In DC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" and updated "Vol min and max" values in the table. - In "Flash memory AC timing specifications" table in Flash memory AC timing specifications section: - Updated the "t_{psus}" typ value from 7 us to 9.4 us. - Updated the "t_{psus}" max value from 9.1 us to 11.5 us. - Added "Continuous SCK Timing" table in DSPI timing section. - Added "ADC pad leakage" at 105°C TA conditions in "ADC conversion characteristics (for 12-bit)" table in ADC electrical specifications section. - In "STANDBY Current consumption characteristics" table in Supply current characteristics section: - Updated the Typ and max values of IDD Standby current. - Added IDD Standby3 current spec for FIRC ON. - Removed IVDDHV and IVDDLv specs in 16 MHz RC Oscillator electrical specifications section. - Added Reset Sequence section, with Reset Sequence Duration, BAF execution duration section, and Reset Sequence Distribution as its sub-sections.

Table continues on the next page...