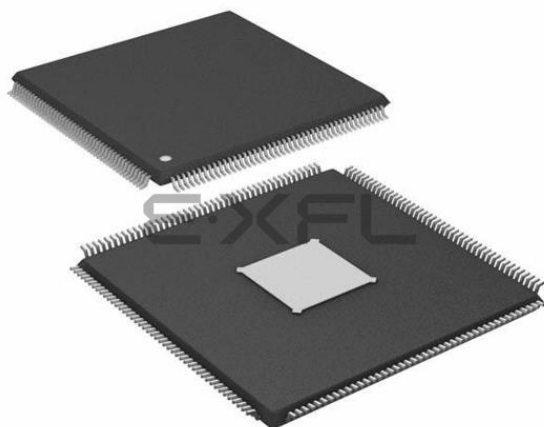




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746ck1amku6r

NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest number or address (e.g., FlexCAN0) and end at highest available number or address (e.g., MPC574xB/C have 6 CAN, ending with FlexCAN5).

Table 1. MPC5746C Family Comparison¹

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C
CPU	e200z4	e200z4	e200z4	e200z4 e200z2	e200z4 e200z2	e200z4 e200z2
FPU	e200z4	e200z4	e200z4	e200z4	e200z4	e200z4
Maximum Operating Frequency ²	160MHz (Z4)	160MHz (Z4)	160MHz (Z4)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)
Flash memory	2 MB	1.5 MB	3 MB	1.5 MB	2 MB	3 MB
EEPROM support	Emulated up to 64K			Emulated up to 64K		
RAM	256 KB	192 KB	384 KB (Optional 512KB) ^{3, 3}	192 KB	256 KB	384 KB (Optional 512KB) ³
ECC	End to End					
SMPU	16 entry					
DMA	32 channels					
10-bit ADC	36 Standard channels 32 External channels					
12-bit ADC	15 Precision channels 16 Standard channels					
Analog Comparator	3					
BCTU	1					
SWT	1, SWT[0] ⁴			2 ⁴		
STM	1, STM[0]			2		
PIT-RTI	16 channels PIT 1 channels RTI					
RTC/API	1					
Total Timer I/O ⁵	64 channels 16-bits					
LINFlexD	1 Master and Slave (LINFlexD[0], 11 Master (LINFlexD[1:11]))			1 Master and Slave (LINFlexD[0], 15 Master (LINFlexD[1:15]))		
FlexCAN	6 with optional CAN FD support (FlexCAN[0:5])			8 with optional CAN FD support (FlexCAN[0:7])		
DSPI/SPI	4 x DSPI 4 x SPI					

Table continues on the next page...

Table 2. MPC5746C Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW partition	MPC5744	MPC5745	MPC5746
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	not available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	7	not available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	7	not available	not available	available
0x011C0000	0x011FFFFFFF	256 KB code Flash block 7	7	not available	not available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	not available	not available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	not available	not available	not available

Table 3. MPC5746C Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW partition	MPC5744B MPC5745B MPC5746B	MPC5744C MPC5745C MPC5746C
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	not available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	not available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	not available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	not available	available

Table 4. MPC5746C Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40000000	0x40001FFF	8 KB	SRAM0	available	available	available
0x40002000	0x4000FFFF	56 KB	SRAM1	available	available	available
0x40010000	0x4001FFFF	64 KB	SRAM2	available	available	available
0x40020000	0x4002FFFF	64 KB	SRAM3	available	available	available

Table continues on the next page...

Table 4. MPC5746C Family Comparison - RAM Memory Map (continued)

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40030000	0x4003FFFF	64 KB	SRAM4	not available	available	available
0x40040000	0x4004FFFF	64 KB	SRAM5	not available	not available	available
0x40050000	0x4005FFFF	64 KB	SRAM6	not available	not available	available
0x40060000	0x4006FFFF	64 KB	SRAM7	not available	not available	optional
0x40070000	0x4007FFFF	64 KB	SRAM8	not available	not available	optional

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5746C.

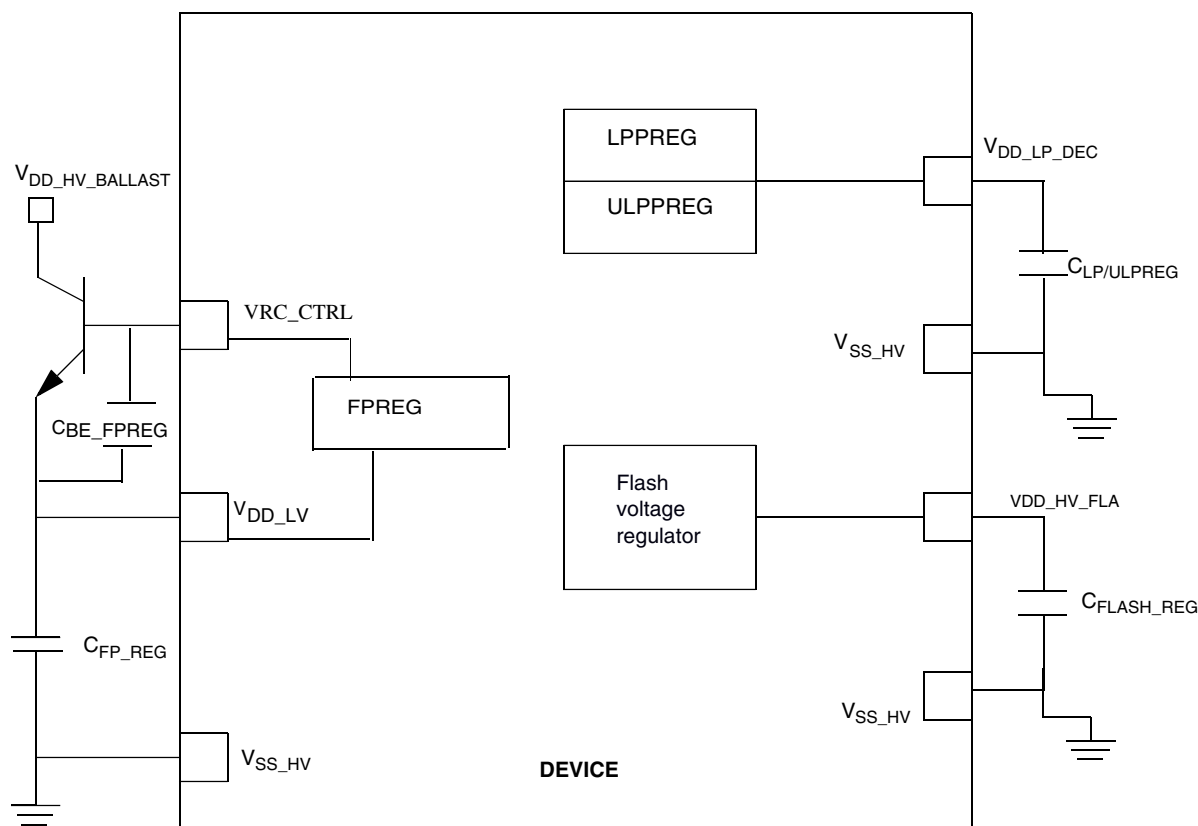


Figure 2. Voltage regulator capacitance connection

NOTE

On BGA, VSS_LV and VSS_HV have been joined on substrate and renamed as VSS.

Table 8. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _{fp_reg} ¹	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2 ²	3	μF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
C _{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	μF
	Combined ESR of external capacitor	—	0.001	—	0.1	Ohm
C _{be_fpreg} ³	Capacitor in parallel to base-emitter	BCP68 and BCP56		3.3		nF
		MJD31		4.7		

Table continues on the next page...

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
$I_{DD_HV_ADC_REF}$ ^{10, 11, 11}	ADC REF Operating current	$T_a = 125\text{ }^{\circ}\text{C}$ ⁵ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 5.5\text{ V}$	—	200	400	μA
		$T_a = 105\text{ }^{\circ}\text{C}$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 5.5\text{ V}$	—	200	—	
		$T_a = 85\text{ }^{\circ}\text{C}$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 5.5\text{ V}$	—	200	—	
		$T_a = 25\text{ }^{\circ}\text{C}$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 3.6\text{ V}$	—	200	—	
$I_{DD_HV_ADCx}$ ¹¹	ADC HV Operating current	$T_a = 125\text{ }^{\circ}\text{C}$ ⁵ ADC operating at 80 MHz $V_{DD_HV_ADC} = 5.5\text{ V}$	—	1.2	2	mA
		$T_a = 25\text{ }^{\circ}\text{C}$ ADC operating at 80 MHz $V_{DD_HV_ADC} = 3.6\text{ V}$	—	1	2	
$I_{DD_HV_FLASH}$ ¹²	Flash Operating current during read access	$T_a = 125\text{ }^{\circ}\text{C}$ ⁵ 3.3 V supplies 160 MHz frequency	—	40	45	mA
		$T_a = 105\text{ }^{\circ}\text{C}$ 3.3 V supplies 160 MHz frequency	—	40	45	
		$T_a = 85\text{ }^{\circ}\text{C}$ 3.3 V supplies 160 MHz frequency	—	40	45	

- The content of the Conditions column identifies the components that draw the specific current.
- Single e200Z4 core cache disabled @80 MHz, no FlexRay, no ENET, 2 x CAN, 8 LINFlexD, 2 SPI, ADC0 and 1 used constantly, no HSM, Memory: 2M flash, 128K RAM RUN mode, Clocks: FIRC on, XOSC, PLL on, SIRC on for TOD, no 32KHz crystal (TOD runs off SIRC).
- Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C. In case of internal ballast mode, it is expected that the external ballast is not mounted and BAL_SELECT_INT pin is tied to VDD_HV_A supply on board. Internal ballast can be used for all use cases with current consumption upto 150mA
- The power consumption does not consider the dynamic current of I/Os
- $T_j=150^{\circ}\text{C}$. Assumes $T_a=125^{\circ}\text{C}$
 - Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#)
- e200Z4 core, 160MHz, cache enabled; e200Z2 core , 80MHz, no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 256K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
- e200Z4 core, 120MHz, cache enabled; e200Z2 core, 60MHz; no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 128K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 14. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns) ¹ L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[Src 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry ²	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01 ³
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00 ³
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input) ⁴		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.
3. Slew rate control modes
4. Input slope = 2ns

NOTE

The specification given above is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The specification given above is measured between 20% / 80%.

5.2 DC electrical specifications @ 3.3V Range

Table 15. DC electrical specifications @ 3.3V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	Pad_I_HV Input Buffer High Voltage	$0.72 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil (pad_i_hv)	Pad_I_HV Input Buffer Low Voltage	$VDD_HV_x - 0.3$	$0.45 \cdot VDD_HV_x$	V
Vhys (pad_i_hv)	Pad_I_HV Input Buffer Hysteresis	$0.11 \cdot VDD_HV_x$		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	$0.67 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	$VDD_HV_x - 0.3$	$0.35 \cdot VDD_HV_x$	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	$0.57 \cdot VDD_HV_x^{1,1}$	$VDD_HV_x^{1,1} + 0.3$	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	$VDD_HV_x - 0.3$	$0.4 \cdot VDD_HV_x^{1,1}$	V
Vhys	CMOS Input Buffer Hysteresis	$0.09 \cdot VDD_HV_x^{1,1}$		V
Pull_IH (pad_i_hv)	Weak Pullup Current ^{2,2} Low	15		μA
Pull_IH (pad_i_hv)	Weak Pullup Current ^{3,3} High		55	μA
Pull_IL (pad_i_hv)	Weak Pulldown Current ³ Low	28		μA
Pull_IL (pad_i_hv)	Weak Pulldown Current ² High		85	μA
Pull_Ioh	Weak Pullup Current ⁴	15	50	μA
Pull_Iol	Weak Pulldown Current ⁵	15	50	μA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	μA
Voh	Output High Voltage ⁶	$0.8 \cdot VDD_HV_x^{1,1}$	—	V
Vol	Output Low Voltage ⁷ Output Low Voltage ⁸	—	$0.2 \cdot VDD_HV_x^{1,1}$ $0.1 \cdot VDD_HV_x$	V
Ioh_f	Full drive Ioh ^{9,9} (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol ⁹ (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh ⁹ (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol ⁹ (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

1. $VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C$

2. Measured when pad = $0.69 \cdot VDD_HV_x$

3. Measured when pad = $0.49 \cdot VDD_HV_x$

4. Measured when pad = 0 V

5. Measured when pad = VDD_HV_x

6. Measured when pad is sourcing 2 mA

7. Measured when pad is sinking 2 mA

8. Measured when pad is sinking 1.5 mA

9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

Table 20. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
R_{AD}^6	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity (precise channel)	—	–2	—	2	LSB
INL	Integral non-linearity (standard channel)	—	–3	—	3	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (precision channel)	150 °C	—	—	250	nA
	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{\text{precision channels}}$	Total unadjusted error for precision channels	Without current injection	–6	+/-4	6	LSB
		With current injection ^{7, 7}		+/-5		LSB
$TUE_{\text{standard/extended channels}}$	Total unadjusted error for standard/extended channels	Without current injection	–8	+/-6	8	LSB
		With current injection ⁷		+/-8		LSB
t_{recovery}	STOP mode to Run mode recovery time				< 1	μs

- Active ADC input, $V_{inA} < [\min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]$. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions ($VDD_HV_x = 3.3\text{ V}$)' for required relation between IO_supply_A,B,C and ADC_Supply .
- The internally generated clock (known as AD_clk or $ADCK$) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
- This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
- Apart from t_{sample} and t_{conv} , few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
- See Figure 6.
- Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (V_{INA} , see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK^2 frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time ³	80 MHz @ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

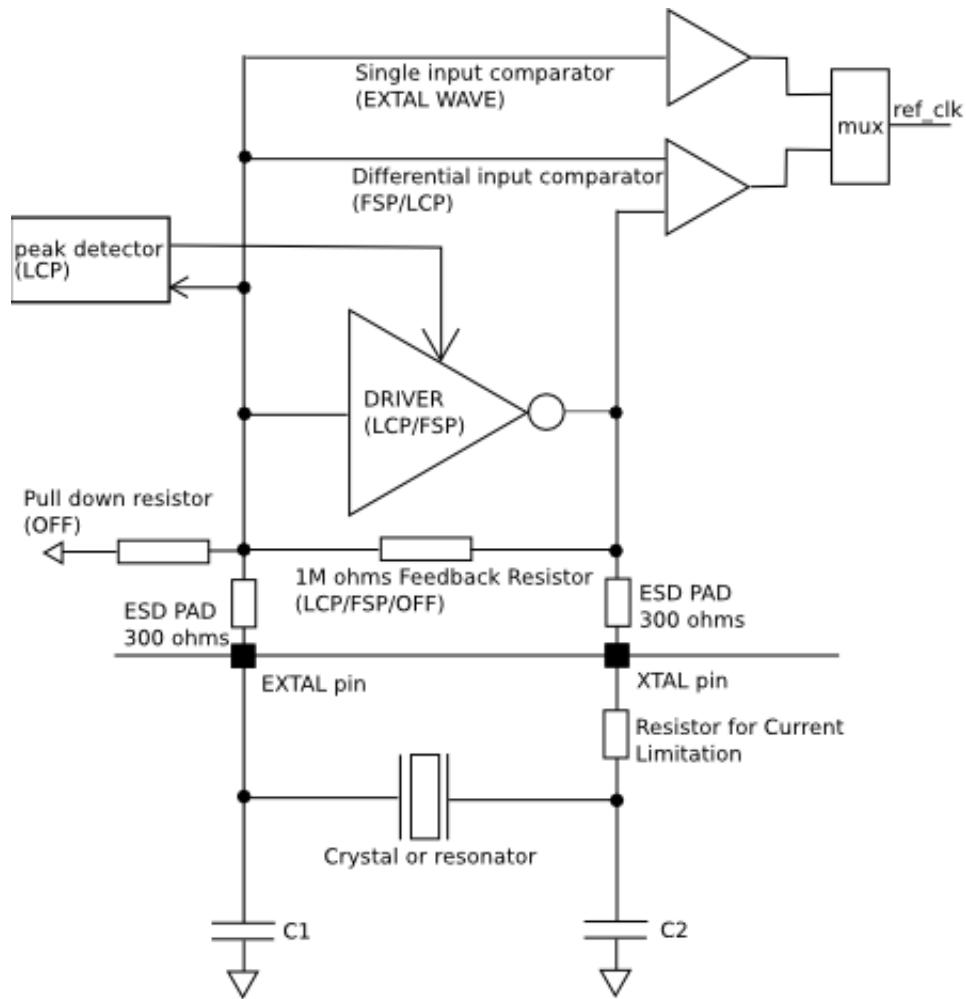


Figure 7. Oscillator connections scheme

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	LCP			23		mA/V
		FSP			33		
V_{XOSCHS}	Oscillation Amplitude	LCP ^{1, 2, 1, 2}	8 MHz		1.0		V_{PP}
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP ¹	8 MHz		2		ms
			16 MHz		1		
			40 MHz		0.5		

Table continues on the next page...

Table 23. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
	Oscillator Analog Circuit supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		
		LCP	8 MHz		141		uA
			16 MHz		252		
			40 MHz		518		
V _{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3	1.95			V
V _{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3			1.25	V

1. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board.
2. Typ value for oscillator supply 3.3 V@27 °C

6.2.2 32 kHz Oscillator electrical specifications

Table 24. 32 kHz oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{osc_lo}	Oscillator crystal or resonator frequency		32		40	KHz
t _{cst}	Crystal Start-up Time ^{1, 2}				2	s

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 16 MHz RC Oscillator electrical specifications

Table 25. 16 MHz RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F _{Target}	IRC target frequency	—	—	16	—	MHz
PTA	IRC frequency variation after trimming	—	-5	—	5	%
T _{startup}	Startup time	—		—	1.5	us
T _{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T _{LTJIT}	Long term jitter		—	—	0.2	%

Table 30. Flash memory program and erase specifications

Symbol	Characteristic ¹	Typ ²	Factory Programming ^{3, 4}		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life ⁵	Lifetime Max ⁶		
						20°C ≤T _A ≤30°C	-40°C ≤T _J ≤150°C	
t _{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		μs
t _{ppgm}	Page (256 bits) program time	73	200	300	108	500		μs
t _{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		μs
t _{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t _{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t _{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t _{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t _{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t _{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
t _{256kers}	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
t _{256kpgm}	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programming times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max ^{1, 1}	Units ^{2, 2}
t _{ai16kseq}	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x T _{period} x N _{read}	—
t _{ai32kseq}	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x T _{period} x N _{read}	—
t _{ai64kseq}	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x T _{period} x N _{read}	—

Table continues on the next page...

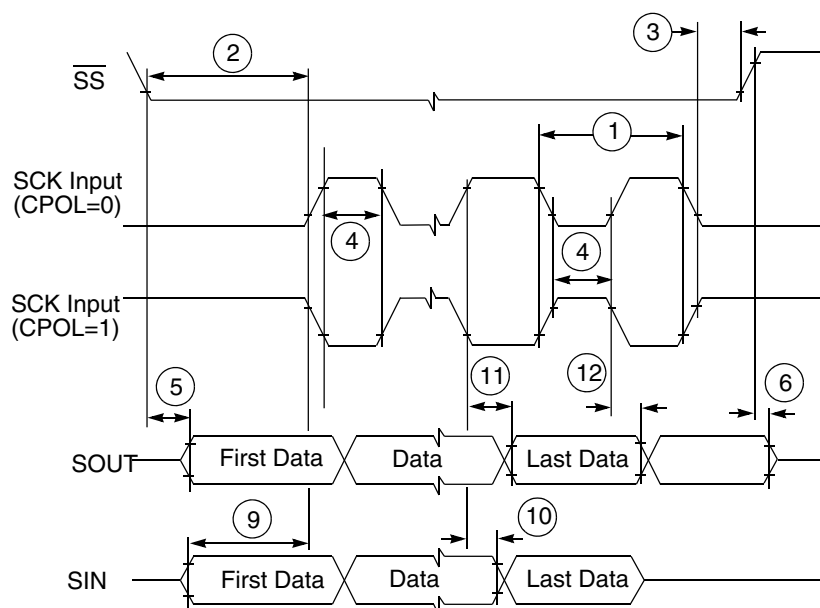


Figure 14. DSPI modified transfer format timing – slave, CPHA = 0

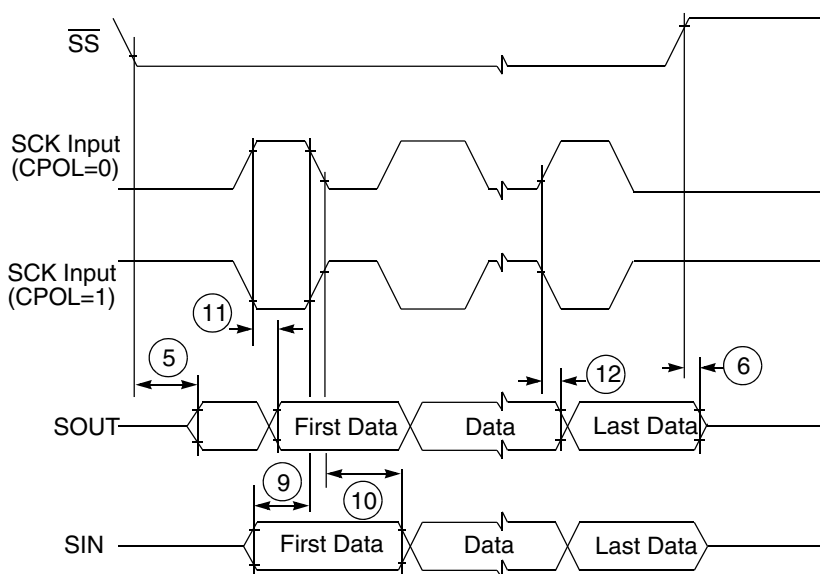


Figure 15. DSPI modified transfer format timing — slave, CPHA = 1

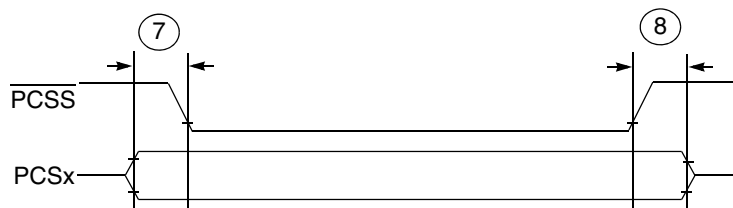


Figure 16. DSPI PCS strobe (PCSS) timing

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

6.4.2.2 TxEN

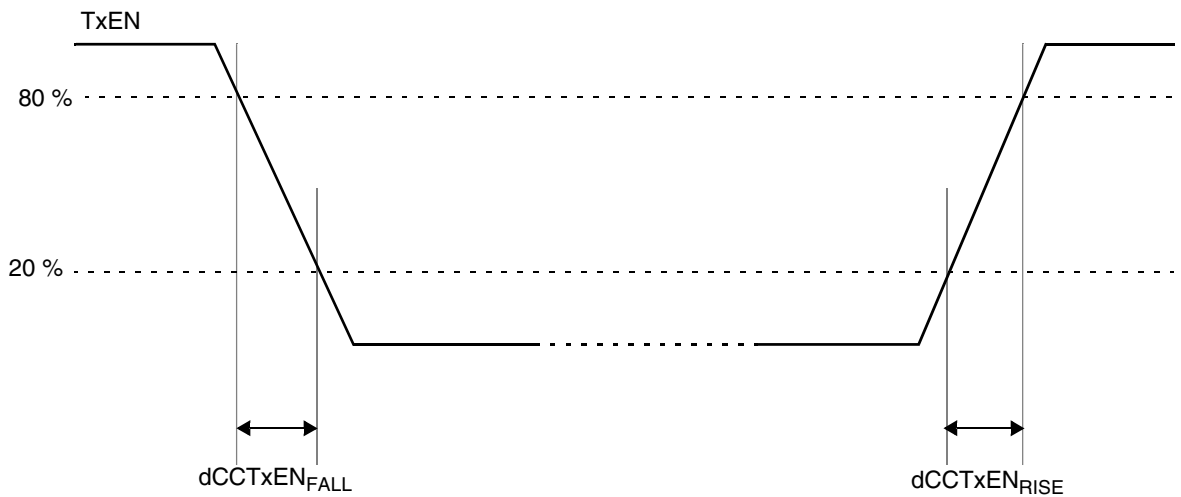


Figure 17. TxEN signal

Table 38. TxEN output characteristics¹

Name	Description	Min	Max	Unit
dCCTxEN _{RISE25}	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN _{FALL25}	Fall time of TxEN signal at CC	—	9	ns
dCCTxEN ₀₁	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxEN ₁₀	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD_HV_IOx} = 3.3\text{ V} \pm 5\%, \pm 10\%$, $T_J = -40\text{ }^{\circ}\text{C} / 150\text{ }^{\circ}\text{C}$, TxEN pin load maximum 25 pF

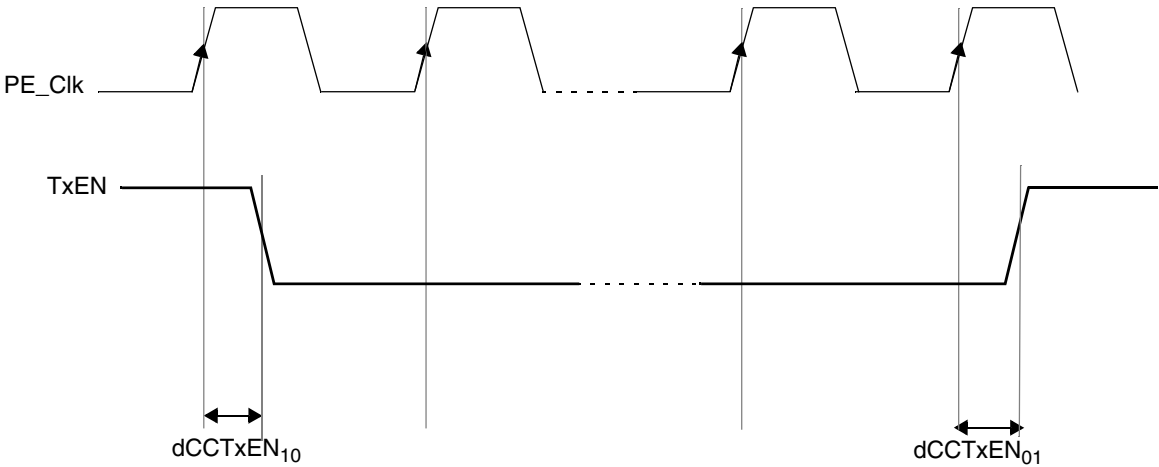


Figure 18. TxEN signal propagation delays

6.4.2.3 TxD

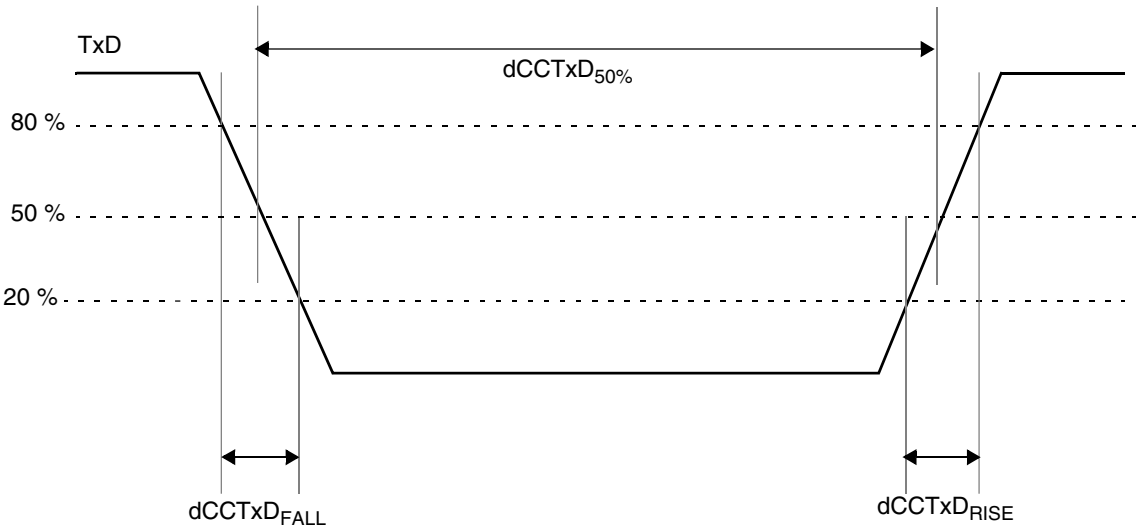


Figure 19. TxD Signal

Table 39. TxD output characteristics

Name	Description ¹	Min	Max	Unit
dCCT _{xAsym}	Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns)	-2.45	2.45	ns
dCCTxD _{RISE25} +dCCTxD _{FALL25}	Sum of Rise and Fall time of TxD signal at the output	—	9 ²	ns

Table continues on the next page...

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, T_J = -40 oC / 150 oC.

6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 41. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

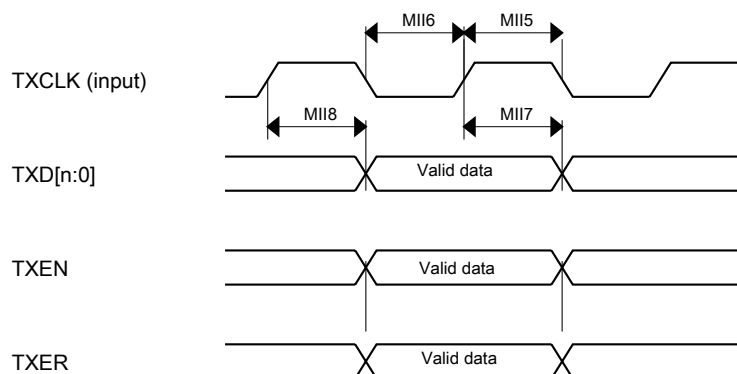
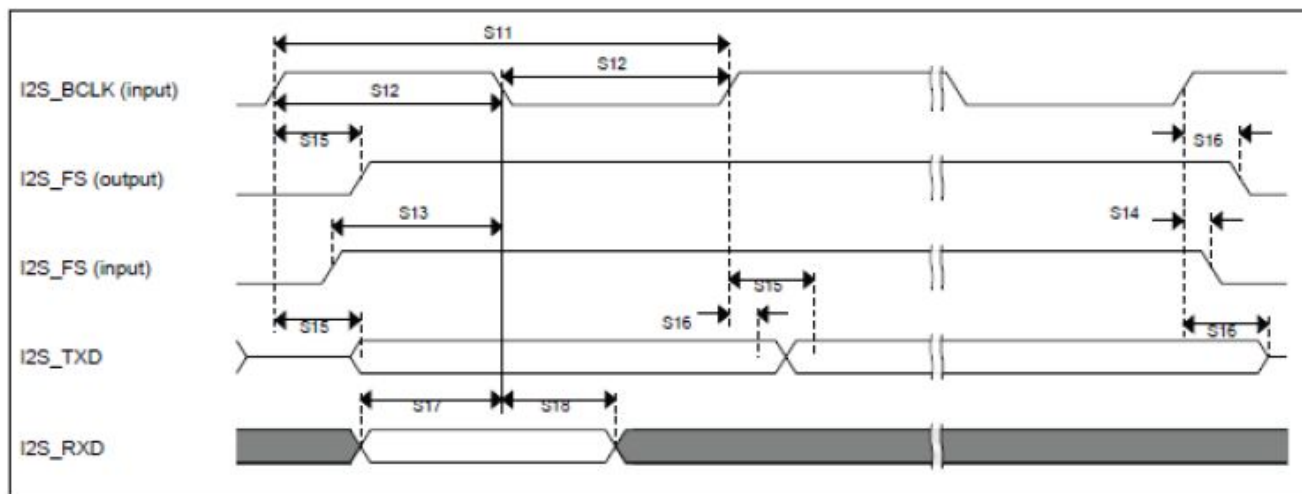


Figure 21. RMII/MII transmit signal timing diagram

Table 44. Slave mode SAI Timing (continued)

No	Parameter	Value		Unit
		Min	Max	
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

**Figure 24. Slave mode SAI Timing**

6.5 Debug specifications

6.5.1 JTAG interface timing

Table 45. JTAG pin AC electrical characteristics ¹

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time ^{2, 2}	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20 ^{3, 3}	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600 ^{4, 4}	ns

Table continues on the next page...

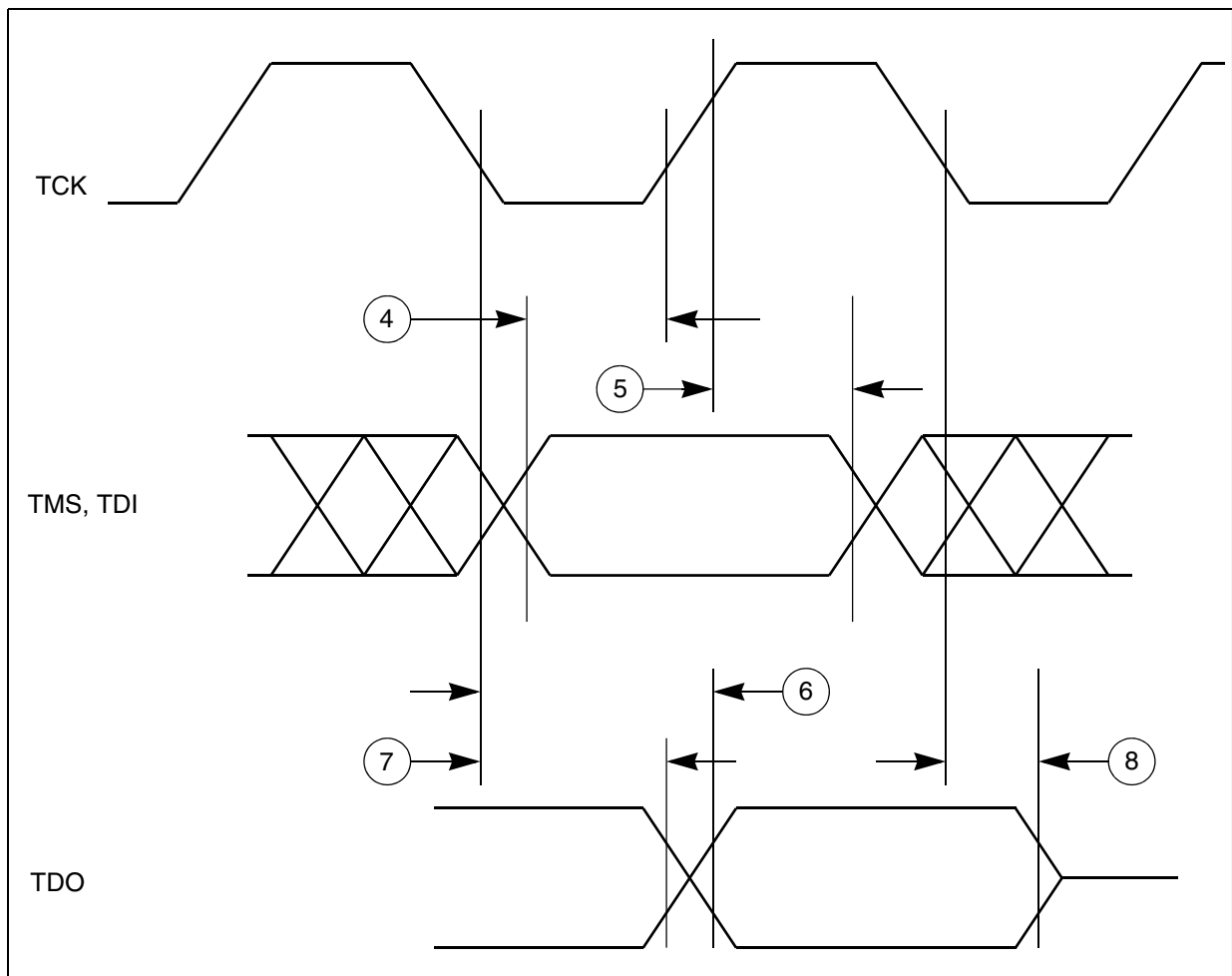


Figure 26. JTAG test access port timing

10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

Table 50. BAF execution duration

BAF execution duration	Min	Typ	Max	Unit
BAF execution time (boot header at first location)	—	200	—	μs
BAF execution time (boot header at last location)	—	—	320	μs

10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

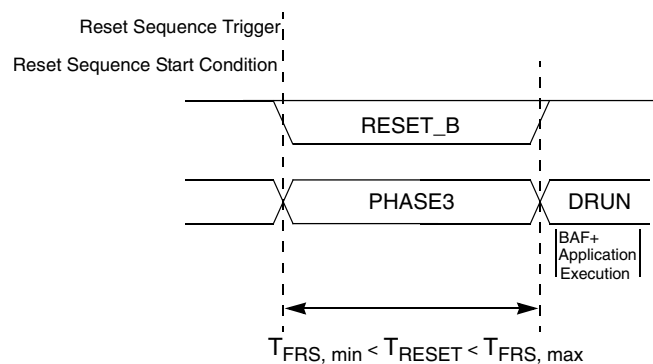


Figure 36. Functional reset sequence short

The reset sequences shown in [Figure 35](#) and [Figure 36](#) are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

11.1 Revision History

The following table provides a revision history for this document.

Table 51. Revision History

Rev. No.	Date	Substantial Changes
Rev 1	14 March 2013	Initial Release

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev 4	9 March 2016	- In section, Voltage regulator electrical characteristics - In table, Voltage regulator electrical specifications: - Updated the footnote on $V_{DD_HV_BALLAST}$
Rev 5	27 February 2017	- In Family Comparison section: - Updated the "MPC5746C Family Comparison" table. - added "NVM Memory Map 1", "NVM Memory Map 2", and "RAM Memory Map" tables. - Updated the product version, flash memory size and optional fields information in Ordering Information section. - In Recommended Operating Conditions section, removed the note related to additional crossover current. $V_{DD_HV_C}$ row added in "Voltage regulator electrical specifications" table in Voltage regulator electrical characteristics section. - In Voltage Monitor Electrical Characteristics section, updated the "Trimmed" Fall and Rise specs of $V_{HVD_LV_cold}$ parameter in "Voltage Monitor Electrical Characteristics" table. - In AC Electrical Specifications: 3.3 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. - In DC Electrical Specifications: 3.3 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" and updated "Vol min and max" values in the table. - In AC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" in the table. - In DC Electrical Specifications: 5 V Range section, changed the occurrences of "ipp_sre[1:0]" to "SIUL2_MSCRn.SRC[1:0]" and updated "Vol min and max" values in the table. - In "Flash memory AC timing specifications" table in Flash memory AC timing specifications section: - Updated the "t_{psus}" typ value from 7 us to 9.4 us. - Updated the "t_{psus}" max value from 9.1 us to 11.5 us. - Added "Continuous SCK Timing" table in DSPI timing section. - Added "ADC pad leakage" at 105°C TA conditions in "ADC conversion characteristics (for 12-bit)" table in ADC electrical specifications section. - In "STANDBY Current consumption characteristics" table in Supply current characteristics section: - Updated the Typ and max values of I_{DD} Standby current. - Added I_{DD} Standby3 current spec for FIRC ON. - Removed I_{VDDHV} and I_{VDDL} specs in 16 MHz RC Oscillator electrical specifications section. - Added Reset Sequence section, with Reset Sequence Duration, BAF execution duration section, and Reset Sequence Distribution as its sub-sections.

Table continues on the next page...