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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	178
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746ck1ammj6r

- Debug functionality
 - e200z2 core: NDI per IEEE-ISTO 5001-2008 Class3+
 - e200z4 core: NDI per IEEE-ISTO 5001-2008 Class 3+
- Timer
 - 16 Periodic Interrupt Timers (PITs)
 - Two System Timer Modules (STM)
 - Three Software Watchdog Timers (SWT)
 - 64 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels
- Device/board boundary Scan testing supported with Joint Test Action Group (JTAG) of IEEE 1149.1 and IEEE 1149.7 (CJTAG)
- Security
 - Hardware Security Module (HSMv2)
 - Password and Device Security (PASS) supporting advanced censorship and life-cycle management
 - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Functional Safety
 - ISO26262 ASIL-B compliance
- Multiple operating modes
 - Includes enhanced low power operation

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Table 2. MPC5746C Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW partition	MPC5744	MPC5745	MPC5746
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	not available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	7	not available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	7	not available	not available	available
0x011C0000	0x011FFFFFFF	256 KB code Flash block 7	7	not available	not available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	not available	not available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	not available	not available	not available

Table 3. MPC5746C Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW partition	MPC5744B MPC5745B MPC5746B	MPC5744C MPC5745C MPC5746C
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	not available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	not available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	not available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	not available	available

Table 4. MPC5746C Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40000000	0x40001FFF	8 KB	SRAM0	available	available	available
0x40002000	0x4000FFFF	56 KB	SRAM1	available	available	available
0x40010000	0x4001FFFF	64 KB	SRAM2	available	available	available
0x40020000	0x4002FFFF	64 KB	SRAM3	available	available	available

Table continues on the next page...

Table 4. MPC5746C Family Comparison - RAM Memory Map (continued)

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40030000	0x4003FFFF	64 KB	SRAM4	not available	available	available
0x40040000	0x4004FFFF	64 KB	SRAM5	not available	not available	available
0x40050000	0x4005FFFF	64 KB	SRAM6	not available	not available	available
0x40060000	0x4006FFFF	64 KB	SRAM7	not available	not available	optional
0x40070000	0x4007FFFF	64 KB	SRAM8	not available	not available	optional

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5746C.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 5. Absolute maximum ratings

Symbol	Parameter	Conditions ¹	Min	Max	Unit
$V_{DD_HV_A}$, $V_{DD_HV_B}$, $V_{DD_HV_C}$ ^{2,3}	3.3 V - 5.5V input/output supply voltage	—	−0.3	6.0	V
$V_{DD_HV_FLA}$ ^{4,5}	3.3 V flash supply voltage (when supplying from an external source in bypass mode)	—	−0.3	3.63	V
$V_{DD_LP_DEC}$ ⁶	Decoupling pin for low power regulators ⁷	—	−0.3	1.32	V
$V_{DD_HV_ADC1_REF}$ ⁸	3.3 V / 5.0 V ADC1 high reference voltage	—	−0.3	6	V
$V_{DD_HV_ADC0}$ $V_{DD_HV_ADC1}$	3.3 V to 5.5V ADC supply voltage	—	−0.3	6.0	V
$V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$	3.3V to 5.5V ADC supply ground	—	−0.1	0.1	V
V_{DD_LV} ^{9, 10, 10, 11, 11, 12}	Core logic supply voltage	—	−0.3	1.32	V
V_{INA}	Voltage on analog pin with respect to ground (V_{SS_HV})	—	−0.3	Min ($V_{DD_HV_x}$, $V_{DD_HV_ADCx}$, $V_{DD_ADCx_REF}$) +0.3	V
V_{IN}	Voltage on any digital pin with respect to ground (V_{SS_HV})	Relative to $V_{DD_HV_A}$, $V_{DD_HV_B}$, $V_{DD_HV_C}$	−0.3	$V_{DD_HV_x} + 0.3$	V
I_{INJPAD}	Injected input current on any pin during overload condition	Always	−5	5	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	−50	50	mA
T_{ramp}	Supply ramp rate	—	0.5 V / min	100V/ms	—
T_A ¹³	Ambient temperature	—	−40	125	°C
T_{STG}	Storage temperature	—	−55	165	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. $V_{DD_HV_B}$ and $V_{DD_HV_C}$ are common together on the 176 LQFP-EP package.
3. Allowed $V_{DD_HV_x} = 5.5\text{--}6.0$ V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, $T_J = 150$ °C, remaining time at or below 5.5 V.
4. $V_{DD_HV_FLA}$ must be connected to $V_{DD_HV_A}$ when $V_{DD_HV_A} = 3.3$ V
5. $V_{DD_HV_FLA}$ must be disconnected from ANY power sources when $V_{DD_HV_A} = 5$ V
6. This pin should be decoupled with low ESR 1 μ F capacitor.
7. Not available for input voltage, only for decoupling internal regulators
8. 10-bit ADC does not have dedicated reference and its reference is bonded to 10-bit ADC supply($V_{DD_HV_ADC0}$) inside the package.
9. Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum $T_J = 150$ °C, remaining time as defined in footnotes 10 and 11.
10. Allowed 1.38 – 1.45 V– for 10 hours cumulative time at maximum $T_J = 150$ °C, remaining time as defined in footnote 11.
11. 1.32 – 1.38 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.326 V at maximum $T_J = 150$ °C.
12. If HVD on core supply ($V_{HVD_LV_x}$) is enabled, it will generate a reset when supply goes above threshold.
13. $T_J = 150$ °C. Assumes $T_A = 125$ °C
 - Assumes maximum θ_{JA} for 2s2p board. See [Thermal attributes](#)

Table 8. Voltage regulator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{\text{flash_reg}}$ ⁴	External decoupling / stability capacitor for internal Flash regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2	3	μF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
$C_{\text{HV_VDD_A}}$	VDD_HV_A supply capacitor ^{5, 5}	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_VDD_B}}$	VDD_HV_B supply capacitor ⁵	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_VDD_C}}$	VDD_HV_C supply capacitor ⁵	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_ADC0}}$ $C_{\text{HV_ADC1}}$	HV ADC supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_ADR}}$ ⁶	HV ADC SAR reference supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.47	—	—	μF
$V_{\text{DD_HV_BALLAST}}^{\text{AST}}$ ⁷	FPREG Ballast collector supply voltage	When collector of NPN ballast is directly supplied by an on board supply source (not shared with VDD_HV_A supply pin) without any series resistance, that is, $R_{\text{C_BALLAST}}$ less than 0.01 Ohm.	2.25	—	5.5	V
$R_{\text{C_BALLAST}}$	Series resistor on collector of FPREG ballast	When VDD_HV_BALLAST is shorted to VDD_HV_A on the board	—	—	0.1	Ohm
t_{SU}	Start-up time with external ballast after main supply (VDD_HV_A) stabilization	$C_{\text{fp_reg}} = 3 \mu\text{F}$	—	74	—	μs
$t_{\text{SU_int}}$	Start-up time with internal ballast after main supply (VDD_HV_A) stabilization	$C_{\text{fp_reg}} = 3 \mu\text{F}$	—	103	—	μs
t_{ramp}	Load current transient	Iload from 15% to 55% $C_{\text{fp_reg}} = 3 \mu\text{F}$		1.0		μs

1. Split capacitance on each pair VDD_LV pin should sum up to a total value of $C_{\text{fp_reg}}$
2. Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.
3. Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
4. It is required to minimize the board parasitic inductance from decoupling capacitor to VDD_HV_FL A pin and the routing inductance should be less than 1nH.

Table 9. Voltage monitor electrical characteristics (continued)

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up ¹	Mask Opt ^{2, 2}	Reset Type	Min	Typ	Max	V
V _{LVD_LV_PD} 2_cold	LV supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.1400	1.1550	1.1750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.1600	1.1750	1.1950	V

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.
3. There is no voltage monitoring on the V_{DD_HV_ADC0}, V_{DD_HV_ADC1}, V_{DD_HV_B} and V_{DD_HV_C} I/O segments. For applications requiring monitoring of these segments, either connect these to V_{DD_HV_A} at the PCB level or monitor externally.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 10. Current consumption characteristics

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
I _{DD_BODY_1} 2, 3	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies ^{4, 4} T _a = 125°C ^{5, 5} V _{DD_LV} = 1.25 V V _{DD_HV_A} = 5.5V SYS_CLK = 80MHz	—	—	147	mA
		T _a = 105°C	—	—	142	mA
		T _a = 85 °C	—	—	137	mA

Table continues on the next page...

5.3 AC specifications @ 5 V Range

Table 16. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. Delay (ns) ¹ L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCrN[Src 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		4.5/4.5		1.3/1.2	25	11
		6/6		2.5/2	50	
		13/13		9/9	200	
		5.25/5.25		3/2	25	
		9/8		5/4	50	10
		22/22		18/16	200	
		27/27		13/13	50	
		40/40		24/24	200	
		40/40		24/24	50	00 ²
		65/65		40/40	200	
pad_i_hv/ pad_sr_hv (input)		1.5/1.5		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output

2. Slew rate control modes

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V

Table continues on the next page...

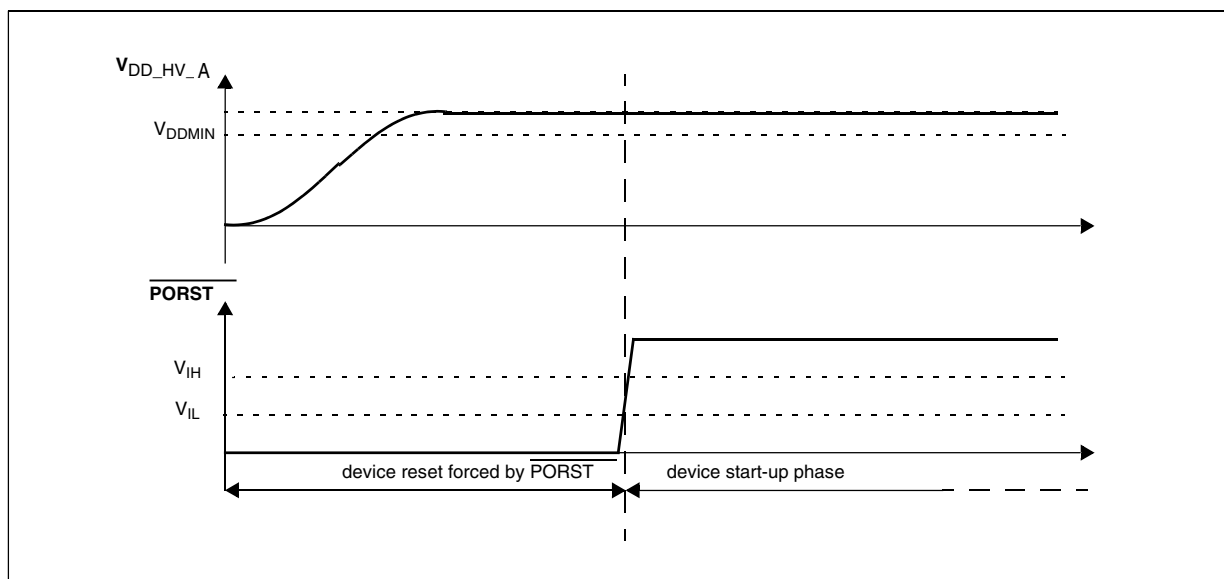


Figure 3. Start-up reset requirements

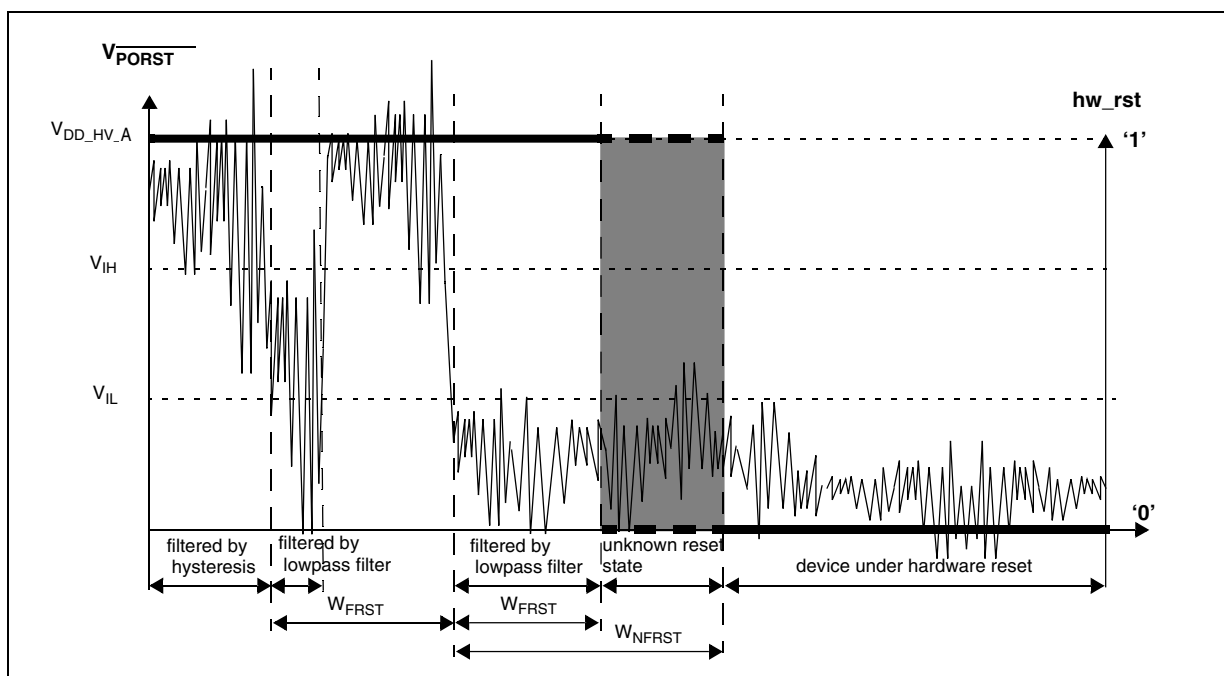


Figure 4. Noise filtering on reset signal

Table 18. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	CMOS Input Buffer High Voltage	—	$0.65 \cdot V_{D_{HV_x}}$	—	$V_{D_{HV_x}} + 0.3$	V
V_{IL}	CMOS Input Buffer Low Voltage	—	$V_{D_{HV_x}} - 0.3$	—	$0.35 \cdot V_{D_{HV_x}}$	V

Table continues on the next page...

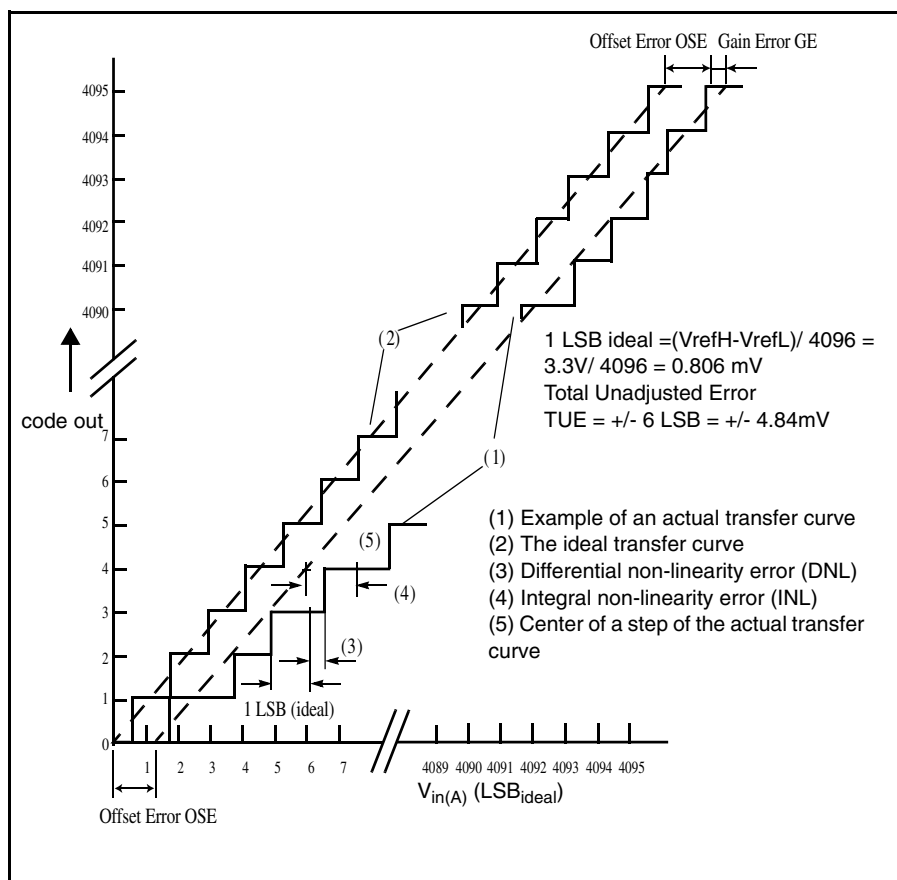


Figure 5. ADC characteristics and error definitions

Table 20. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
R_{AD}^6	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity (precise channel)	—	–2	—	2	LSB
INL	Integral non-linearity (standard channel)	—	–3	—	3	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (precision channel)	150 °C	—	—	250	nA
	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{\text{precision channels}}$	Total unadjusted error for precision channels	Without current injection	–6	+/-4	6	LSB
		With current injection ^{7, 7}		+/-5		LSB
$TUE_{\text{standard/extended channels}}$	Total unadjusted error for standard/extended channels	Without current injection	–8	+/-6	8	LSB
		With current injection ⁷		+/-8		LSB
t_{recovery}	STOP mode to Run mode recovery time				< 1	μs

1. Active ADC input, $V_{inA} < [\min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]$. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions ($VDD_HV_x = 3.3\text{ V}$)' for required relation between IO_supply_A,B,C and ADC_Supply .
2. The internally generated clock (known as AD_clk or $ADCK$) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from t_{sample} and t_{conv} , few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 6.
7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (V_{INA} , see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK^2 frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time ³	80 MHz @ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

Table 21. ADC conversion characteristics (for 10-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
t_{conv}	Conversion time ⁴	80 MHz	550	—	—	ns
t_{total_conv}	Total Conversion time $t_{sample} + t_{conv}$ (for standard channels)	80 MHz	1	—	—	μs
	Total Conversion time $t_{sample} + t_{conv}$ (for extended channels)		1.5	—	—	
C_S ⁵	ADC input sampling capacitance	—	—	3	5	pF
C_{P1} ⁵	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2} ⁵	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1} ⁵	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	k Ω
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD} ⁵	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max positive/negative injection		–5	—	5	mA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
$TUE_{standard/extended}$ channels	Total unadjusted error for standard channels	Without current injection	–4	+/-3	4	LSB
		With current injection ⁶		+/-4		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	μs

1. Active ADC Input, $V_{inA} < [\min(ADC_ADV, IO_Supply_A,B,C)]$. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO_supply_A , B, C and ADC_Supply .
2. The internally generated clock (known as AD_clk or $ADCK$) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See [Figure 65](#)
6. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (V_{INA} , see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

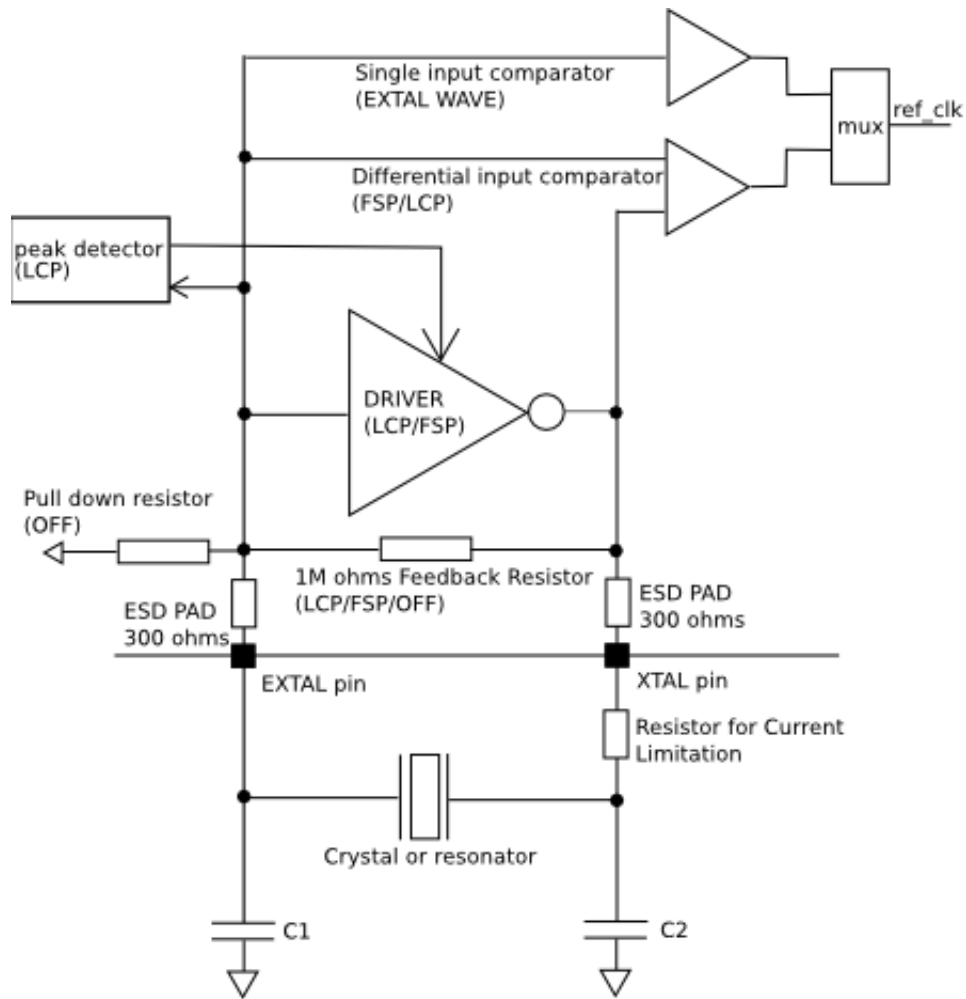


Figure 7. Oscillator connections scheme

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	LCP			23		mA/V
		FSP			33		
V_{XOSCHS}	Oscillation Amplitude	LCP ^{1, 2, 1, 2}	8 MHz		1.0		V_{PP}
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP ¹	8 MHz		2		ms
			16 MHz		1		
			40 MHz		0.5		

Table continues on the next page...

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

6.4.2.2 TxEN

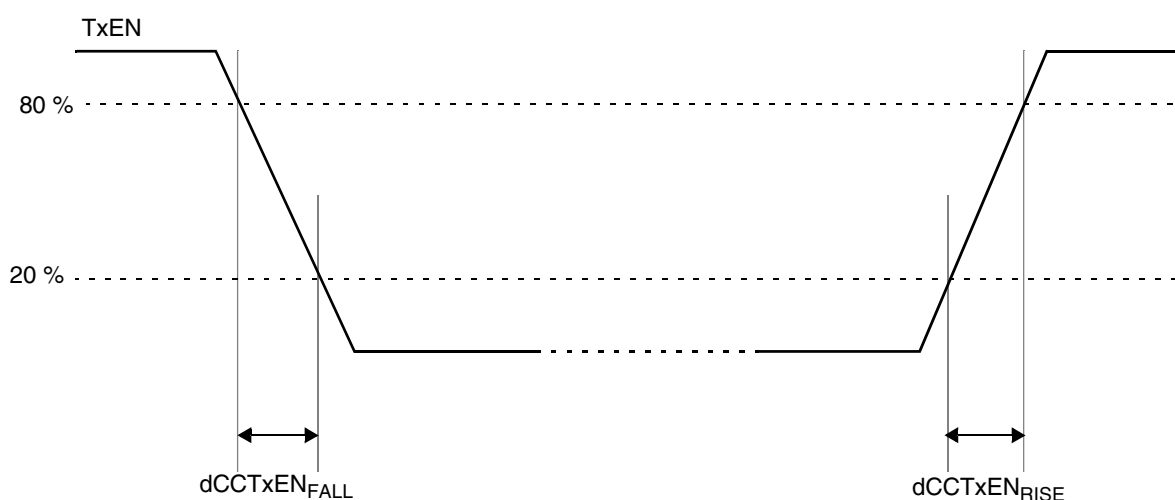


Figure 17. TxEN signal

Table 38. TxEN output characteristics¹

Name	Description	Min	Max	Unit
dCCTxEN _{RISE25}	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN _{FALL25}	Fall time of TxEN signal at CC	—	9	ns
dCCTxEN ₀₁	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxEN ₁₀	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD_HV_IOx} = 3.3\text{ V} -5\%, \pm 10\%$, $T_J = -40\text{ }^{\circ}\text{C} / 150\text{ }^{\circ}\text{C}$, TxEN pin load maximum 25 pF

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = -40 oC / 150 oC.

6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 41. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

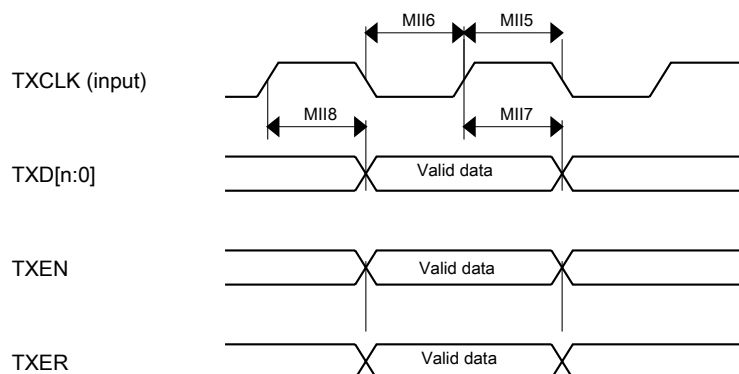
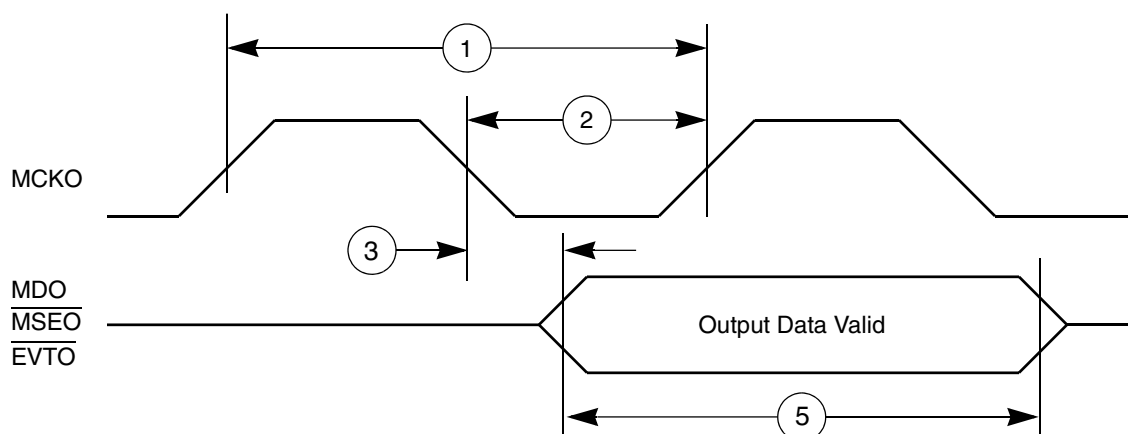
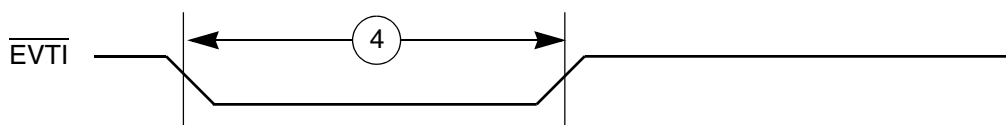


Figure 21. RMII/MII transmit signal timing diagram

Table 46. Nexus debug port timing ¹ (continued)

No.	Symbol	Parameter	Condition s	Min	Max	Unit
9	t_{NTDIH} , t_{NTMSH}	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

**Figure 28. Nexus output timing****Figure 29. Nexus EVTI Input Pulse Width**

6.5.4 External interrupt timing (IRQ pin)

Table 48. External interrupt timing specifications

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time	—	6	—	t_{CYC}

These values apply when IRQ pins are configured for rising edge or falling edge events, but not both.

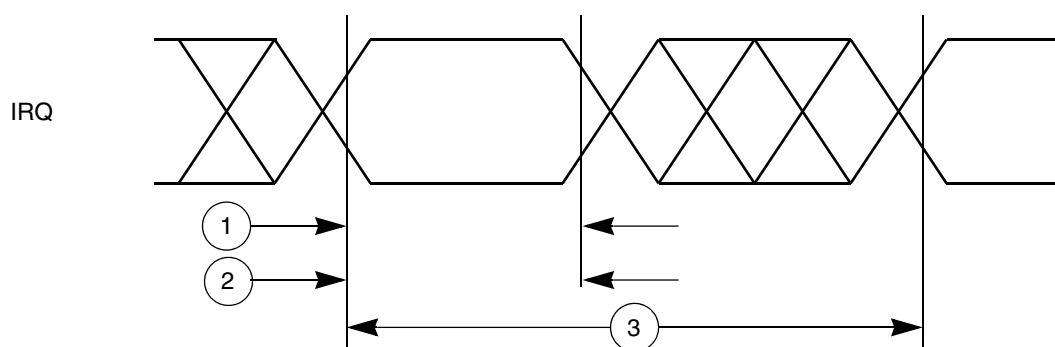


Figure 31. External interrupt timing

7 Thermal attributes

7.1 Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50.7	$^{\circ}\text{C/W}$	11, 22
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	24.2	$^{\circ}\text{C/W}$	1, 2, 33
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	38.1	$^{\circ}\text{C/W}$	1, 3

Table continues on the next page...

10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

Table 50. BAF execution duration

BAF execution duration	Min	Typ	Max	Unit
BAF execution time (boot header at first location)	—	200	—	μs
BAF execution time (boot header at last location)	—	—	320	μs

10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

Reset sequence

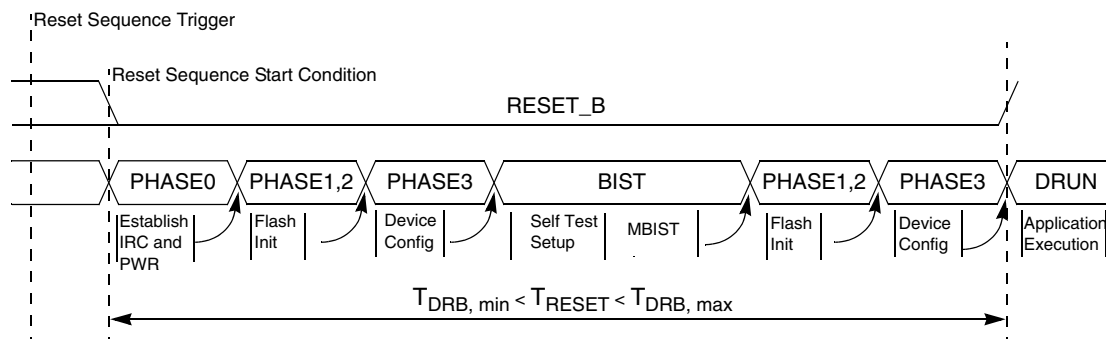


Figure 32. Destructive reset sequence, BIST enabled

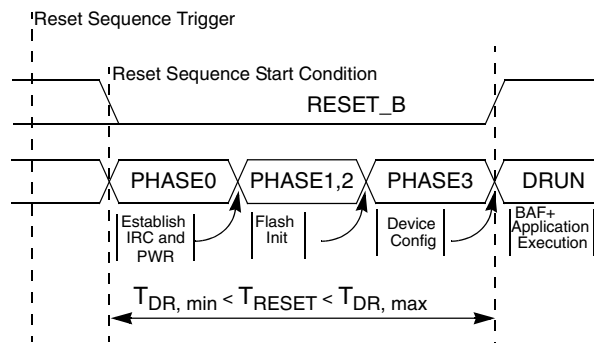


Figure 33. Destructive reset sequence, BIST disabled

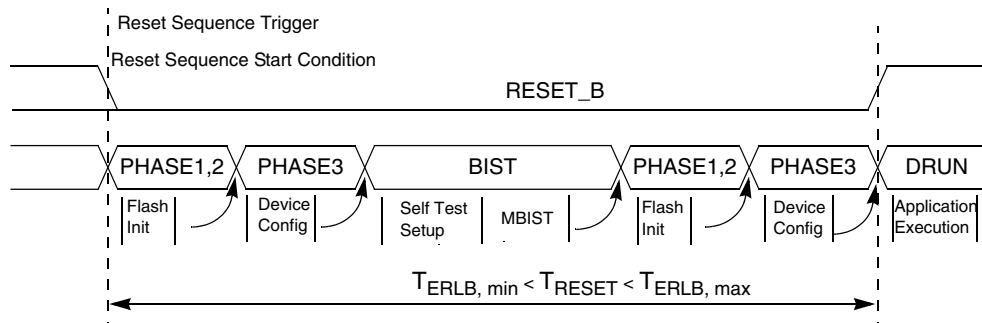


Figure 34. External reset sequence long, BIST enabled

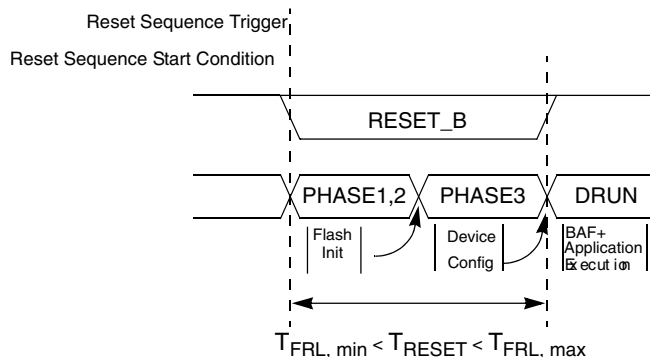


Figure 35. Functional reset sequence long