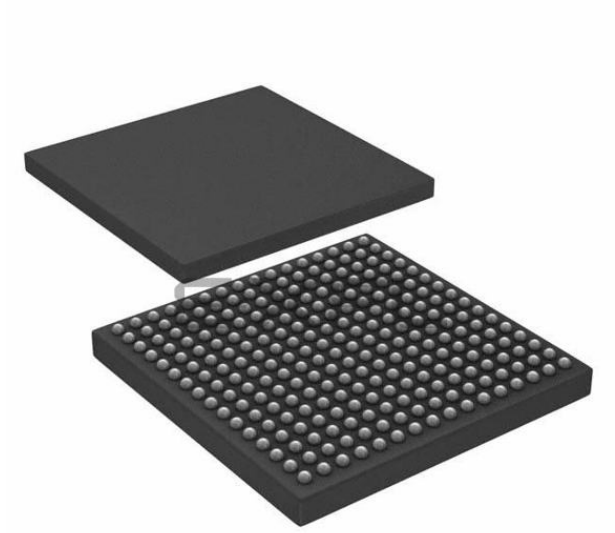

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Details	
Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	178
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746ck1mmj6r

Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V) (continued)

Symbol	Parameter	Conditions[1]	Min[2]	Max	Unit
T_A[8]	Ambient temperature under bias	f_{CPU} ≤ 160 MHz	–40	125	°C
T_J	Junction temperature under bias	—	–40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. Only applicable when supplying from external source.
5. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
6. VIN1_CMP_REF ≤ VDD_HV_A
7. This supply is shorted VDD_HV_A on lower packages.
8. T_J=150°C. Assumes T_A=125°C
   - Assumes maximum θJA of 2s2p board. See Thermal attributes

NOTE

If VDD_HV_A is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. VDD_HV_FLA should not be supplied externally and should only have decoupling capacitor.

Table 7. Recommended operating conditions ($V_{DD\_HV\_x}$ = 5 V)

Symbol	Parameter	Conditions [1]	Min[2]	Max	Unit
$V_{DD\_HV\_A}$ $V_{DD\_HV\_B}$ $V_{DD\_HV\_C}$	HV IO supply voltage	—	4.5	5.5	V
$V_{DD\_HV\_FLA}$[3]	HV flash supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_ADC1\_REF}$	HV ADC1 high reference voltage	—	3.15	5.5	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	HV ADC supply voltage	—	max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05	5.5	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV}[4]	Core supply voltage	—	1.2	1.32	V
$V_{IN1\_CMP\_REF}$[5, 6]	Analog Comparator DAC reference voltage	—	3.15	5.5[5]	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_A[7]	Ambient temperature under bias	f_{CPU} ≤ 160 MHz	–40	125	°C
T_J	Junction temperature under bias	—	–40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. When VDD_HV is in 5 V range, VDD_HV_FLA cannot be supplied externally.This pin is decoupled with C_{flash_reg}.

5. 1. For VDD_HV_x, 1µf on each side of the chip
      a. 0.1 µf close to each VDD/VSS pin pair.
      b. 10 µf near for each power supply source
      c. For VDD_LV, 0.1uf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter.
   2. For VDD_LV, 0.1uf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter
6. Only applicable to ADC1
7. In external ballast configuration the following must be ensured during power-up and power-down (Note: If $V_{DD\_HV\_BALLAST}$ is supplied from the same source as VDD_HV_A this condition is implicitly met):
   - During power-up, $V_{DD\_HV\_BALLAST}$ must have met the min spec of 2.25V before VDD_HV_A reaches the POR_HV_RISE min of 2.75V.
   - During power-down, $V_{DD\_HV\_BALLAST}$ must not drop below the min spec of 2.25V until VDD_HV_A is below POR_HV_FALL min of 2.7V.

NOTE

For a typical configuration using an external ballast transistor with separate supply for VDD_HV_A and the ballast collector, a bulk storage capacitor (as defined in Table 8) is required on VDD_HV_A close to the device pins to ensure a stable supply voltage.

Extra care must be taken if the VDD_HV_A supply is also being used to power the external ballast transistor or the device is running in internal regulation mode. In these modes, the inrush current on device Power Up or on exit from Low Power Modes is significant and may case the VDD_HV_A voltage to drop resulting in an LVD reset event. To avoid this, the board layout should be optimized to reduce common trace resistance or additional capacitance at the ballast transistor collector (or VDD_HV_A pins in the case of internal regulation mode) is required. NXP recommends that customers simulate the external voltage supply circuitry.

In all circumstances, the voltage on VDD_HV_A must be maintained within the specified operating range (see Recommended operating conditions) to prevent LVD events.

Table 9. Voltage monitor electrical characteristics (continued)

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt[2, 2]	Reset Type	Min	Typ	Max	V
$V_{LVD\_LV\_PD2\_cold}$	LV supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.1400	1.1550	1.1750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.1600	1.1750	1.1950	V

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.
3. There is no voltage monitoring on the $V_{DD\_HV\_ADC0}$, $V_{DD\_HV\_ADC1}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ I/O segments. For applications requiring monitoring of these segments, either connect these to $V_{DD\_HV\_A}$ at the PCB level or monitor externally.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 10. Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_BODY\_1}$ [2, 3]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4, 4] T_a = 125°C [5, 5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 80MHz	—	—	147	mA
		T_a = 105°C	—	—	142	mA
		T_a = 85 °C	—	—	137	mA

Table continues on the next page...

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_BODY\_2}$ 6	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125°C[5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	—	246	mA
		T_a = 105°C	—	—	235	mA
		T_a = 85°C	—	—	210	mA
$I_{DD\_BODY\_3}$ 7	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125 °C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	181	mA
		T_a = 105 °C	—	—	176	mA
		T_a = 85°C	—	—	171	mA
$I_{DD\_BODY\_4}$[8]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125 °C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	264	mA
		T_a = 105 °C	—	—	176	mA
		T_a = 85 °C	—	—	171	mA
I_{DD_STOP}	STOP mode Operating current	T_a = 125 °C[9] V_{DD_LV} = 1.25 V	—	—	49	mA
		T_a = 105 °C V_{DD_LV} = 1.25 V	—	10.6	—	
		T_a = 85 °C V_{DD_LV} = 1.25 V	—	8.1	—	
		T_a = 25 °C V_{DD_LV} = 1.25 V	—	4.6	—	

Table continues on the next page...

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_HV\_ADC\_REF}$[10, 11, 11]	ADC REF Operating current	T_a = 125 °C[5] 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 5.5 V	—	200	400	µA
		T_a = 105 °C 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 5.5 V	—	200	—	
		T_a = 85 °C 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 5.5 V	—	200	—	
		T_a = 25 °C 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 3.6 V	—	200	—	
$I_{DD\_HV\_ADCx}$[11]	ADC HV Operating current	T_a = 125 °C[5] ADC operating at 80 MHz $V_{DD\_HV\_ADC}$ = 5.5 V	—	1.2	2	mA
		T_a = 25 °C ADC operating at 80 MHz $V_{DD\_HV\_ADC}$ = 3.6 V	—	1	2	
$I_{DD\_HV\_FLASH}$[12]	Flash Operating current during read access	T_a = 125 °C[5] 3.3 V supplies 160 MHz frequency	—	40	45	mA
		T_a = 105 °C 3.3 V supplies 160 MHz frequency	—	40	45	
		T_a = 85 °C 3.3 V supplies 160 MHz frequency	—	40	45	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Single e200Z4 core cache disabled @80 MHz, no FlexRay, no ENET, 2 x CAN, 8 LINFlexD, 2 SPI, ADC0 and 1 used constantly, no HSM, Memory: 2M flash, 128K RAM RUN mode, Clocks: FIRC on, XOSC, PLL on, SIRC on for TOD, no 32KHz crystal (TOD runs off SIRC).
3. Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C. In case of internal ballast mode, it is expected that the external ballast is not mounted and BAL_SELECT_INT pin is tied to VDD_HV_A supply on board. Internal ballast can be used for all use cases with current consumption upto 150mA
4. The power consumption does not consider the dynamic current of I/Os
5. Tj=150°C. Assumes Ta=125°C
   - Assumes maximum θJA of 2s2p board. SeeThermal attributes
6. e200Z4 core, 160MHz, cache enabled; e200Z2 core , 80MHz, no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 256K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
7. e200Z4 core, 120MHz, cache enabled; e200Z2 core, 60MHz; no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 128K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal

8. e200Z4 core, 160MHz, cache enabled; e200Z4 core, 80MHz; HSM fully operational (Z0 core @80MHz) FlexRay, 5x CAN, 5x LINFlexD, 2x SPI, 1x ADC used constantly, 1xeMIOS (5 ch), Memory: 3M flash, 384K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
9. Assuming Ta=Tj, as the device is in Stop mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes.
10. Internal structures hold the input voltage less than $V_{DD\_HV\_ADC\_REF}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
11. This value is the total current for two ADCs.Each ADC might consume upto 2mA at max.
12. This assumes the default configuration of flash controller register. For more details, refer to Flash memory program and erase specifications

Table 11. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
LPU_RUN	with 256K RAM	T_a = 25 °C SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF	—	10	—	mA
		T_a = 85 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	10.5	—	
		T_a = 105 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	11	—	
		T_a = 125 °C[2, 2] SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	—	26	
LPU_STOP	with 256K RAM	T_a = 25 °C	—	0.18	—	mA
		T_a = 85 °C	—	0.60	—	
		T_a = 105 °C	—	1.00	—	
		T_a = 125 °C [2]	—	—	10.6	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

Table 12. STANDBY Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
STANDBY0	STANDBY with 8K RAM	T_a = 25 °C	—	71	—	µA
		T_a = 85 °C	—	125	700	
		T_a = 105 °C	—	195	1225	
		T_a = 125 °C [2, 2]	—	314	2100	
STANDBY1	STANDBY with 64K RAM	T_a = 25 °C	—	72	—	µA
		T_a = 85 °C	—	140	715	
		T_a = 105 °C	—	225	1275	
		T_a = 125 °C [2]	—	358	2250	

Table continues on the next page...

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 14. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry[2]	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01[3]
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00[3]
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input)[4]		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.
3. Slew rate control modes
4. Input slope = 2ns

NOTE

The specification given above is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The specification given above is measured between 20% / 80%.

5.3 AC specifications @ 5 V Range

Table 16. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		4.5/4.5		1.3/1.2	25	11
		6/6		2.5/2	50	
		13/13		9/9	200	
		5.25/5.25		3/2	25	10
		9/8		5/4	50	
		22/22		18/16	200	
		27/27		13/13	50	01[2, 2]
		40/40		24/24	200	
		40/40		24/24	50	00[2]
		65/65		40/40	200	
pad_i_hv/ pad_sr_hv (input)		1.5/1.5		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V

Table continues on the next page...

Table 17. DC electrical specifications @ 5 V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Vil (pad_i_hv)	pad_i_hv Input Buffer Low Voltage	VDD_HV_x - 0.3	0.45*VDD_HV_x	V
Vhys (pad_i_hv)	pad_i_hv Input Buffer Hysteresis	0.09*VDD_HV_x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65* VDD_HV_x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VDD_HV_x - 0.3	0.35*VDD_HV_x	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * VDD_HV_x[1, 1]	VDD_HV_x[1] + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VDD_HV_x - 0.3	0.40 * VDD_HV_x[1]	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x[1]		V
Pull_IIH (pad_i_hv)	Weak Pullup Current[2, 2] Low	23		µA
Pull_IIH (pad_i_hv)	Weak Pullup Current[3, 3] High		82	µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[3] Low	40		µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[2] High		130	µA
Pull_Ioh	Weak Pullup Current[4]	30	80	µA
Pull_Iol	Weak Pulldown Current[5]	30	80	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[6]	0.8 * VDD_HV_x[1]	—	V
Vol	Output Low Voltage[7] Output Low Voltage[8]	—	0.2*VDD_HV_x 0.1*VDD_HV_x	V
Ioh_f	Full drive Ioh[9, 9] (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

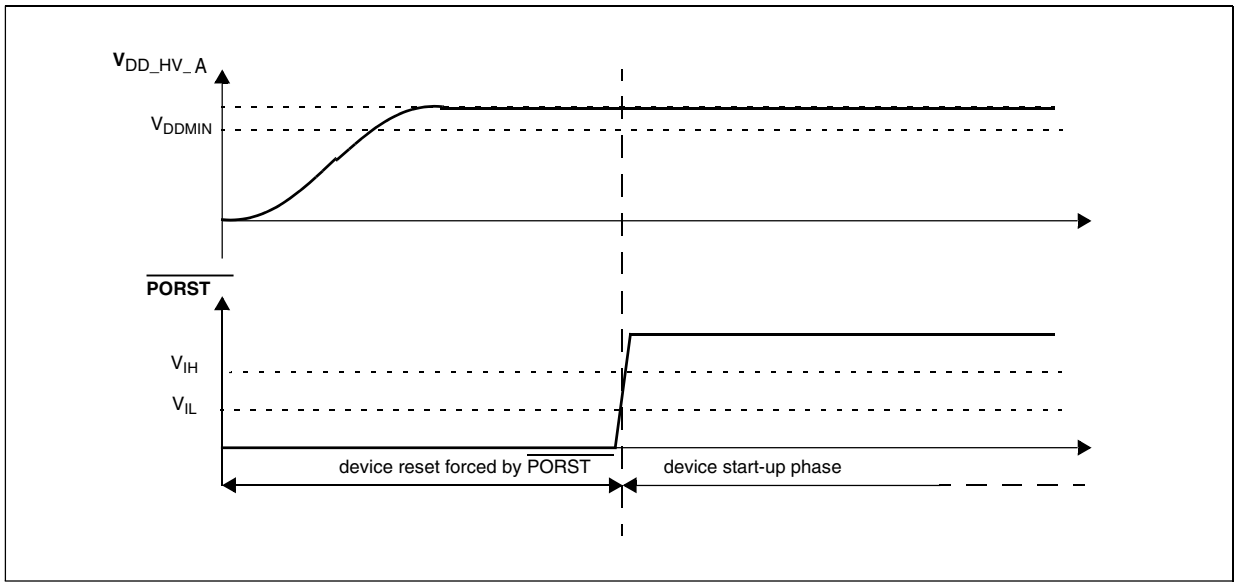


Figure 3. Start-up reset requirements

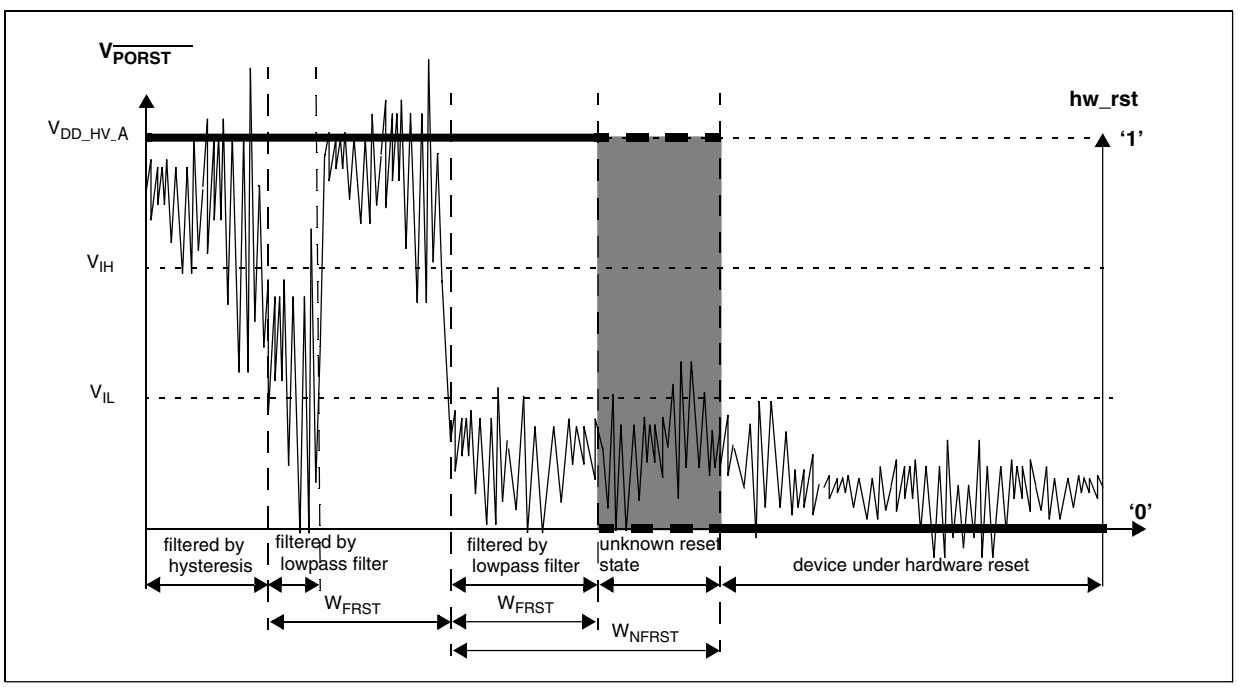


Figure 4. Noise filtering on reset signal

Table 18. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	CMOS Input Buffer High Voltage	—	$0.65*V_{DD\_HV\_x}$	—	$V_{DD\_HV\_x}$ +0.3	V
V_{IL}	CMOS Input Buffer Low Voltage	—	$V_{DD\_HV\_x}$-0.3	—	$0.35*V_{DD\_HV\_x}$	V

Table continues on the next page...

Table 23. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
	Oscillator Analog Circuit supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		
		LCP	8 MHz		141		uA
			16 MHz		252		
			40 MHz		518		
V_{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3	1.95			V
V_{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3			1.25	V

1. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board.
2. Typ value for oscillator supply 3.3 V@27 °C

6.2.2 32 kHz Oscillator electrical specifications

Table 24. 32 kHz oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{osc_lo}	Oscillator crystal or resonator frequency		32		40	KHz
t_{cst}	Crystal Start-up Time[1, 2]				2	s

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 16 MHz RC Oscillator electrical specifications

Table 25. 16 MHz RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F_{Target}	IRC target frequency	—	—	16	—	MHz
PTA	IRC frequency variation after trimming	—	-5	—	5	%
$T_{startup}$	Startup time	—		—	1.5	us
T_{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T_{LTJIT}	Long term jitter		—	—	0.2	%

Table 28. Jitter calculation (continued)

Type of jitter	Jitter due to Supply Noise (ps) J_{SN}[1]	Jitter due to Fractional Mode (ps) J_{SDM}[2]	Jitter due to Fractional Mode J_{SSCG} (ps) [3]	1 Sigma Random Jitter J_{RJ} (ps) [4]	Total Period Jitter (ps)
Long Term Jitter (Integer Mode)				40	+/-(N x J_{RJ})
Long Term jitter (Fractional Mode)				100	+/-(N x J_{RJ})

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on VDD_LV and VSS_LV.
2. This jitter component is added when the PLL is working in the fractional mode.
3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.
4. The value of N is dependent on the accuracy requirement of the application. See Table 29

Table 29. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27
4	6.30 × 1e-03
5	5.63 × 1e-05
6	2.00 × 1e-07
7	2.82 × 1e-10

6.3 Memory interfaces

6.3.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.

Table 31. Flash memory Array Integrity and Margin Read specifications (continued)

Symbol	Characteristic	Min	Typical	Max[1, 1]	Units[2, 2]
$t_{ai256kseq}$	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

6.3.3 Flash memory module life specifications

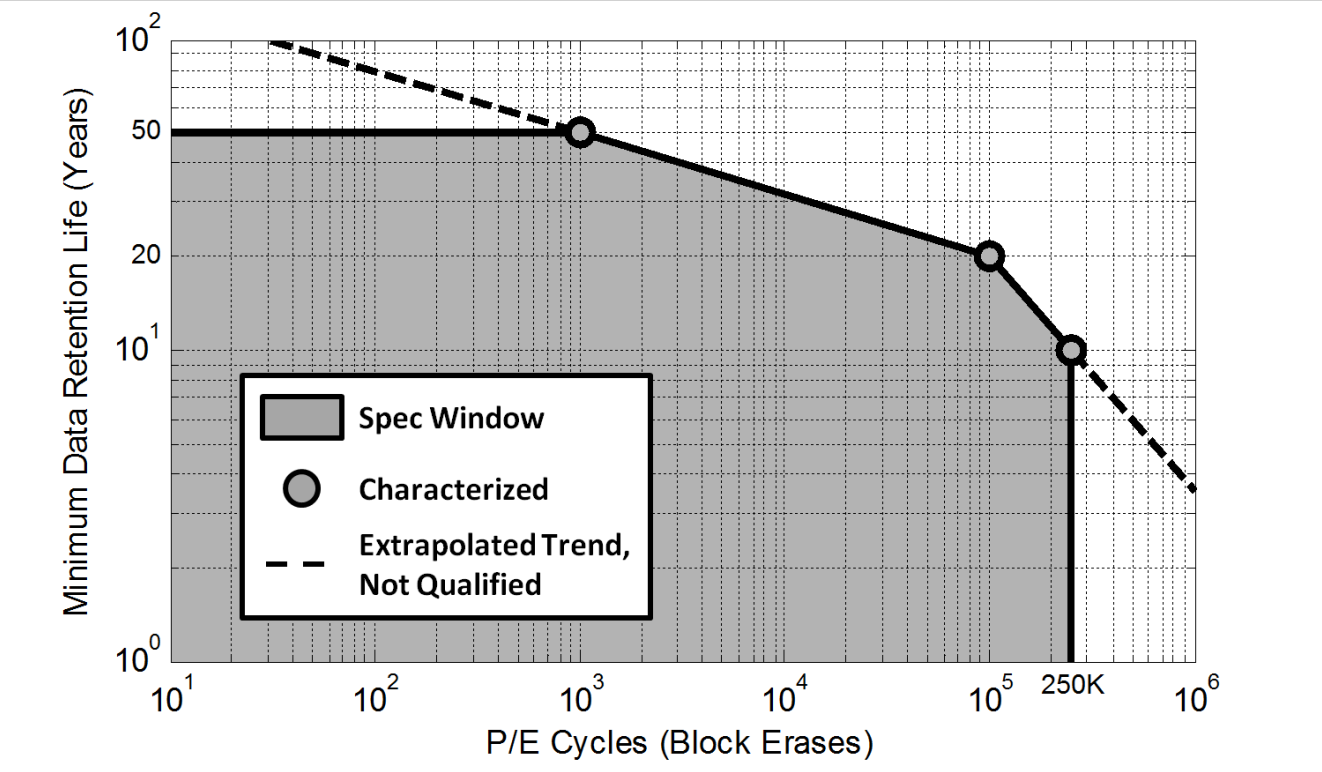
Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1, 1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2, 2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

6.3.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



6.3.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs

Table continues on the next page...

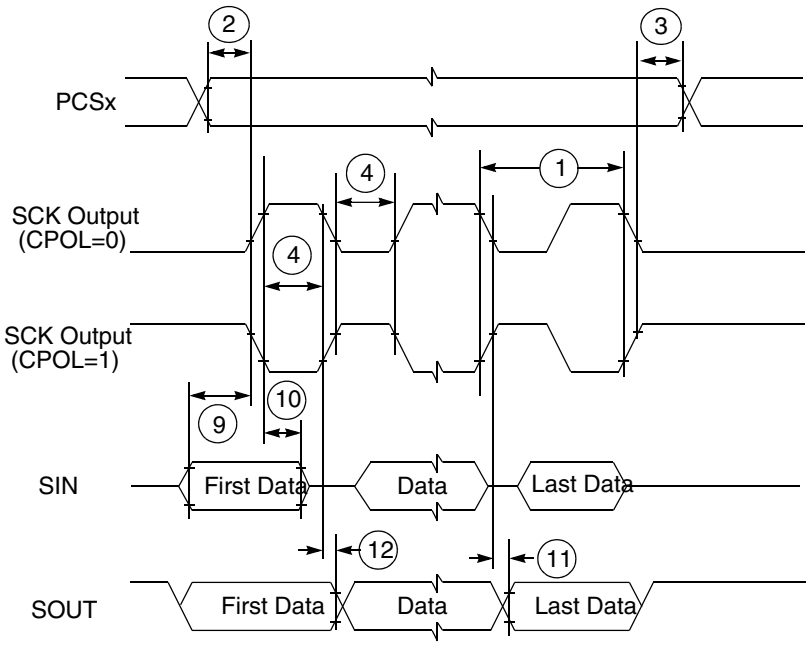


Figure 8. DSPI classic SPI timing — master, CPHA = 0

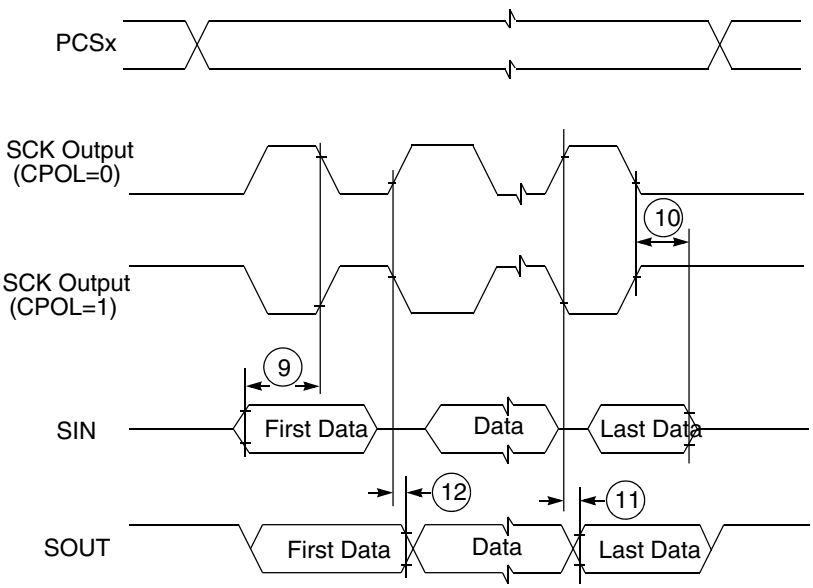


Figure 9. DSPI classic SPI timing — master, CPHA = 1

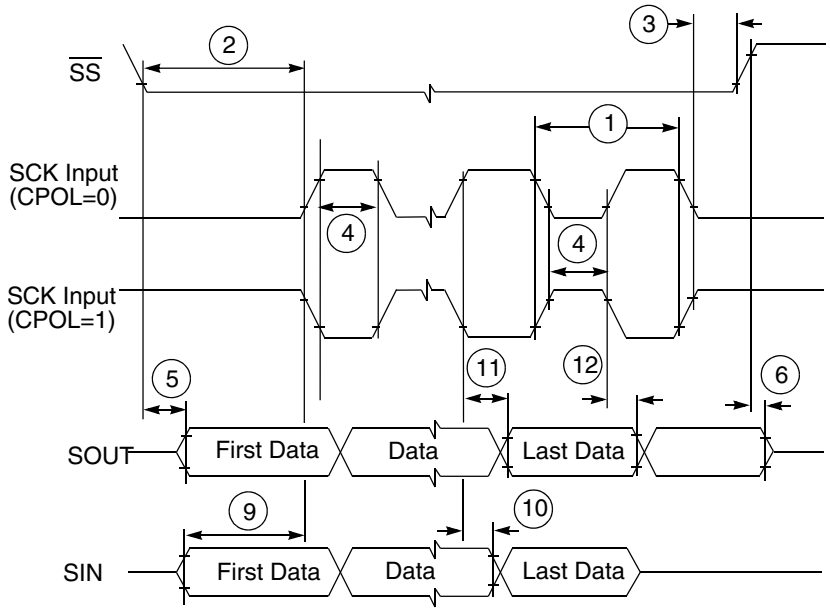


Figure 14. DSPI modified transfer format timing – slave, CPHA = 0

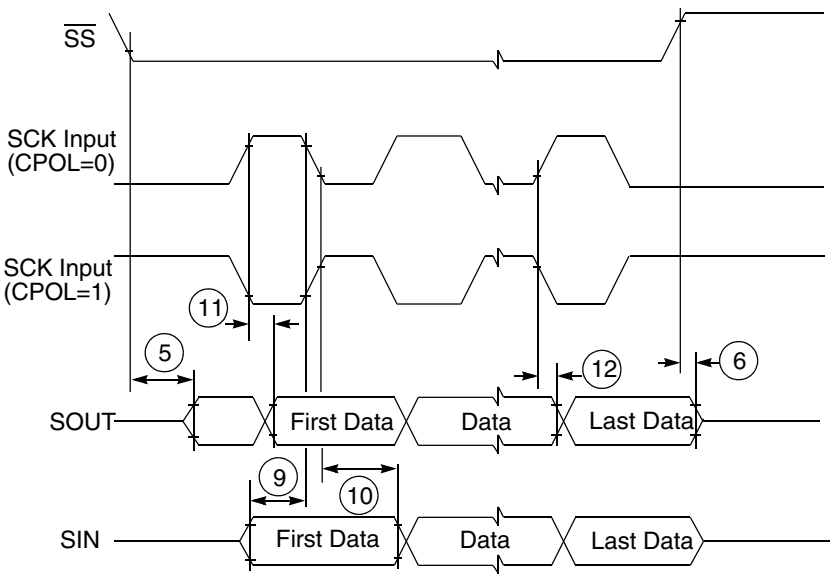


Figure 15. DSPI modified transfer format timing — slave, CPHA = 1

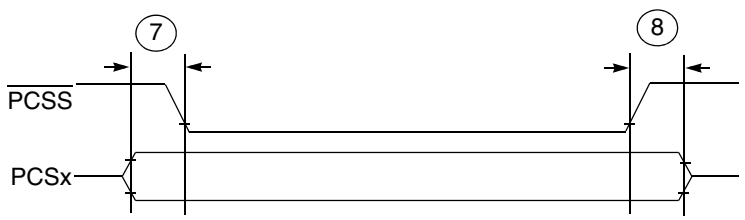


Figure 16. DSPI PCS strobe (PCSS) timing

Table 45. JTAG pin AC electrical characteristics [1] (continued)

#	Symbol	Characteristic	Min	Max	Unit
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

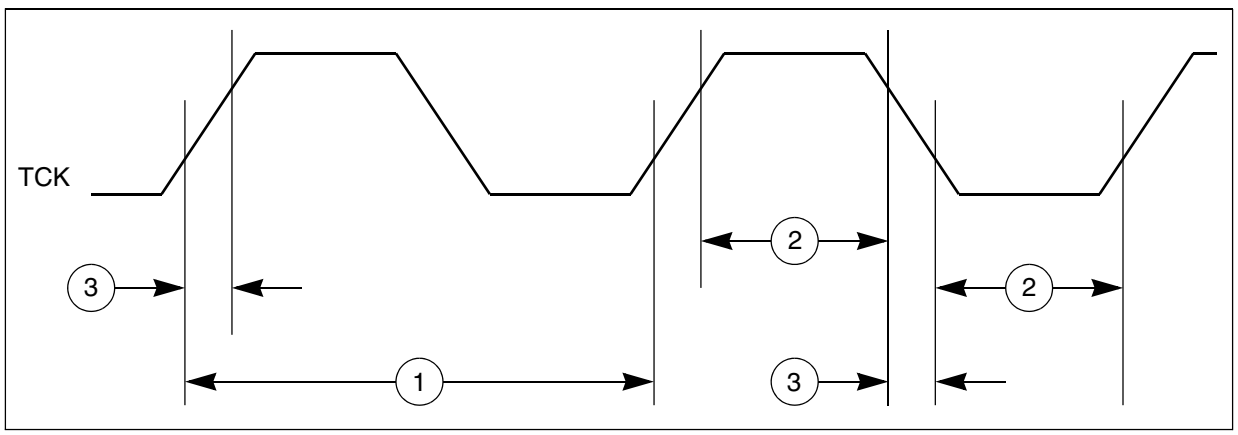


Figure 25. JTAG test clock input timing

Table 46. Nexus debug port timing [1] (continued)

No.	Symbol	Parameter	Conditions	Min	Max	Unit
9	t_{NTDIH}, t_{NTMSH}	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

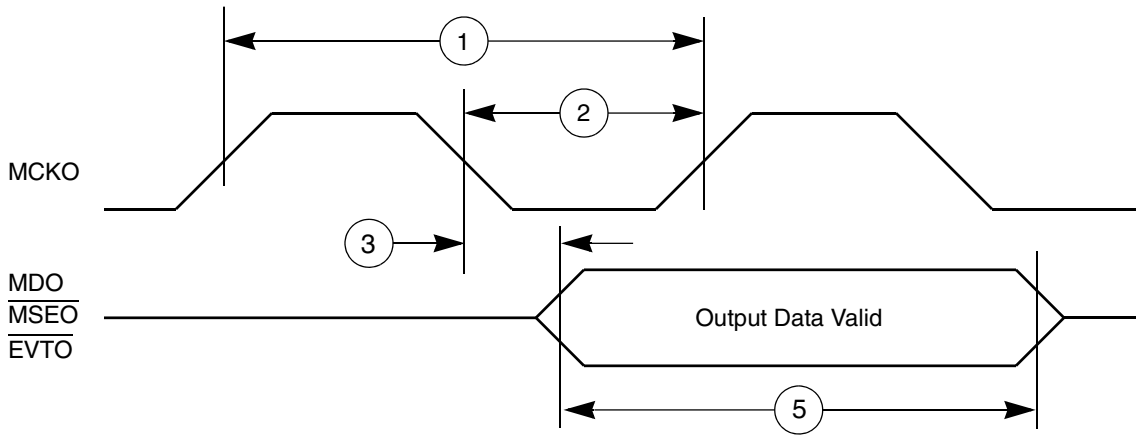


Figure 28. Nexus output timing

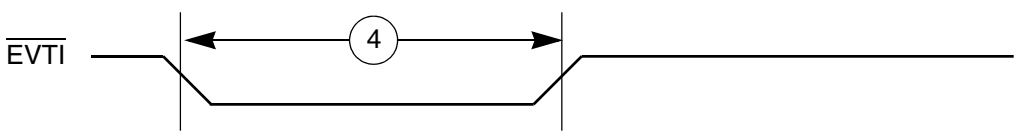


Figure 29. Nexus EVTI Input Pulse Width

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

Rev 2	7 August 2015	• In features:
		  • Updated BAF feature with sentence, Boot Assist Flash (BAF) supports internal flash programming via a serial link (SCI)
		  • Updated FlexCAN3 with FD support
		  • Updated number of STMs to two.
		• In Block diagram:
		  • Updated SRAM size from 128 KB to 256 KB.
		• In Family Comparison:
		  • Added note: All optional features (Flash memory, RAM, Peripherals) start with lowest number or address (e.g. FlexCAN0) and end at highest available number or address (e.g. MPC574xB/D have 6 CAN, ending with FlexCAN5).
		  • Revised MPC5746C Family Comparison table.
		• In Ordering parts:
		  • Updated ordering parts diagram to include 100 MAPBGA information and optional fields.
		• In table: Absolute maximum ratings
		  • Removed entry: 'V_{SS_HV}'
		  • Added spec for 'V_{DD12}'
		  • Updated 'Max' column for 'V_{INA}'
		  • Updated footnote for $V_{DD\_HV\_ADC1\_REF}$.
		  • Added footnote to 'Conditions', All voltages are referred to V_{SS_HV} unless otherwise specified
		  • Removed footnote from 'Max', Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
		• In section: Recommended operating conditions
		  • Added opening text: "The following table describes the operating conditions ... "
		  • Added note: "$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ are all ... "
		  • In table: Recommended operating conditions (VDD_HV_x = 3.3 V) and (VDD_HV_x = 5 V)
		  • Added footnote to 'Conditions' cloumn, (All voltages are referred to V_{SS_HV} unless otherwise specified).
		  • Updated footnote for 'Min' column to Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
		  • Removed footnote for '$V_{DD\_HV\_A}$', '$V_{DD\_HV\_B}$', and '$V_{DD\_HV\_C}$' entry and updated the parameter column.
		  • Removed entry : 'V_{SS_HV}'
		  • Updated 'Parameter' column for '$V_{DD\_HV\_FLA}$', '$V_{DD\_HV\_ADC1\_REF}$', 'V_{DD_LV}'
		  • Updated 'Min' column for '$V_{DD\_HV\_ADC0}$' '$V_{DD\_HV\_ADC1}$'
		  • Updated 'Parameter' 'Min' 'Max' columns for '$V_{SS\_HV\_ADC0}$' and '$V_{SS\_HV\_ADC1}$'
		  • Updated footnote for 'V_{DD_LV} ' to V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
		  • Removed row for symbol 'V_{SS_LV}'
		  • Removed footnote from 'Max' column of '$V_{DD\_HV\_ADC0}$' and '$V_{DD\_HV\_ADC1}$', (PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1).
		  • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)
		  • Removed footnote from '$V_{IN1\_CMP\_REF}$', (Only applicable when supplying from external source).
		  • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 5 V)
		  • Added spec for '$V_{IN1\_CMP\_REF}$' and corresponding footnotes.

Table continues on the next page...

Table 51. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In section: Voltage monitor electrical characteristics
		  • Updated description for Low Voltage detector block.
		  • Added note, BCP56, MCP68 and MJD31 are guaranteed ballasts.
		  • In table: Voltage regulator electrical specifications
		  • Added footnote, Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
		  • Revised table, Voltage monitor electrical characteristics

		• In section: Supply current characteristics
		  • In table: Current consumption characteristics
		  • $I_{DD\_BODY\_4}$: Updated SYS_CLK to 120 MHz.
		  • $I_{DD\_BODY\_4}$: Updated Max for T_a= 105 °C fand 85 °C)
		  • I_{dd_STOP}: Added condition for T_a= 105 °C and removed Max value for T_a= 85 °C.
		  • $I_{DD\_HV\_ADC\_REF}$: Added condition for T_a= 105 °C and 85 °C and removed Max value for T_a= 25 °C.
		  • $I_{DD\_HV\_FLASH}$: Added condition for T_a= 105 °C and 85 °C
		  • In table: Low Power Unit (LPU) Current consumption characteristics
		  • LPU_RUN and LPU_STOP: Added condition for T_a= 105 °C and 85 °C
		  • In table: STANDBY Current consumption characteristics
		  • Added condition for T_a= 105 °C and 85 °C for all entries.
		
		• In section: I/O parameters
		  • In table: Functional Pad AC Specifications @ 3.3 V Range
		  • Updated values for 'pad_sr_hv (output)'
		  • In table: DC electrical specifications @ 3.3V Range
		  • Updateded Min and Max values for Vih and Vil respectively.
		  • In table: Functional Pad AC Specifications @ 5 V Range
		  • Updated values for 'pad_sr_hv (output)'
		  • In table DC electrical specifications @ 5 V Range
		  • Updated Min value for Vhys

Table continues on the next page...