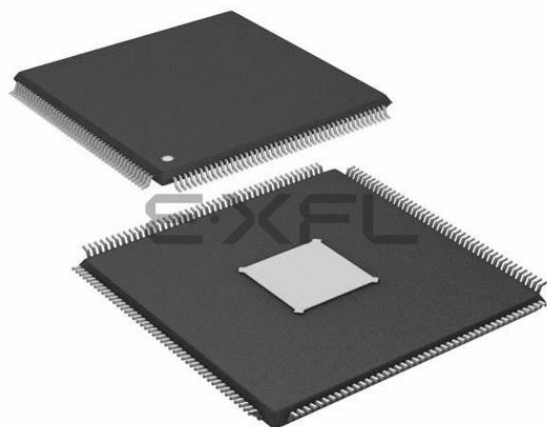




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746csk1amku6

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Table 2. MPC5746C Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW partition	MPC5744	MPC5745	MPC5746
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	not available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	7	not available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	7	not available	not available	available
0x011C0000	0x011FFFFFFF	256 KB code Flash block 7	7	not available	not available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	not available	not available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	not available	not available	not available

Table 3. MPC5746C Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW partition	MPC5744B MPC5745B MPC5746B	MPC5744C MPC5745C MPC5746C
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	not available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	not available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	not available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	not available	available

Table 4. MPC5746C Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40000000	0x40001FFF	8 KB	SRAM0	available	available	available
0x40002000	0x4000FFFF	56 KB	SRAM1	available	available	available
0x40010000	0x4001FFFF	64 KB	SRAM2	available	available	available
0x40020000	0x4002FFFF	64 KB	SRAM3	available	available	available

Table continues on the next page...

Table 4. MPC5746C Family Comparison - RAM Memory Map (continued)

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40030000	0x4003FFFF	64 KB	SRAM4	not available	available	available
0x40040000	0x4004FFFF	64 KB	SRAM5	not available	not available	available
0x40050000	0x4005FFFF	64 KB	SRAM6	not available	not available	available
0x40060000	0x4006FFFF	64 KB	SRAM7	not available	not available	optional
0x40070000	0x4007FFFF	64 KB	SRAM8	not available	not available	optional

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5746C.

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

NOTE

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FL A should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FL A should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

Table 6. Recommended operating conditions (V_{DD_HV_x} = 3.3 V)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
V _{DD_HV_A} V _{DD_HV_B} V _{DD_HV_C}	HV IO supply voltage	—	3.15	3.6	V
V _{DD_HV_FL A} ³	HV flash supply voltage	—	3.15	3.6	V
V _{DD_HV_ADC1_REF}	HV ADC1 high reference voltage	—	3.0	5.5	V
V _{DD_HV_ADC0} V _{DD_HV_ADC1}	HV ADC supply voltage	—	max(V _{DD_HV_A} , V _{DD_HV_B} , V _{DD_HV_C}) - 0.05	3.6	V
V _{SS_HV_ADC0} V _{SS_HV_ADC1}	HV ADC supply ground	—	-0.1	0.1	V
V _{DD_LV} ^{4, 5}	Core supply voltage	—	1.2	1.32	V
V _{IN1_CMP_REF} ^{6, 7}	Analog Comparator DAC reference voltage	—	3.15	3.6	V
I _{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA

Table continues on the next page...

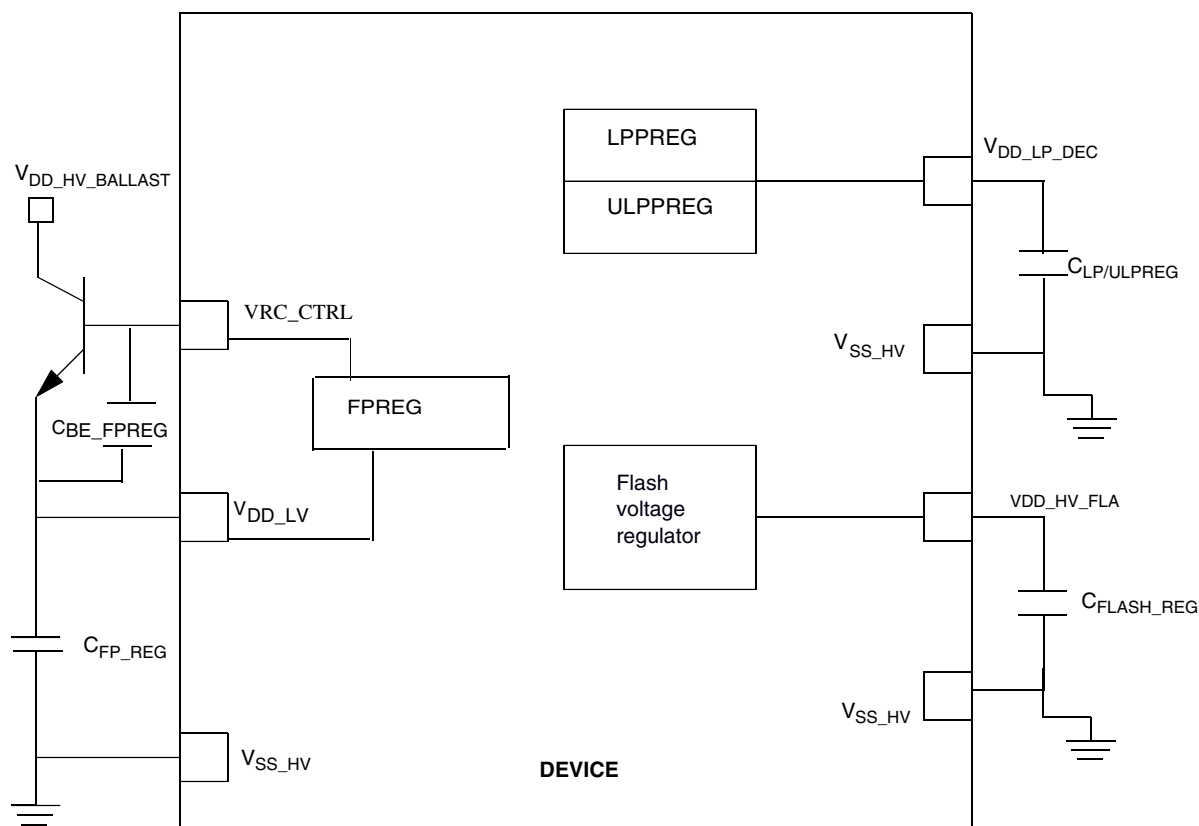


Figure 2. Voltage regulator capacitance connection

NOTE

On BGA, VSS_LV and VSS_HV have been joined on substrate and renamed as VSS.

Table 8. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _{fp_reg} ¹	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2 ²	3	μF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
C _{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	μF
	Combined ESR of external capacitor	—	0.001	—	0.1	Ohm
C _{be_fpreg} ³	Capacitor in parallel to base-emitter	BCP68 and BCP56		3.3		nF
		MJD31		4.7		

Table continues on the next page...

Table 8. Voltage regulator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{\text{flash_reg}}$ ⁴	External decoupling / stability capacitor for internal Flash regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2	3	μF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
$C_{\text{HV_VDD_A}}$	VDD_HV_A supply capacitor ^{5, 5}	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_VDD_B}}$	VDD_HV_B supply capacitor ⁵	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_VDD_C}}$	VDD_HV_C supply capacitor ⁵	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_ADC0}}$ $C_{\text{HV_ADC1}}$	HV ADC supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{\text{HV_ADR}}$ ⁶	HV ADC SAR reference supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.47	—	—	μF
$V_{\text{DD_HV_BALLAST}}^{\text{AST}}$ ⁷	FPREG Ballast collector supply voltage	When collector of NPN ballast is directly supplied by an on board supply source (not shared with VDD_HV_A supply pin) without any series resistance, that is, $R_{\text{C_BALLAST}}$ less than 0.01 Ohm.	2.25	—	5.5	V
$R_{\text{C_BALLAST}}$	Series resistor on collector of FPREG ballast	When VDD_HV_BALLAST is shorted to VDD_HV_A on the board	—	—	0.1	Ohm
t_{SU}	Start-up time with external ballast after main supply (VDD_HV_A) stabilization	$C_{\text{fp_reg}} = 3 \mu\text{F}$	—	74	—	μs
$t_{\text{SU_int}}$	Start-up time with internal ballast after main supply (VDD_HV_A) stabilization	$C_{\text{fp_reg}} = 3 \mu\text{F}$	—	103	—	μs
t_{ramp}	Load current transient	Iload from 15% to 55% $C_{\text{fp_reg}} = 3 \mu\text{F}$		1.0		μs

1. Split capacitance on each pair VDD_LV pin should sum up to a total value of $C_{\text{fp_reg}}$
2. Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.
3. Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
4. It is required to minimize the board parasitic inductance from decoupling capacitor to VDD_HV_FL A pin and the routing inductance should be less than 1nH.

Table 9. Voltage monitor electrical characteristics (continued)

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up ¹	Mask Opt ^{2, 2}	Reset Type	Min	Typ	Max	V
V _{LVD_LV_PD2_cold}	LV supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.1400	1.1550	1.1750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.1600	1.1750	1.1950	V

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.
3. There is no voltage monitoring on the V_{DD_HV_ADC0}, V_{DD_HV_ADC1}, V_{DD_HV_B} and V_{DD_HV_C} I/O segments. For applications requiring monitoring of these segments, either connect these to V_{DD_HV_A} at the PCB level or monitor externally.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 10. Current consumption characteristics

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
I _{DD_BODY_12, 3}	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies ^{4, 4} T _a = 125°C ^{5, 5} V _{DD_LV} = 1.25 V V _{DD_HV_A} = 5.5V SYS_CLK = 80MHz	—	—	147	mA
		T _a = 105°C	—	—	142	mA
		T _a = 85 °C	—	—	137	mA

Table continues on the next page...

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
$I_{DD_HV_ADC_REF}$ ^{10, 11, 11}	ADC REF Operating current	$T_a = 125\text{ }^{\circ}\text{C}$ ⁵ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 5.5\text{ V}$	—	200	400	μA
		$T_a = 105\text{ }^{\circ}\text{C}$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 5.5\text{ V}$	—	200	—	
		$T_a = 85\text{ }^{\circ}\text{C}$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 5.5\text{ V}$	—	200	—	
		$T_a = 25\text{ }^{\circ}\text{C}$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 3.6\text{ V}$	—	200	—	
$I_{DD_HV_ADCx}$ ¹¹	ADC HV Operating current	$T_a = 125\text{ }^{\circ}\text{C}$ ⁵ ADC operating at 80 MHz $V_{DD_HV_ADC} = 5.5\text{ V}$	—	1.2	2	mA
		$T_a = 25\text{ }^{\circ}\text{C}$ ADC operating at 80 MHz $V_{DD_HV_ADC} = 3.6\text{ V}$	—	1	2	
$I_{DD_HV_FLASH}$ ¹²	Flash Operating current during read access	$T_a = 125\text{ }^{\circ}\text{C}$ ⁵ 3.3 V supplies 160 MHz frequency	—	40	45	mA
		$T_a = 105\text{ }^{\circ}\text{C}$ 3.3 V supplies 160 MHz frequency	—	40	45	
		$T_a = 85\text{ }^{\circ}\text{C}$ 3.3 V supplies 160 MHz frequency	—	40	45	

- The content of the Conditions column identifies the components that draw the specific current.
- Single e200Z4 core cache disabled @80 MHz, no FlexRay, no ENET, 2 x CAN, 8 LINFlexD, 2 SPI, ADC0 and 1 used constantly, no HSM, Memory: 2M flash, 128K RAM RUN mode, Clocks: FIRC on, XOSC, PLL on, SIRC on for TOD, no 32KHz crystal (TOD runs off SIRC).
- Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C. In case of internal ballast mode, it is expected that the external ballast is not mounted and BAL_SELECT_INT pin is tied to VDD_HV_A supply on board. Internal ballast can be used for all use cases with current consumption upto 150mA
- The power consumption does not consider the dynamic current of I/Os
- $T_j=150^{\circ}\text{C}$. Assumes $T_a=125^{\circ}\text{C}$
 - Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#)
- e200Z4 core, 160MHz, cache enabled; e200Z2 core , 80MHz, no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 256K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
- e200Z4 core, 120MHz, cache enabled; e200Z2 core, 60MHz; no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 128K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal

8. e200Z4 core, 160MHz, cache enabled; e200Z4 core, 80MHz; HSM fully operational (Z0 core @80MHz) FlexRay, 5x CAN, 5x LINFlexD, 2x SPI, 1x ADC used constantly, 1x eMIOS (5 ch), Memory: 3M flash, 384K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
9. Assuming $T_a = T_j$, as the device is in Stop mode. Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#).
10. Internal structures hold the input voltage less than $V_{DD_HV_ADC_REF} + 1.0$ V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
11. This value is the total current for two ADCs. Each ADC might consume upto 2mA at max.
12. This assumes the default configuration of flash controller register. For more details, refer to [Flash memory program and erase specifications](#)

Table 11. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
LPU_RUN	with 256K RAM	$T_a = 25\text{ }^{\circ}\text{C}$ SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF	—	10	—	mA
		$T_a = 85\text{ }^{\circ}\text{C}$ SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	10.5	—	
		$T_a = 105\text{ }^{\circ}\text{C}$ SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	11	—	
		$T_a = 125\text{ }^{\circ}\text{C}$ ^{2, 2} SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	—	26	
LPU_STOP	with 256K RAM	$T_a = 25\text{ }^{\circ}\text{C}$	—	0.18	—	mA
		$T_a = 85\text{ }^{\circ}\text{C}$	—	0.60	—	
		$T_a = 105\text{ }^{\circ}\text{C}$	—	1.00	—	
		$T_a = 125\text{ }^{\circ}\text{C}$ ²	—	—	10.6	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming $T_a = T_j$, as the device is in static (fully clock gated) mode. Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#)

Table 12. STANDBY Current consumption characteristics

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
STANDBY0	STANDBY with 8K RAM	$T_a = 25\text{ }^{\circ}\text{C}$	—	71	—	μA
		$T_a = 85\text{ }^{\circ}\text{C}$	—	125	700	
		$T_a = 105\text{ }^{\circ}\text{C}$	—	195	1225	
		$T_a = 125\text{ }^{\circ}\text{C}$ ^{2, 2}	—	314	2100	
STANDBY1	STANDBY with 64K RAM	$T_a = 25\text{ }^{\circ}\text{C}$	—	72	—	μA
		$T_a = 85\text{ }^{\circ}\text{C}$	—	140	715	
		$T_a = 105\text{ }^{\circ}\text{C}$	—	225	1275	
		$T_a = 125\text{ }^{\circ}\text{C}$ ²	—	358	2250	

Table continues on the next page...

5.2 DC electrical specifications @ 3.3V Range

Table 15. DC electrical specifications @ 3.3V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	Pad_I_HV Input Buffer High Voltage	$0.72 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil (pad_i_hv)	Pad_I_HV Input Buffer Low Voltage	$VDD_HV_x - 0.3$	$0.45 \cdot VDD_HV_x$	V
Vhys (pad_i_hv)	Pad_I_HV Input Buffer Hysteresis	$0.11 \cdot VDD_HV_x$		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	$0.67 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	$VDD_HV_x - 0.3$	$0.35 \cdot VDD_HV_x$	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	$0.57 \cdot VDD_HV_x^{1,1}$	$VDD_HV_x^{1,1} + 0.3$	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	$VDD_HV_x - 0.3$	$0.4 \cdot VDD_HV_x^{1,1}$	V
Vhys	CMOS Input Buffer Hysteresis	$0.09 \cdot VDD_HV_x^{1,1}$		V
Pull_IH (pad_i_hv)	Weak Pullup Current ^{2,2} Low	15		μA
Pull_IH (pad_i_hv)	Weak Pullup Current ^{3,3} High		55	μA
Pull_IL (pad_i_hv)	Weak Pulldown Current ³ Low	28		μA
Pull_IL (pad_i_hv)	Weak Pulldown Current ² High		85	μA
Pull_Ioh	Weak Pullup Current ⁴	15	50	μA
Pull_Iol	Weak Pulldown Current ⁵	15	50	μA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	μA
Voh	Output High Voltage ⁶	$0.8 \cdot VDD_HV_x^{1,1}$	—	V
Vol	Output Low Voltage ⁷ Output Low Voltage ⁸	—	$0.2 \cdot VDD_HV_x^{1,1}$ $0.1 \cdot VDD_HV_x$	V
Ioh_f	Full drive Ioh ^{9,9} (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol ⁹ (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh ⁹ (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol ⁹ (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

1. $VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C$

2. Measured when pad = $0.69 \cdot VDD_HV_x$

3. Measured when pad = $0.49 \cdot VDD_HV_x$

4. Measured when pad = 0 V

5. Measured when pad = VDD_HV_x

6. Measured when pad is sourcing 2 mA

7. Measured when pad is sinking 2 mA

8. Measured when pad is sinking 1.5 mA

9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.3 AC specifications @ 5 V Range

Table 16. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. Delay (ns) ¹ L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCrN[Src 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		4.5/4.5		1.3/1.2	25	11
		6/6		2.5/2	50	
		13/13		9/9	200	
		5.25/5.25		3/2	25	10
		9/8		5/4	50	
		22/22		18/16	200	
		27/27		13/13	50	01 ^{2, 2}
		40/40		24/24	200	
		40/40		24/24	50	00 ²
		65/65		40/40	200	
pad_i_hv/ pad_sr_hv (input)		1.5/1.5		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output

2. Slew rate control modes

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V

Table continues on the next page...

Table 21. ADC conversion characteristics (for 10-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
t_{conv}	Conversion time ⁴	80 MHz	550	—	—	ns
t_{total_conv}	Total Conversion time $t_{sample} + t_{conv}$ (for standard channels)	80 MHz	1	—	—	μs
	Total Conversion time $t_{sample} + t_{conv}$ (for extended channels)		1.5	—	—	
C_S ⁵	ADC input sampling capacitance	—	—	3	5	pF
C_{P1} ⁵	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2} ⁵	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1} ⁵	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	k Ω
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD} ⁵	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max positive/negative injection		–5	—	5	mA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
$TUE_{standard/extended}$ channels	Total unadjusted error for standard channels	Without current injection	–4	+/-3	4	LSB
		With current injection ⁶		+/-4		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	μs

1. Active ADC Input, $V_{inA} < [\min(ADC_ADV, IO_Supply_A,B,C)]$. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO_supply_A , B, C and ADC_Supply .
2. The internally generated clock (known as AD_clk or $ADCK$) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See [Figure 65](#)
6. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (V_{INA} , see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

6.1.2 Analog Comparator (CMP) electrical specifications

Table 22. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	μA
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	μA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1_CMP_REF}$	V
V_{AIO}	Analog input offset voltage ^{1, 1}	-47	—	47	mV
V_H	Analog comparator hysteresis ^{2, 2} - CR0[HYSTCTR] = 00 - CR0[HYSTCTR] = 01 - CR0[HYSTCTR] = 10 - CR0[HYSTCTR] = 11	—	1	25	mV
		—	20	50	mV
		—	40	70	mV
		—	60	105	mV
		—	—	—	—
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) ^{1, 3, 3}	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) ^{1, 3}	—	5	21	μs
	Analog comparator initialization delay, High speed mode ^{4, 4}	—	4		μs
	Analog comparator initialization delay, Low speed mode ⁴	—	100		μs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	μA
	5V Reference Voltage	—	10	16	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ⁵
DNL	6-bit DAC differential non-linearity	-0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD_HV_A}-0.6V$
3. Full swing = V_{IH} , V_{IL}
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

6.4.2.2 TxEN

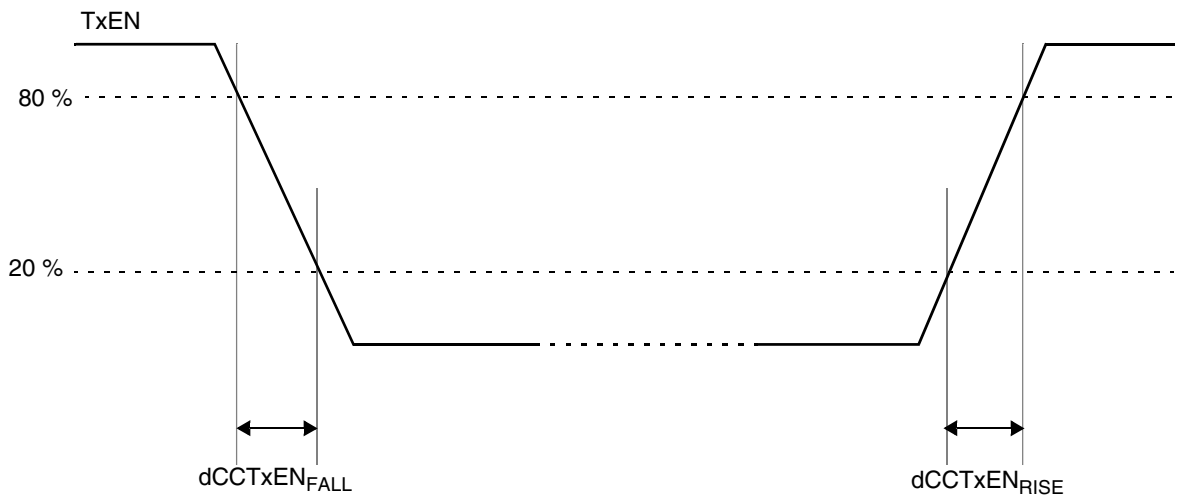


Figure 17. TxEN signal

Table 38. TxEN output characteristics¹

Name	Description	Min	Max	Unit
dCCTxEN _{RISE25}	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN _{FALL25}	Fall time of TxEN signal at CC	—	9	ns
dCCTxEN ₀₁	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxEN ₁₀	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD_HV_IOx} = 3.3\text{ V} \pm 5\%, \pm 10\%$, $T_J = -40\text{ }^{\circ}\text{C} / 150\text{ }^{\circ}\text{C}$, TxEN pin load maximum 25 pF

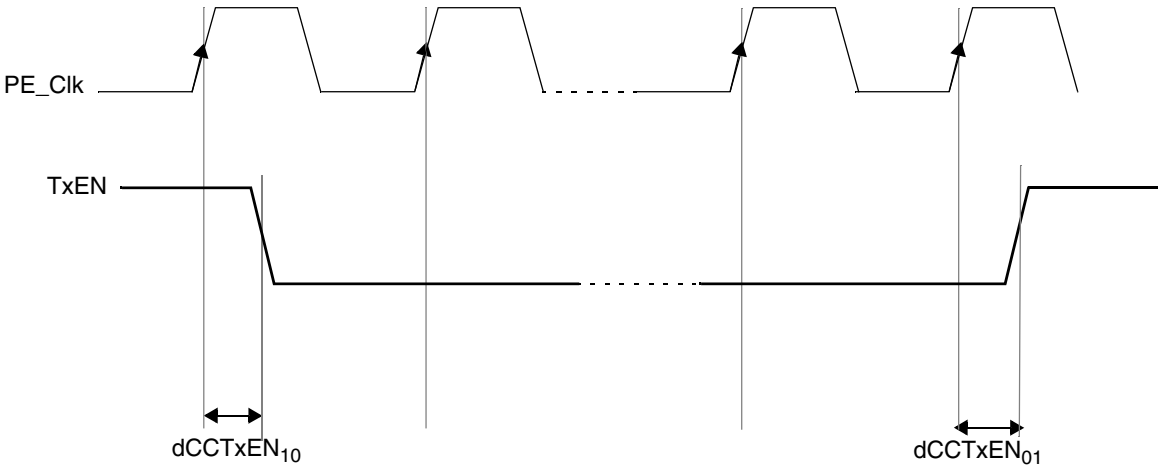


Figure 18. TxEN signal propagation delays

6.4.2.3 TxD

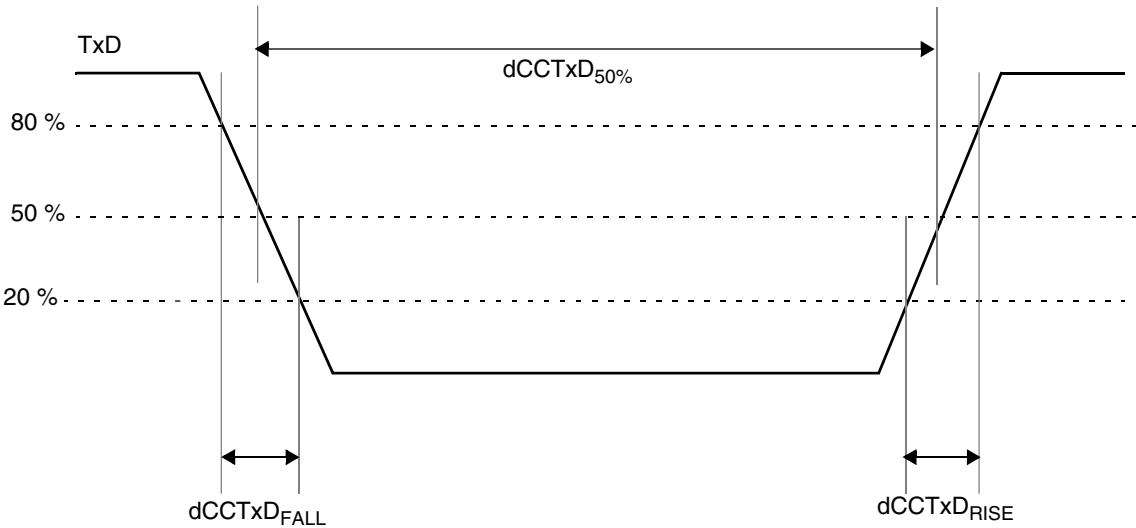


Figure 19. TxD Signal

Table 39. TxD output characteristics

Name	Description ¹	Min	Max	Unit
dCCT _{xAsym}	Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns)	-2.45	2.45	ns
dCCTxD _{RISE25} +dCCTxD _{FALL25}	Sum of Rise and Fall time of TxD signal at the output	—	9 ²	ns

Table continues on the next page...

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = -40 oC / 150 oC.

6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 41. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

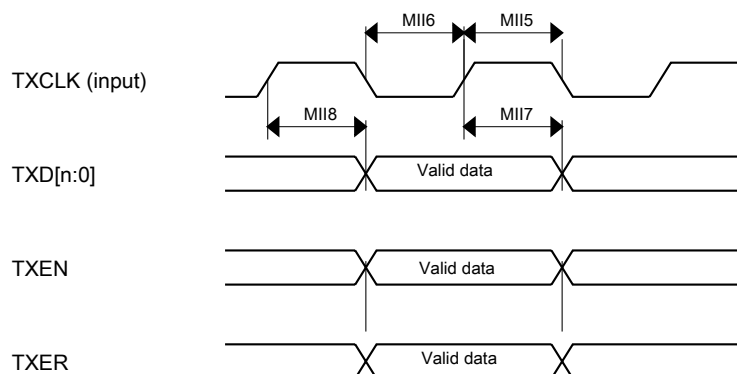


Figure 21. RMII/MII transmit signal timing diagram

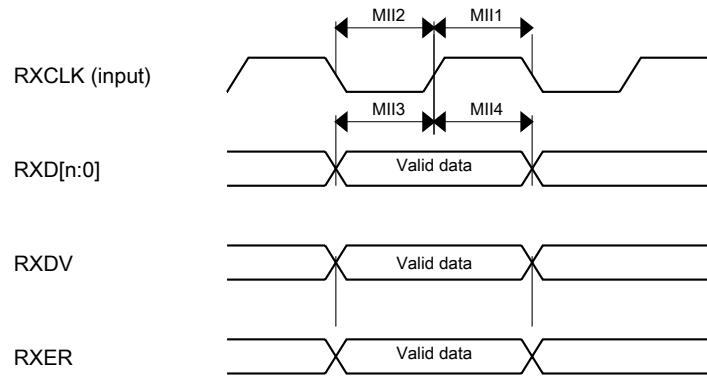


Figure 22. RMII/MII receive signal timing diagram

6.4.3.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 42. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

6.4.4 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 43. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns

Table continues on the next page...

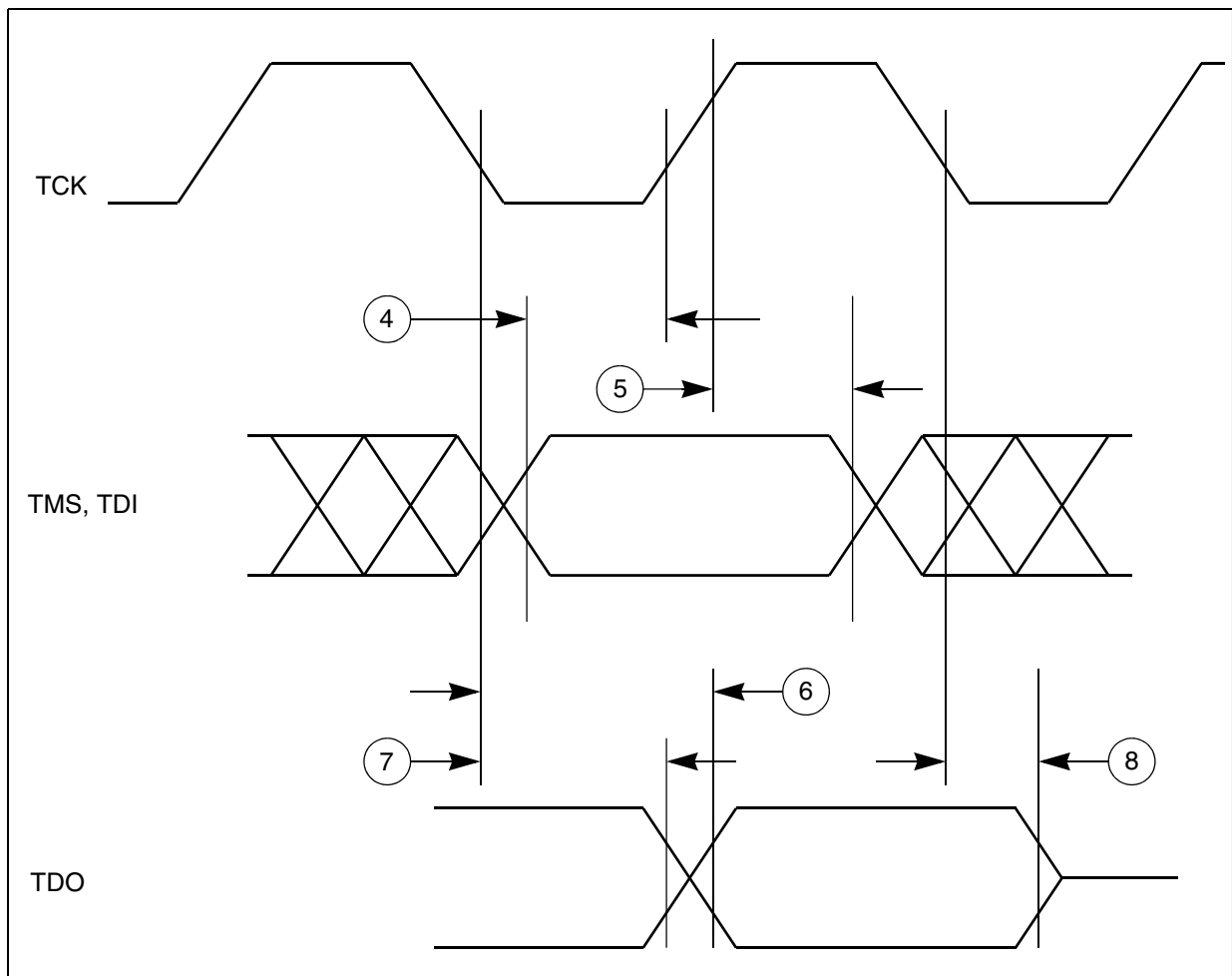


Figure 26. JTAG test access port timing

10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

Table 50. BAF execution duration

BAF execution duration	Min	Typ	Max	Unit
BAF execution time (boot header at first location)	—	200	—	μs
BAF execution time (boot header at last location)	—	—	320	μs

10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

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