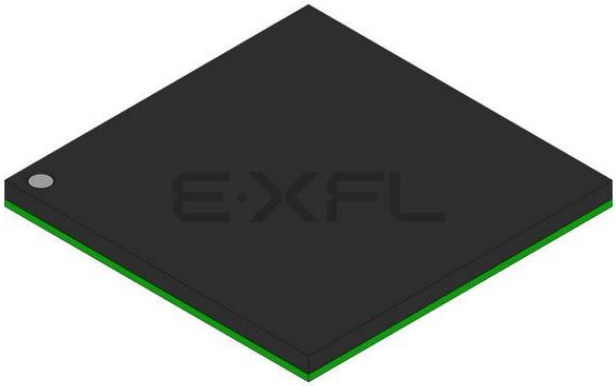

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z2, e200z4 |
| Core Size | 32-Bit Dual-Core |
| Speed | 80MHz/160MHz |
| Connectivity | CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG |
| Peripherals | DMA, LVD, POR, WDT |
| Number of I/O | 178 |
| Program Memory Size | 3MB (3M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 80x10b, 64x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-MAPPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5746csk1mmj6 |

- Debug functionality
  - e200z2 core:NDI per IEEE-ISTO 5001-2008 Class3+
  - e200z4 core: NDI per IEEE-ISTO 5001-2008 Class 3+

- Timer
  - 16 Periodic Interrupt Timers (PITs)
  - Two System Timer Modules (STM)
  - Three Software Watchdog Timers (SWT)
  - 64 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels

- Device/board boundary Scan testing supported with Joint Test Action Group (JTAG) of IEEE 1149.1 and IEEE 1149.7 (CJTAG)

- Security
  - Hardware Security Module (HSMv2)
  - Password and Device Security (PASS) supporting advanced censorship and life-cycle management
  - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts

- Functional Safety
  - ISO26262 ASIL-B compliance

- Multiple operating modes
  - Includes enhanced low power operation

# Table of Contents

# 1 Block diagram

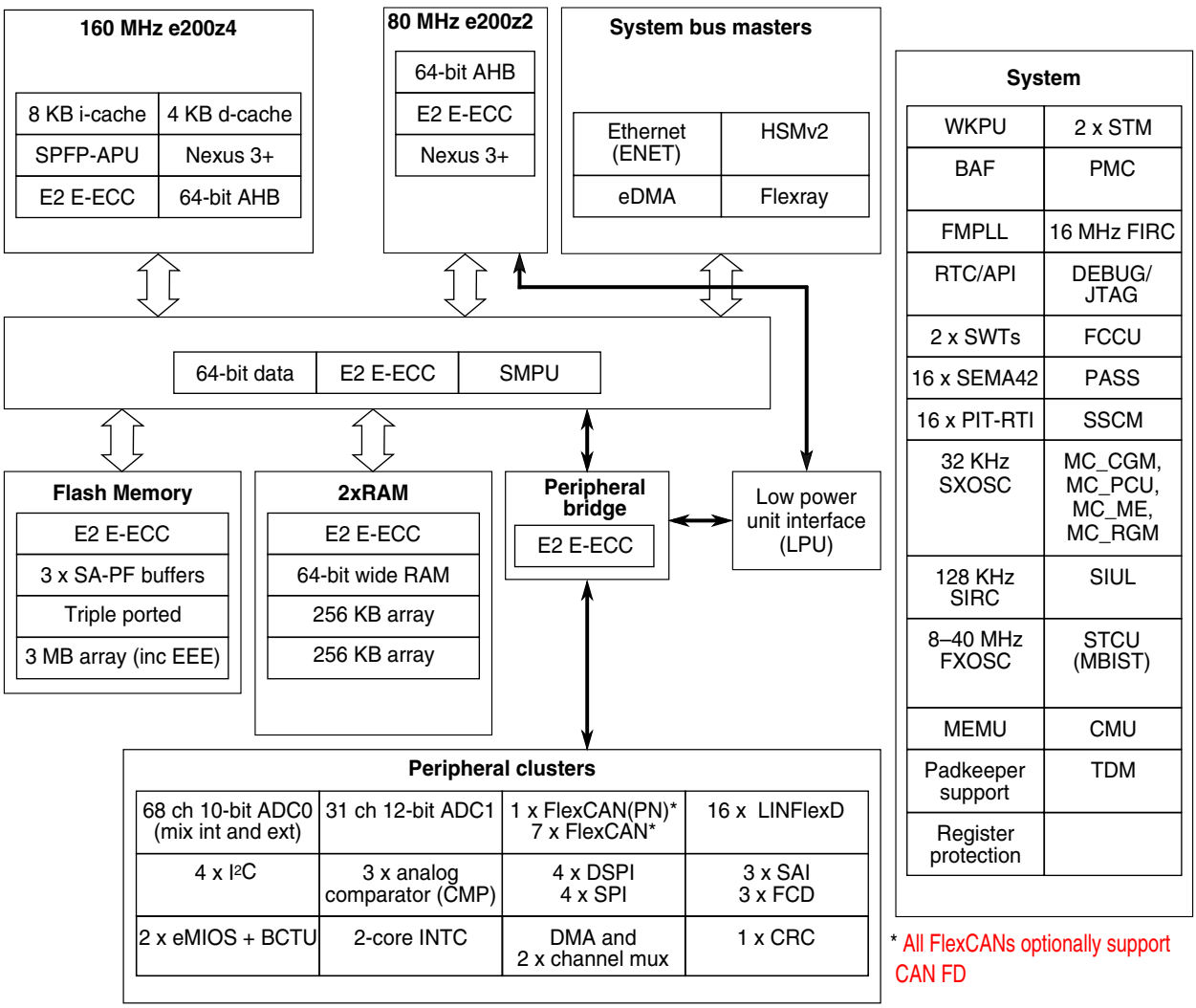


**Figure 1. MPC5746C block diagram**

# 2 Family comparison

The following table provides a summary of the different members of the MPC5746C family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

## Table 1. MPC5746C Family Comparison[1] (continued)

| Feature | MPC5745B | MPC5744B | MPC5746B | MPC5744C | MPC5745C | MPC5746C |
|---|---|---|---|---|---|---|
| $I^2C$ | 4 | 4 | 4 | 4 | | |
| SAI/$I^2S$ | 3 | 3 | 3 | 3 | | |
| FXOSC | 8 - 40 MHz | | | | | |
| SXOSC | 32 KHz | | | | | |
| FIRC | 16 MHz | | | | | |
| SIRC | 128 KHz | | | | | |
| FMPLL | 1 | | | | | |
| Low Power Unit (LPU) | Yes | | | | | |
| FlexRay 2.1 (dual channel) | Yes, 128 MB | Yes, 128 MB | Yes, 128 MB | Yes, 128 MB | | |
| Ethernet (RMII, MII + 1588, Muti queue AVB support) | 1 | 1 | 1 | 1 | | |
| CRC | 1 | | | | | |
| MEMU | 2 | | | | | |
| STCU2 | 1 | | | | | |
| HSM-v2 (security) | Optional | | | | | |
| Censorship | Yes | | | | | |
| FCCU | 1 | | | | | |
| Safety level | Specific functions ASIL-B certifiable | | | | | |
| User MBIST | Yes | | | | | |
| I/O Retention in Standby | Yes | | | | | |
| GPIO[6] | Up to 264 GPI and up to 246 GPIO | | | | | |
| Debug | JTAGC,<br>cJTAG | | | | | |
| Nexus | Z4 N3+ (Only available on 324BGA (development only) )<br>Z2 N3+ (Only available on 324BGA (development only) ) | | | | | |
| Packages | 176 LQFP-EP<br>256 BGA<br>100 BGA | 176 LQFP-EP<br>256 BGA<br>100 BGA | 176 LQFP-EP<br>256 BGA<br>100 BGA | 176 LQFP-EP<br>256 BGA<br>100 BGA | 176 LQFP-EP<br>256 BGA<br>100 BGA | 176 LQFP-EP<br>256 BGA,<br>324 BGA (development only)<br>100 BGA |

1. Feature set dependent on selected peripheral multiplexing, table shows example. Peripheral availability is package dependent.
2. Based on 125°C ambient operating temperature and subject to full device characterization.
3. Contact NXP representative for part number
4. Additional SWT included when HSM option selected
5. See device datasheet and reference manual for information on to timer channel configuration and functions.
6. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

## Table 2. MPC5746C Family Comparison - NVM Memory Map 1

| Start Address | End Address | Flash block | RWW partition | MPC5744 | MPC5745 | MPC5746 |
|---|---|---|---|---|---|---|
| 0x01000000 | 0x0103FFFF | 256 KB code Flash block 0 | 6 | available | available | available |
| 0x01040000 | 0x0107FFFF | 256 KB code Flash block 1 | 6 | available | available | available |
| 0x01080000 | 0x010BFFFF | 256 KB code Flash block 2 | 6 | available | available | available |
| 0x010C0000 | 0x010FFFFF | 256 KB code Flash block3 | 6 | available | available | available |
| 0x01100000 | 0x0113FFFF | 256 KB code Flash block 4 | 6 | not available | available | available |
| 0x01140000 | 0x0117FFFF | 256 KB code Flash block 5 | 7 | not available | available | available |
| 0x01180000 | 0x011BFFFF | 256 KB code Flash block 6 | 7 | not available | not available | available |
| 0x011C0000 | 0x011FFFFF | 256 KB code Flash block 7 | 7 | not available | not available | available |
| 0x01200000 | 0x0123FFFF | 256 KB code Flash block 8 | 7 | not available | not available | available |
| 0x01240000 | 0x0127FFFF | 256 KB code Flash block 9 | 7 | not available | not available | not available |

## Table 3. MPC5746C Family Comparison - NVM Memory Map 2

| Start Address | End Address | Flash block | RWW partition | MPC5744B<br>MPC5745B<br>MPC5746B | MPC5744C<br>MPC5745C<br>MPC5746C |
|---|---|---|---|---|---|
| 0x00F90000 | 0x00F93FFF | 16 KB data Flash | 2 | available | available |
| 0x00F94000 | 0x00F97FFF | 16 KB data Flash | 2 | available | available |
| 0x00F98000 | 0x00F9BFFF | 16 KB data Flash | 2 | available | available |
| 0x00F9C000 | 0x00F9FFFF | 16 KB data Flash | 2 | available | available |
| 0x00FA0000 | 0x00FA3FFF | 16 KB data Flash | 3 | not available | available |
| 0x00FA4000 | 0x00FA7FFF | 16 KB data Flash | 3 | not available | available |
| 0x00FA8000 | 0x00FABFFF | 16 KB data Flash | 3 | not available | available |
| 0x00FAC000 | 0x00FAFFFF | 16 KB data Flash | 3 | not available | available |

## Table 4. MPC5746C Family Comparison - RAM Memory Map

| Start Address | End Address | Allocated size | Description | MPC5744 | MPC5745 | MPC5746 |
|---|---|---|---|---|---|---|
| 0x40000000 | 0x40001FFF | 8 KB | SRAM0 | available | available | available |
| 0x40002000 | 0x4000FFFF | 56 KB | SRAM1 | available | available | available |
| 0x40010000 | 0x4001FFFF | 64 KB | SRAM2 | available | available | available |
| 0x40020000 | 0x4002FFFF | 64 KB | SRAM3 | available | available | available |

*Table continues on the next page...*

## 4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

**NOTE**

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

**Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)**

| Symbol | Parameter | Conditions[1] | Min[2] | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD\_HV\_A}$<br>$V_{DD\_HV\_B}$<br>$V_{DD\_HV\_C}$ | HV IO supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_FLA}$[3] | HV flash supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_ADC1\_REF}$ | HV ADC1 high reference voltage | — | 3.0 | 5.5 | V |
| $V_{DD\_HV\_ADC0}$<br>$V_{DD\_HV\_ADC1}$ | HV ADC supply voltage | — | max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05 | 3.6 | V |
| $V_{SS\_HV\_ADC0}$<br>$V_{SS\_HV\_ADC1}$ | HV ADC supply ground | — | -0.1 | 0.1 | V |
| $V_{DD\_LV}$[4, 5] | Core supply voltage | — | 1.2 | 1.32 | V |
| $V_{IN1\_CMP\_REF}$[6, 7] | Analog Comparator DAC reference voltage | — | 3.15 | 3.6 | V |
| $I_{INJPAD}$ | Injected input current on any pin during overload condition | — | -3.0 | 3.0 | mA |

*Table continues on the next page...*

## Table 8. Voltage regulator electrical specifications (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{flash\_reg}$[4] | External decoupling / stability capacitor for internal Flash regulators | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1.32 | 2.2 | 3 | µF |
| | Combined ESR of external capacitor | — | 0.001 | — | 0.03 | Ohm |
| $C_{HV\_VDD\_A}$ | VDD_HV_A supply capacitor [5, 5] | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | µF |
| $C_{HV\_VDD\_B}$ | VDD_HV_B supply capacitor[5] | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | µF |
| $C_{HV\_VDD\_C}$ | VDD_HV_C supply capacitor[5] | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | µF |
| $C_{HV\_ADC0}$ $C_{HV\_ADC1}$ | HV ADC supply decoupling capacitances | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | µF |
| $C_{HV\_ADR}$[6] | HV ADC SAR reference supply decoupling capacitances | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 0.47 | — | — | µF |
| $V_{DD\_HV\_BALLAST}$[7] | FPREG Ballast collector supply voltage | When collector of NPN ballast is directly supplied by an on board supply source (not shared with VDD_HV_A supply pin) without any series resistance, that is, $R_{C\_BALLAST}$ less than 0.01 Ohm. | 2.25 | — | 5.5 | V |
| $R_{C\_BALLAST}$ | Series resistor on collector of FPREG ballast | When VDD_HV_BALLAST is shorted to VDD_HV_A on the board | — | — | 0.1 | Ohm |
| $t_{SU}$ | Start-up time with external ballastafter main supply (VDD_HV_A) stabilization | Cfp_reg = 3 µF | — | 74 | — | µs |
| $t_{SU\_int}$ | Start-up time with internal ballast after main supply (VDD_HV_A) stabilization | Cfp_reg = 3 µF | — | 103 | — | µs |
| $t_{ramp}$ | Load current transient | Iload from 15% to 55% $C_{fp\_reg}$ = 3 µF | | 1.0 | | µs |

1. Split capacitance on each pair VDD_LV pin should sum up to a total value of $C_{fp\_reg}$
2. Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.
3. Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
4. It is required to minimize the board parasitic inductance from decoupling capacitor to VDD_HV_FLA pin and the routing inductance should be less than 1nH.

## Table 10. Current consumption characteristics (continued)

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_HV\_ADC\_REF}$[10, 11, 11] | ADC REF Operating current | $T_a$ = 125 °C[5]<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 5.5 V | — | 200 | 400 | µA |
| | | $T_a$ = 105 °C<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 5.5 V | — | 200 | — | |
| | | $T_a$ = 85 °C<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 5.5 V | — | 200 | — | |
| | | $T_a$ = 25 °C<br>2 ADCs operating at 80 MHz<br>$V_{DD\_HV\_ADC\_REF}$ = 3.6 V | — | 200 | — | |
| $I_{DD\_HV\_ADCx}$[11] | ADC HV Operating current | $T_a$ = 125 °C[5]<br>ADC operating at 80 MHz<br>$V_{DD\_HV\_ADC}$ = 5.5 V | — | 1.2 | 2 | mA |
| | | $T_a$ = 25 °C<br>ADC operating at 80 MHz<br>$V_{DD\_HV\_ADC}$ = 3.6 V | — | 1 | 2 | |
| $I_{DD\_HV\_FLASH}$[12] | Flash Operating current during read access | $T_a$ = 125 °C[5]<br>3.3 V supplies<br>160 MHz frequency | — | 40 | 45 | mA |
| | | $T_a$ = 105 °C<br>3.3 V supplies<br>160 MHz frequency | — | 40 | 45 | |
| | | $T_a$ = 85 °C<br>3.3 V supplies<br>160 MHz frequency | — | 40 | 45 | |

1. The content of the Conditions column identifies the components that draw the specific current.
2. Single e200Z4 core cache disabled @80 MHz, no FlexRay, no ENET, 2 x CAN, 8 LINFlexD, 2 SPI, ADC0 and 1 used constantly, no HSM, Memory: 2M flash, 128K RAM RUN mode, Clocks: FIRC on, XOSC, PLL on, SIRC on for TOD, no 32KHz crystal (TOD runs off SIRC).
3. Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C. In case of internal ballast mode, it is expected that the external ballast is not mounted and BAL_SELECT_INT pin is tied to VDD_HV_A supply on board. Internal ballast can be used for all use cases with current consumption upto 150mA
4. The power consumption does not consider the dynamic current of I/Os
5. Tj=150°C. Assumes Ta=125°C
   - Assumes maximum θJA of 2s2p board. SeeThermal attributes
6. e200Z4 core, 160MHz, cache enabled; e200Z2 core , 80MHz, no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 256K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
7. e200Z4 core, 120MHz, cache enabled; e200Z2 core, 60MHz; no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 128K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal

## 5.3 AC specifications @ 5 V Range

**Table 16. Functional Pad AC Specifications @ 5 V Range**

| Symbol | Prop. Delay (ns)[1] L>H/H>L | | Rise/Fall Edge (ns) | | Drive Load (pF) | SIUL2_MSCRn[SRC 1:0] |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | MSB,LSB |
| pad_sr_hv (output) | | 4.5/4.5 | | 1.3/1.2 | 25 | 11 |
| | | 6/6 | | 2.5/2 | 50 | |
| | | 13/13 | | 9/9 | 200 | |
| | | 5.25/5.25 | | 3/2 | 25 | 10 |
| | | 9/8 | | 5/4 | 50 | |
| | | 22/22 | | 18/16 | 200 | |
| | | 27/27 | | 13/13 | 50 | 01[2, 2] |
| | | 40/40 | | 24/24 | 200 | |
| | | 40/40 | | 24/24 | 50 | 00[2] |
| | | 65/65 | | 40/40 | 200 | |
| pad_i_hv/ pad_sr_hv (input) | | 1.5/1.5 | | 0.5/0.5 | 0.5 | NA |

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

**NOTE**

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

**NOTE**

The above specification is measured between 20% / 80%.

## 5.4 DC electrical specifications @ 5 V Range

**Table 17. DC electrical specifications @ 5 V Range**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Vih (pad_i_hv) | pad_i_hv Input Buffer High Voltage | 0.7*VDD_HV_x | VDD_HV_x + 0.3 | V |

*Table continues on the next page...*

**Table 18. Functional reset pad electrical specifications (continued)**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{HYS}$ | CMOS Input Buffer hysterisis | — | 300 | — | — | mV |
| $V_{DD\_POR}$ | Minimum supply for strong pull-down activation | — | — | — | 1.2 | V |
| $I_{OL\_R}$ | Strong pull-down current [1, 1] | Device under power-on reset<br>$V_{DD\_HV\_A}$= $V_{DD\_POR}$<br>$V_{OL}$ = 0.35*$V_{DD\_HV\_A}$ | 0.2 | — | — | mA |
| | | Device under power-on reset<br>$V_{DD\_HV\_A}$= $V_{DD\_POR}$<br>$V_{OL}$ = 0.35*$V_{DD\_HV\_IO}$ | 11 | — | — | mA |
| $W_{FRST}$ | $\overline{\text{RESET}}$ input filtered pulse | — | — | — | 500 | ns |
| $W_{NFRST}$ | $\overline{\text{RESET}}$ input not filtered pulse | — | 2000 | — | — | ns |
| $\|I_{WPU}\|$ | Weak pull-up current absolute value | RESET pin $V_{IN}$ = $V_{DD}$ | 23 | — | 82 | µA |

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

## 5.6 PORST electrical specifications

**Table 19. PORST electrical specifications**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $W_{FPORST}$ | $\overline{\text{PORST}}$ input filtered pulse | — | — | 200 | ns |
| $W_{NFPORST}$ | $\overline{\text{PORST}}$ input not filtered pulse | 1000 | — | — | ns |
| $V_{IH}$ | Input high level | 0.65 x $V_{DD\_HV\_A}$ | — | — | V |
| $V_{IL}$ | Input low level | — | — | 0.35 x $V_{DD\_HV\_A}$ | V |

# 6 Peripheral operating requirements and behaviours

## 6.1 Analog

### 6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

## Table 30. Flash memory program and erase specifications

| Symbol | Characteristic[1] | Typ[2] | Factory Programming[3, 4] | | Field Update | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Initial Max | Initial Max, Full Temp | Typical End of Life[5] | Lifetime Max[6] | | |
| | | | 20°C ≤$T_A$ ≤30°C | -40°C ≤$T_J$ ≤150°C | -40°C ≤$T_J$ ≤150°C | ≤ 1,000 cycles | ≤ 250,000 cycles | |
| $t_{dwpgm}$ | Doubleword (64 bits) program time | 43 | 100 | 150 | 55 | 500 | | µs |
| $t_{ppgm}$ | Page (256 bits) program time | 73 | 200 | 300 | 108 | 500 | | µs |
| $t_{qppgm}$ | Quad-page (1024 bits) program time | 268 | 800 | 1,200 | 396 | 2,000 | | µs |
| $t_{16kers}$ | 16 KB Block erase time | 168 | 290 | 320 | 250 | 1,000 | | ms |
| $t_{16kpgm}$ | 16 KB Block program time | 34 | 45 | 50 | 40 | 1,000 | | ms |
| $t_{32kers}$ | 32 KB Block erase time | 217 | 360 | 390 | 310 | 1,200 | | ms |
| $t_{32kpgm}$ | 32 KB Block program time | 69 | 100 | 110 | 90 | 1,200 | | ms |
| $t_{64kers}$ | 64 KB Block erase time | 315 | 490 | 590 | 420 | 1,600 | | ms |
| $t_{64kpgm}$ | 64 KB Block program time | 138 | 180 | 210 | 170 | 1,600 | | ms |
| $t_{256kers}$ | 256 KB Block erase time | 884 | 1,520 | 2,030 | 1,080 | 4,000 | — | ms |
| $t_{256kpgm}$ | 256 KB Block program time | 552 | 720 | 880 | 650 | 4,000 | — | ms |

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ $T_J$ ≤ 150°C, full spec voltage.

## 6.3.2 Flash memory Array Integrity and Margin Read specifications

### Table 31. Flash memory Array Integrity and Margin Read specifications

| Symbol | Characteristic | Min | Typical | Max[1, 1] | Units[2, 2] |
|---|---|---|---|---|---|
| $t_{ai16kseq}$ | Array Integrity time for sequential sequence on 16 KB block. | — | — | 512 x Tperiod x Nread | — |
| $t_{ai32kseq}$ | Array Integrity time for sequential sequence on 32 KB block. | — | — | 1024 x Tperiod x Nread | — |
| $t_{ai64kseq}$ | Array Integrity time for sequential sequence on 64 KB block. | — | — | 2048 x Tperiod x Nread | — |

*Table continues on the next page...*

**Table 33. Flash memory AC timing specifications (continued)**

| Symbol | Characteristic | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| $t_{drcv}$ | Time to recover once exiting low power mode. | 16<br>plus seven system clock periods. | — | 45<br>plus seven system clock periods | µs |
| $t_{aistart}$ | Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP | — | — | 5 | ns |
| $t_{aistop}$ | Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request. | — | — | 80<br>plus fifteen system clock periods | ns |
| $t_{mrstop}$ | Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request. | 10.36<br>plus four system clock periods | — | 20.42<br>plus four system clock periods | µs |

## 6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

**Table 34. Flash Read Wait State and Address Pipeline Control Combinations**

| Flash frequency | RWSC setting | APC setting |
|---|---|---|
| 0 MHz < fFlash <= 33 MHz | 0 | 0 |
| 33 MHz < fFlash <= 100 MHz | 2 | 1 |
| 100 MHz < fFlash <= 133 MHz | 3 | 1 |
| 133 MHz < fFlash <= 160 MHz | 4 | 1 |

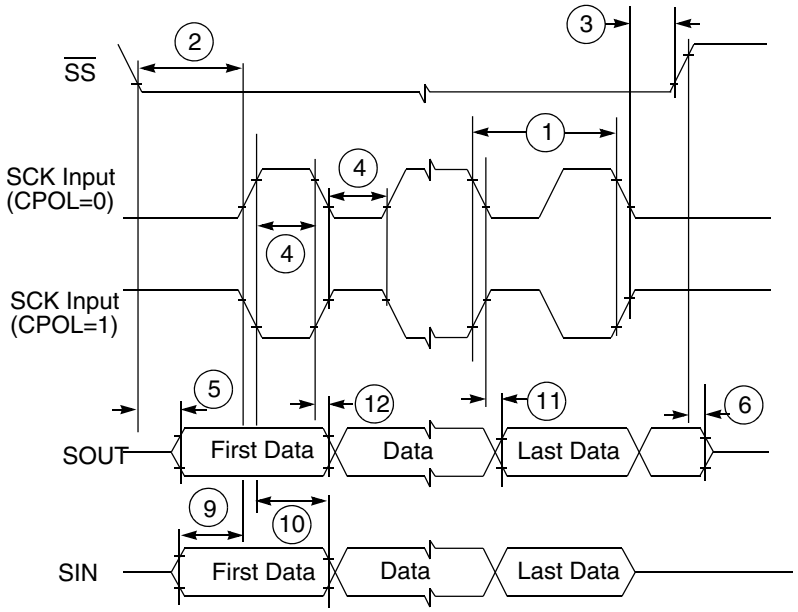


**Figure 10. DSPI classic SPI timing — slave, CPHA = 0**

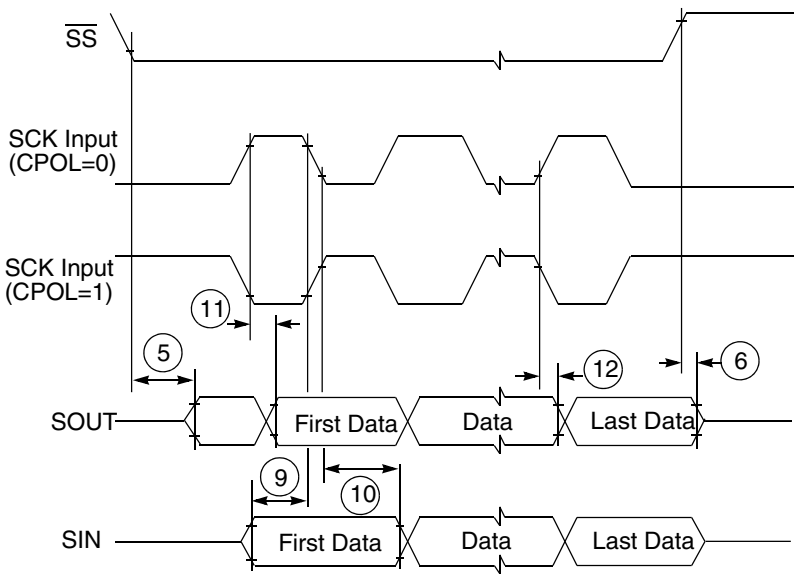


**Figure 11. DSPI classic SPI timing — slave, CPHA = 1**

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = –40 oC / 150 oC.

## 6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

### 6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

**Table 41. MII signal switching specifications**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| — | RXCLK frequency | — | 25 | MHz |
| MII1 | RXCLK pulse width high | 35% | 65% | RXCLK period |
| MII2 | RXCLK pulse width low | 35% | 65% | RXCLK period |
| MII3 | RXD[3:0], RXDV, RXER to RXCLK setup | 5 | — | ns |
| MII4 | RXCLK to RXD[3:0], RXDV, RXER hold | 5 | — | ns |
| — | TXCLK frequency | — | 25 | MHz |
| MII5 | TXCLK pulse width high | 35% | 65% | TXCLK period |
| MII6 | TXCLK pulse width low | 35% | 65% | TXCLK period |
| MII7 | TXCLK to TXD[3:0], TXEN, TXER invalid | 2 | — | ns |
| MII8 | TXCLK to TXD[3:0], TXEN, TXER valid | — | 25 | ns |

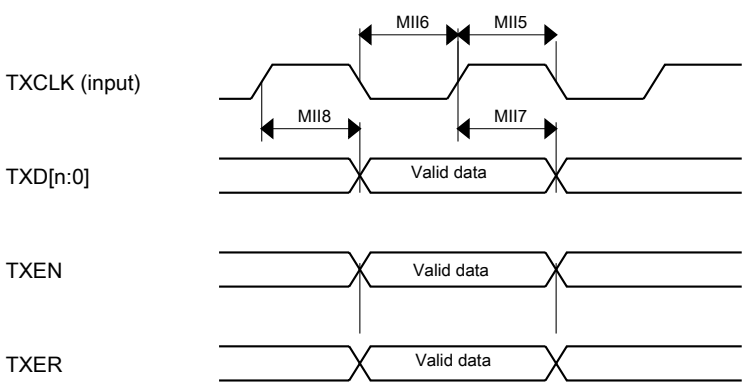


**Figure 21. RMII/MII transmit signal timing diagram**

**Thermal attributes**

| Board type | Symbol | Description | 176LQFP | Unit | Notes |
|---|---|---|---|---|---|
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 17.8 | °C/W | 1, 3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 10.9 | °C/W | 44 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 8.4 | °C/W | 55 |
| — | $\Psi_{JT}$ | Thermal resistance, junction to package top | 0.5 | °C/W | 66 |
| — | $\Psi_{JB}$ | Thermal characterization parameter, junction to package bottom | 0.3 | °C/W | 77 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

| Board type | Symbol | Description | 324 MAPBGA | Unit | Notes |
|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 31.0 | °C/W | 11, 22 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 24.3 | °C/W | 1,2,33 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 23.5 | °C/W | 1, 3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 20.1 | °C/W | 1,3 |

*Table continues on the next page...*

| Board type | Symbol | Description | 100 MAPBGA | Unit | Notes |
|---|---|---|---|---|---|
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 10.8 | °C/W | 44 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 8.2 | °C/W | 55 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 0.2 | °C/W | 66 |
| — | $\Psi_{JB}$ | Thermal characterization parameter, junction to package bottom outside center (natural convection) | 7.8 | °C/W | 77 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

# 8 Dimensions

## 8.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

| Package | NXP Document Number |
|---|---|
| 100 MAPBGA | 98ASA00802D |

*Table continues on the next page...*

### 10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

**Table 50. BAF execution duration**

| BAF execution duration | Min | Typ | Max | Unit |
|---|---|---|---|---|
| BAF execution time (boot header at first location) | — | 200 | — | µs |
| BAF execution time (boot header at last location) | — | — | 320 | µs |

### 10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

**NOTE**

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

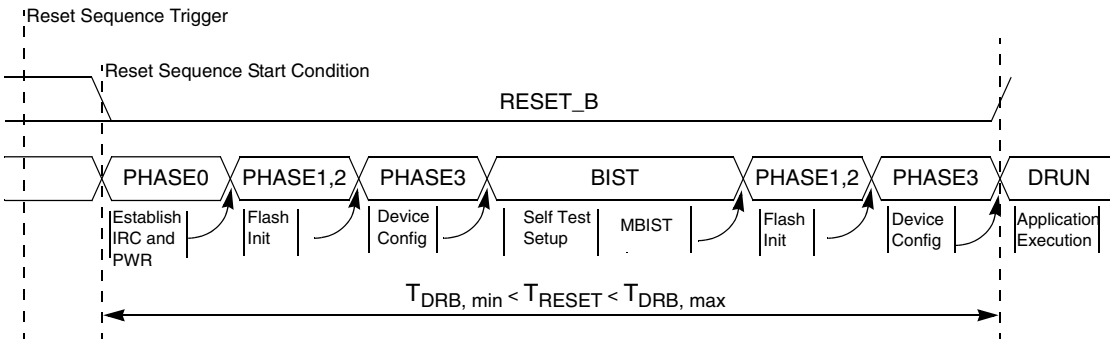


**Figure 32. Destructive reset sequence, BIST enabled**

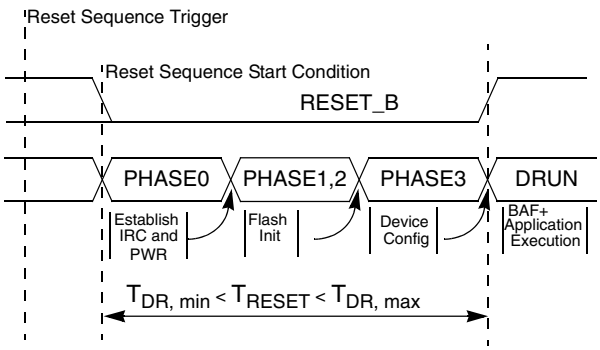


**Figure 33. Destructive reset sequence, BIST disabled**

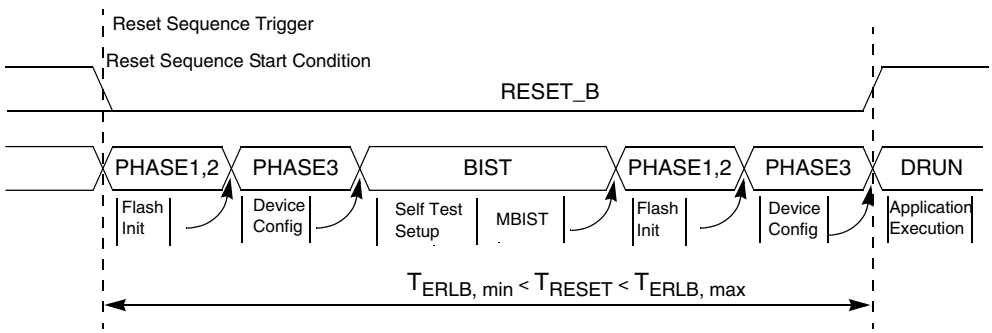


**Figure 34. External reset sequence long, BIST enabled**

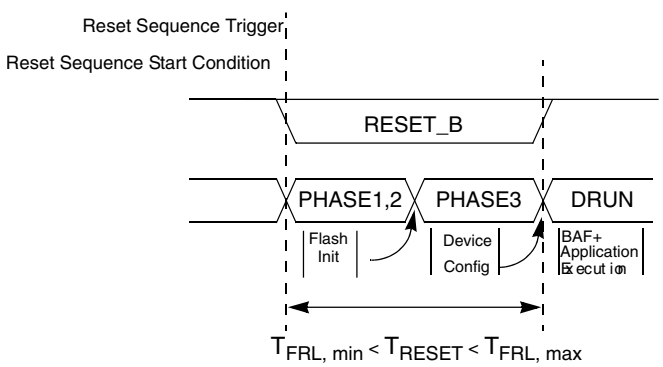


**Figure 35. Functional reset sequence long**

## Table 51. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • In section, Thermal attributes<br>  • Added table for 100 MAPBGA<br><br>• In section Obtaining package dimensions<br>  • Updated package details for 100 MAPBGA |
| | | • Editoral updates throughtout including correction of various module names. |

*Table continues on the next page...*

## Table 51. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| Rev 3 | 2 March 2016 | • In section, Recommended operating conditions<br>  • Added a new Note<br><br>• In section, Voltage regulator electrical characteristics<br>  • In table, Voltage regulator electrical specifications:<br>  • Added a new row for $C_{HV\_VDD\_B}$<br>  • Added a footnote on $V_{DD\_HV\_BALLAST}$<br>  • Added a new Note at the end of this section<br><br>• In section, Voltage monitor electrical characteristics<br>  • In table, Voltage monitor electrical characteristics:<br>  • Removed "$V_{LVD\_FLASH}$" and "$V_{LVD\_FLASH}$ during low power mode using LPBG as reference" rows<br>  • Updated Fall and Rise trimmed Minimum values for $V_{HVD\_LV\_cold}$<br><br>• In section, Supply current characteristics<br>  • In table, Current consumption characteristics:<br>  • Updated the footnote mentioned in the Condition column of $I_{DD\_STOP}$ row<br>  • Updated all TBD values<br>  • In table, Low Power Unit (LPU) Current consumption characteristics:<br>  • Updated the typical value of LPU_STOP to 0.18 mA<br>  • Updated all TBD values<br>  • In table, STANDBY Current consumption characteristics:<br>  • Updated all TBD values<br><br>• In section, AC specifications @ 3.3 V Range<br>  • In table, Functional Pad AC Specifications @ 3.3 V Range:<br>  • Updated Rise/Fall Edge values<br><br>• In section, DC electrical specifications @ 3.3V Range<br>  • In table, DC electrical specifications @ 3.3V Range:<br>  • Updated Max value for Vol to 0.1 * VDD_HV_x<br><br>• In section, AC specifications @ 5 V Range<br>  • In table, Functional Pad AC Specifications @ 5 V Range:<br>  • Updated Rise/Fall Edge values<br><br>• In section, DC electrical specifications @ 5 V Range<br>  • In table, DC electrical specifications @ 5 V Range:<br>  • Updated Min and Max values for Pull_Ioh and Pull_Iol rows<br>  • Updated Max value for Vol to 0.1 * VDD_HV_x<br><br>• In section, Reset pad electrical characteristics<br>  • In table, Functional reset pad electrical specifications:<br>  • Updated parameter column for $V_{IH}$, $V_{IL}$ and $V_{HYS}$ rows<br>  • Updated Min and Max values for $V_{IH}$ and $V_{IL}$ rows<br><br>• In section, PORST electrical specifications<br>  • In table, PORST electrical specifications:<br>  • Updated Unit and Min/Max values for $V_{IH}$ and $V_{IL}$ rows<br><br>• In section, Input equivalent circuit and ADC conversion characteristics<br>  • In table, ADC conversion characteristics (for 12-bit):<br>  • Updated "ADC Analog Pad (pad going to one ADC)" row<br>  • In table, ADC conversion characteristics (for 10-bit):<br>  • Updated "ADC Analog Pad (pad going to one ADC)" row<br><br>• In section, Analog Comparator (CMP) electrical specifications<br>  • In table, Comparator and 6-bit DAC electrical specifications:<br>  • Updated Min and Max values for $V_{AIO}$ to +47 mV<br>  • Updated Max value for $t_{DLS}$ to 21 µs<br><br>• In section, Main oscillator electrical characteristics<br>  • In table, Main oscillator electrical characteristics: |