



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	178
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746csk1mmj6r

3.2 Ordering Information

Example Code	P	PC	57	4	6	C	S	K0	M	MJ	6	R
Qualification Status												
Power Architecture												
Automotive Platform												
Core Version												
Flash Size (core dependent)												
Product												
Optional fields												
Fab and mask indicator												
Temperature spec.												
Package Code												
CPU Frequency												
R = Tape & Reel (blank if Tray)												

Qualification Status P = Engineering samples S = Automotive qualified PC = Power Architecture	Product Version B = Single core C = Dual core	Fab and mask version indicator K = TSMC Fab #(0,1,etc.) = Version of the maskset, like rev. 0=0N65H	Package Code KU = 176 LQFP EP MJ = 256 MAPBGA MN = 324 MAPBGA MH = 100MAPBGA
Automotive Platform 57 = Power Architecture in 55nm	Optional fields Blank = No optional feature S = HSM (Security Module) F = CAN FD B = HSM + CAN FD R = 512K RAM T = HSM + 512K RAM G* = CAN FD + 512K RAM H* = HSM + CAN FD + 512K RAM * G and H for 5746 B/C only	Temperature spec. C = -40.C to +85.C Ta V = -40.C to +105.C Ta M = -40.C to +125.C Ta	CPU Frequency 2 = Z4 operates upto 120 MHz 6 = Z4 operates upto 160 MHz
Core Version 4 = e200z4 Core Version (highest core version in the case of multiple cores)			Shipping Method R = Tape and reel Blank = Tray
Flash Memory Size 4 = 1.5 MB 5 = 2 MB 6 = 3 MB			

Note: Not all part number combinations are available as production product

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in [Table 5](#) for specific conditions

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

NOTE

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FL A should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FL A should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

Table 6. Recommended operating conditions (V_{DD_HV_x} = 3.3 V)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
V _{DD_HV_A} V _{DD_HV_B} V _{DD_HV_C}	HV IO supply voltage	—	3.15	3.6	V
V _{DD_HV_FL A} ³	HV flash supply voltage	—	3.15	3.6	V
V _{DD_HV_ADC1_REF}	HV ADC1 high reference voltage	—	3.0	5.5	V
V _{DD_HV_ADC0} V _{DD_HV_ADC1}	HV ADC supply voltage	—	max(V _{DD_HV_A} , V _{DD_HV_B} , V _{DD_HV_C}) - 0.05	3.6	V
V _{SS_HV_ADC0} V _{SS_HV_ADC1}	HV ADC supply ground	—	-0.1	0.1	V
V _{DD_LV} ^{4, 5}	Core supply voltage	—	1.2	1.32	V
V _{IN1_CMP_REF} ^{6, 7}	Analog Comparator DAC reference voltage	—	3.15	3.6	V
I _{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA

Table continues on the next page...

Table 9. Voltage monitor electrical characteristics (continued)

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up ¹	Mask Opt ^{2, 2}	Reset Type	Min	Typ	Max	V
V _{LVD_LV_PD2_cold}	LV supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.1400	1.1550	1.1750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.1600	1.1750	1.1950	V

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.
3. There is no voltage monitoring on the V_{DD_HV_ADC0}, V_{DD_HV_ADC1}, V_{DD_HV_B} and V_{DD_HV_C} I/O segments. For applications requiring monitoring of these segments, either connect these to V_{DD_HV_A} at the PCB level or monitor externally.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 10. Current consumption characteristics

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
I _{DD_BODY_12, 3}	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies ^{4, 4} T _a = 125°C ^{5, 5} V _{DD_LV} = 1.25 V V _{DD_HV_A} = 5.5V SYS_CLK = 80MHz	—	—	147	mA
		T _a = 105°C	—	—	142	mA
		T _a = 85 °C	—	—	137	mA

Table continues on the next page...

Table 12. STANDBY Current consumption characteristics (continued)

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
STANDBY2	STANDBY with 128K RAM	T _a = 25 °C	—	75	—	μA
		T _a = 85 °C	—	155	730	
		T _a = 105 °C	—	255	1350	
		T _a = 125 °C ²	—	396	2600	
STANDBY3	STANDBY with 256K RAM	T _a = 25 °C	—	80	—	μA
		T _a = 85 °C	—	180	800	
		T _a = 105 °C	—	290	1425	
		T _a = 125 °C ²	—	465	2900	
STANDBY3	FIRC ON	T _a = 25 °C	—	500	—	μA

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming T_a=T_j, as the device is in static (fully clock gated) mode. Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#)

4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 13. ESD ratings

Symbol	Parameter	Conditions ¹	Class	Max value ²	Unit
V _{ESD(HBM)}	Electrostatic discharge (Human Body Model)	T _A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
V _{ESD(CDM)}	Electrostatic discharge (Charged Device Model)	T _A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

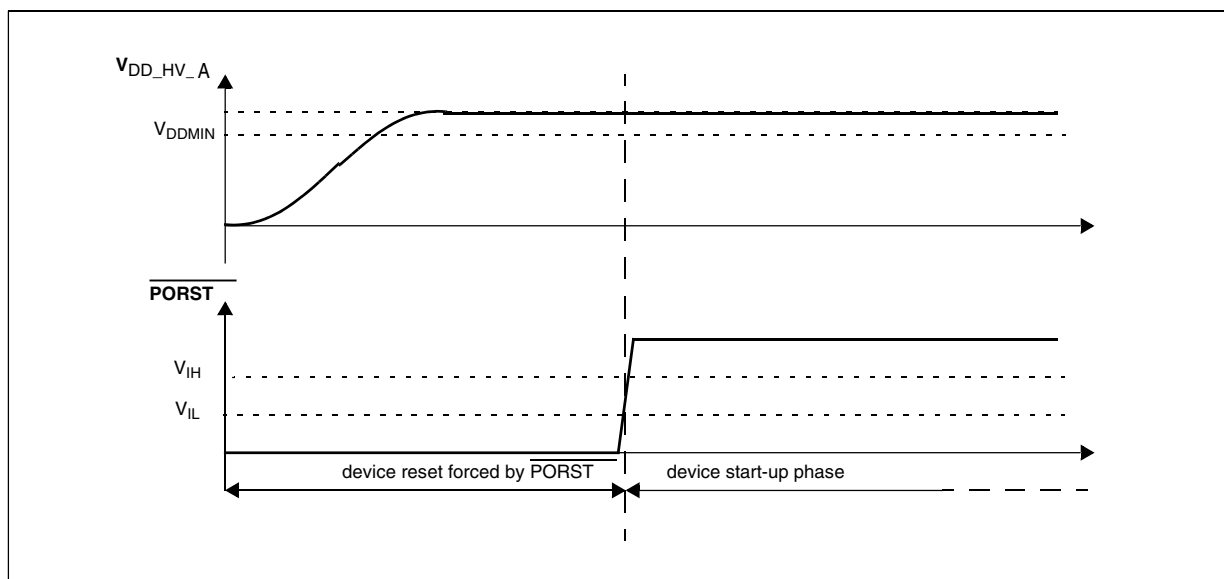


Figure 3. Start-up reset requirements

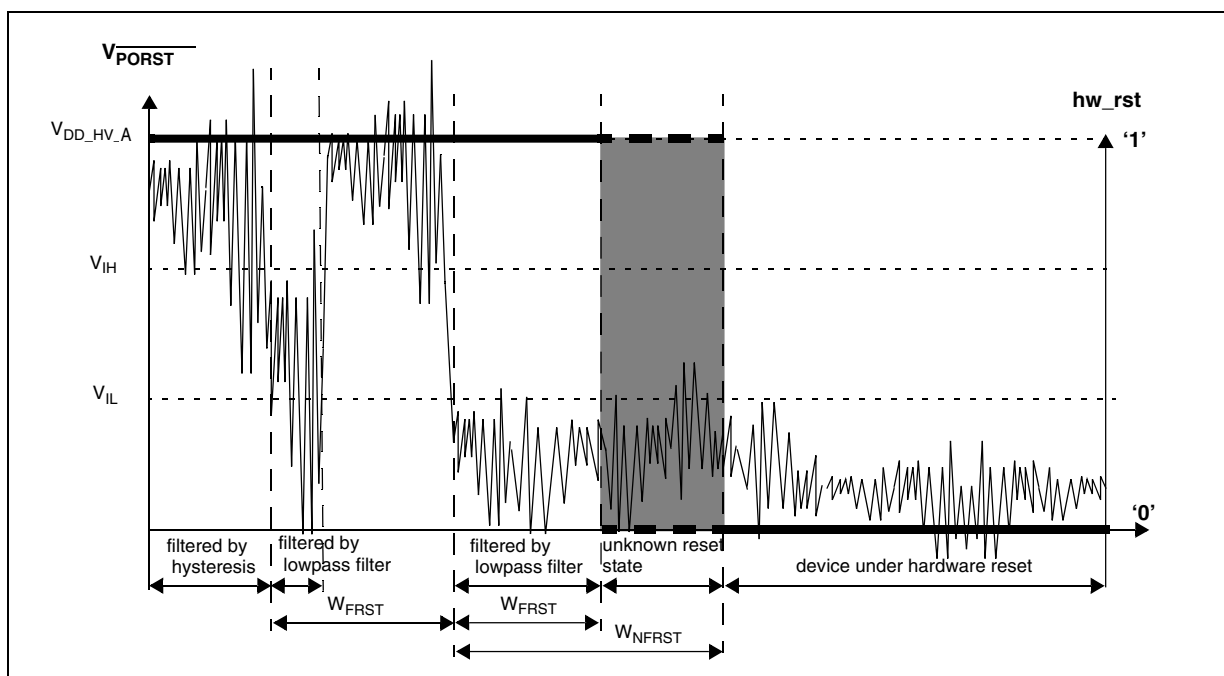


Figure 4. Noise filtering on reset signal

Table 18. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	CMOS Input Buffer High Voltage	—	$0.65 \cdot V_{D_HV_x}$	—	$V_{DD_HV_x} + 0.3$	V
V_{IL}	CMOS Input Buffer Low Voltage	—	$V_{DD_HV_x} - 0.3$	—	$0.35 \cdot V_{DD_HV_x}$	V

Table continues on the next page...

Table 18. Functional reset pad electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{HYS}	CMOS Input Buffer hysteresis	—	300	—	—	mV
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current ^{1, 1}	Device under power-on reset $V_{DD_HV_A} = V_{DD_POR}$ $V_{OL} = 0.35 \times V_{DD_HV_A}$	0.2	—	—	mA
		Device under power-on reset $V_{DD_HV_A} = V_{DD_POR}$ $V_{OL} = 0.35 \times V_{DD_HV_IO}$	11	—	—	mA
W_{FRST}	RESET input filtered pulse	—	—	—	500	ns
W_{NFRST}	RESET input not filtered pulse	—	2000	—	—	ns
I_{WPUL}	Weak pull-up current absolute value	RESET pin $V_{IN} = V_{DD}$	23	—	82	μA

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	PORST input filtered pulse	—	—	200	ns
$W_{NFPORST}$	PORST input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	0.65 x $V_{DD_HV_A}$	—	—	V
V_{IL}	Input low level	—	—	0.35 x $V_{DD_HV_A}$	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

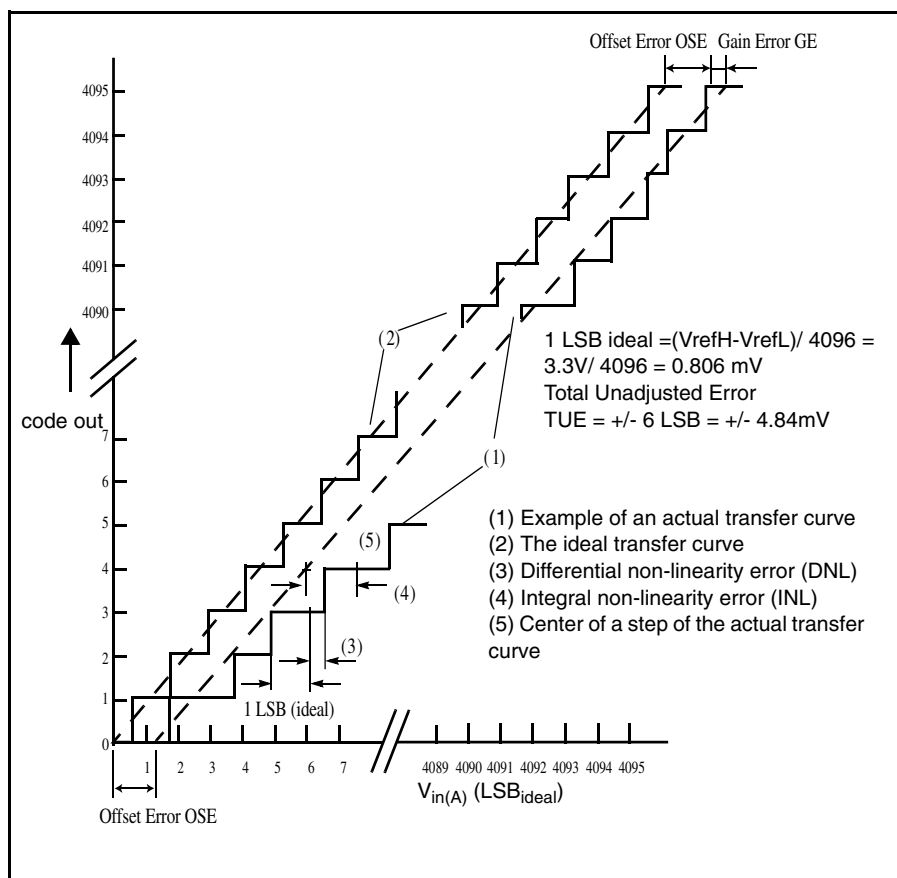


Figure 5. ADC characteristics and error definitions

6.1.1.1 Input equivalent circuit and ADC conversion characteristics

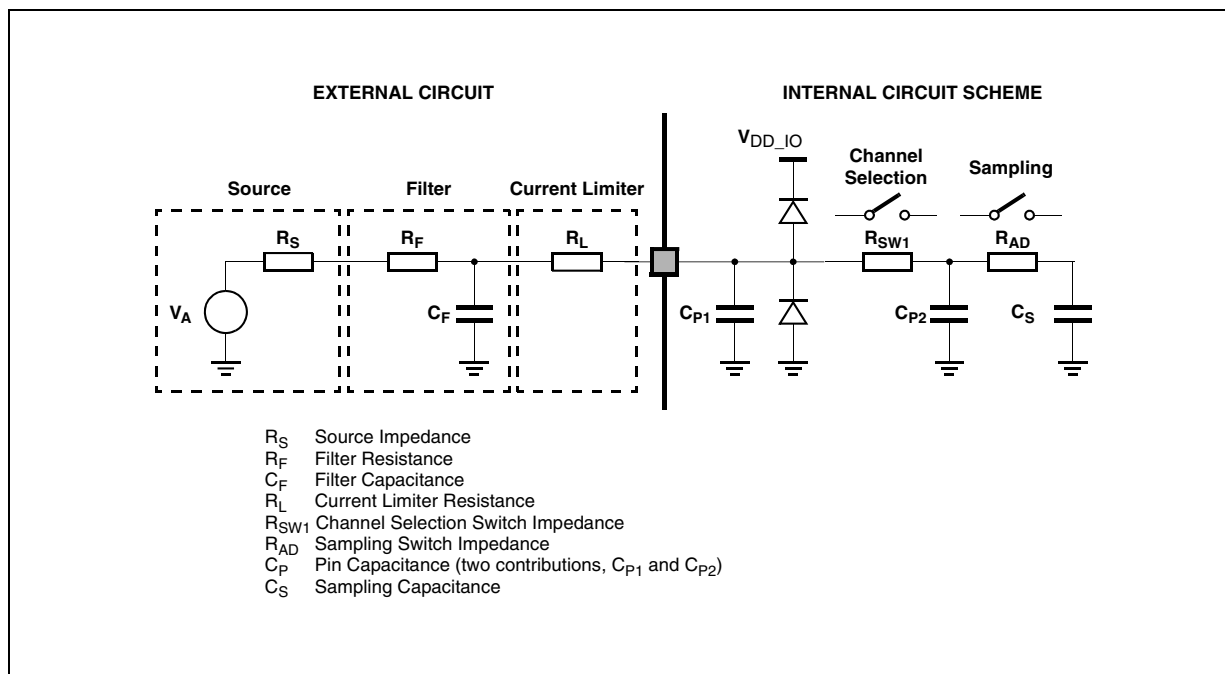


Figure 6. Input equivalent circuit

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

Table 20. ADC conversion characteristics (for 12-bit)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK ² frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1.00	MHz
t_{sample}	Sample time ³	80 MHz @ 100 ohm source impedance	250	—	—	ns
t_{conv}	Conversion time ⁴	80 MHz	700	—	—	ns
t_{total_conv}	Total Conversion time $t_{sample} + t_{conv}$ (for standard and extended channels)	80 MHz	1.5 ⁵	—	—	μs
	Total Conversion time $t_{sample} + t_{conv}$ (for precision channels)		1	—	—	
$C_S^{6, 6}$	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}^6	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}^6	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}^6	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	k Ω
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω

Table continues on the next page...

Table 21. ADC conversion characteristics (for 10-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
t_{conv}	Conversion time ⁴	80 MHz	550	—	—	ns
t_{total_conv}	Total Conversion time $t_{sample} + t_{conv}$ (for standard channels)	80 MHz	1	—	—	μ s
	Total Conversion time $t_{sample} + t_{conv}$ (for extended channels)		1.5	—	—	
C_S ⁵	ADC input sampling capacitance	—	—	3	5	pF
C_{P1} ⁵	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2} ⁵	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1} ⁵	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	k Ω
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD} ⁵	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max positive/negative injection		–5	—	5	mA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
$TUE_{standard/extended}$ channels	Total unadjusted error for standard channels	Without current injection	–4	+/-3	4	LSB
		With current injection ⁶		+/-4		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	μ s

1. Active ADC Input, $V_{inA} < [\min(ADC_ADV, IO_Supply_A,B,C)]$. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO_supply_A , B, C and ADC_Supply .
2. The internally generated clock (known as AD_clk or $ADCK$) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See [Figure 65](#)
6. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (V_{INA} , see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

6.2.4 128 KHz Internal RC oscillator Electrical specifications**Table 26. 128 KHz Internal RC oscillator electrical specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{oscu}^1	Oscillator frequency	Calibrated	119	128	136.5	KHz
	Temperature dependence				600	ppm/C
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	μA
		Clock stopped			200	nA

1. $V_{\text{dd}}=1.2\text{ V}$, 1.32V , $T_{\text{a}}=-40\text{ C}$, 125 C

6.2.5 PLL electrical specifications**Table 27. PLL electrical specifications**

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 28	ps	NON SSCG mode
TIE			See Table 28		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	μs	Calibration mode

Table 28. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN}^1	Jitter due to Fractional Mode (ps) J_{SDM}^2	Jitter due to Fractional Mode J_{SSCG}^3 (ps)	1 Sigma Random Jitter J_{RJ}^4 (ps)	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	$\pm(J_{\text{SN}}+J_{\text{SDM}}+J_{\text{SSCG}}+N^{[4]} \times J_{\text{RJ}})$

Table continues on the next page...

Table 30. Flash memory program and erase specifications

Symbol	Characteristic ¹	Typ ²	Factory Programming ^{3, 4}		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life ⁵	Lifetime Max ⁶		
						20°C ≤T _A ≤30°C	-40°C ≤T _J ≤150°C	
t _{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		μs
t _{ppgm}	Page (256 bits) program time	73	200	300	108	500		μs
t _{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		μs
t _{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t _{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t _{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t _{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t _{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t _{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
t _{256kers}	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
t _{256kpgm}	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programming times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max ^{1, 1}	Units ^{2, 2}
t _{ai16kseq}	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x T _{period} x N _{read}	—
t _{ai32kseq}	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x T _{period} x N _{read}	—
t _{ai64kseq}	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x T _{period} x N _{read}	—

Table continues on the next page...

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	μ s
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	μ s

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 34. Flash Read Wait State and Address Pipeline Control Combinations

Flash frequency	RWSC setting	APC setting
0 MHz < fFlash <= 33 MHz	0	0
33 MHz < fFlash <= 100 MHz	2	1
100 MHz < fFlash <= 133 MHz	3	1
133 MHz < fFlash <= 160 MHz	4	1

Table 35. DSPI electrical specifications (continued)

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	NA	—	-2	—	ns
			Slave	4	—	6	—	
			Master (MTFE = 1, CPHA = 0)	-2	—	10 ¹	—	
			Master (MTFE = 1, CPHA = 1)	-2	—	-2	—	

1. SMPL_PTR should be set to 1

NOTE

Restriction For High Speed modes

- DSPI2, DSPI3, SPI1 and SPI2 will support 40MHz Master mode SCK
- DSPI2, DSPI3, SPI1 and SPI2 will support 25MHz Slave SCK frequency
- Only one {SIN,SOUT and SCK} group per DSPI/SPI will support high frequency mode
- For Master mode MTFE will be 1 for high speed mode
- For high speed slaves, their master have to be in MTFE=1 mode or should be able to support 15ns tSUO delay

NOTE

For numbers shown in the following figures, see [Table 35](#)

Table 36. Continuous SCK timing

Spec	Characteristics	Pad Drive/Load	Value	
			Min	Max
tSCK	SCK cycle timing	strong/50 pF	100 ns	-
-	PCS valid after SCK	strong/50 pF	-	15 ns
-	PCS valid after SCK	strong/50 pF	-4 ns	-

Table 37. DSPI high speed mode I/Os

DSPI	High speed SCK	High speed SIN	High speed SOUT
DSPI2	GPIO[78]	GPIO[76]	GPIO[77]
DSPI3	GPIO[100]	GPIO[101]	GPIO[98]
SPI1	GPIO[173]	GPIO[175]	GPIO[176]
SPI2	GPIO[79]	GPIO[110]	GPIO[111]

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = -40 oC / 150 oC.

6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 41. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

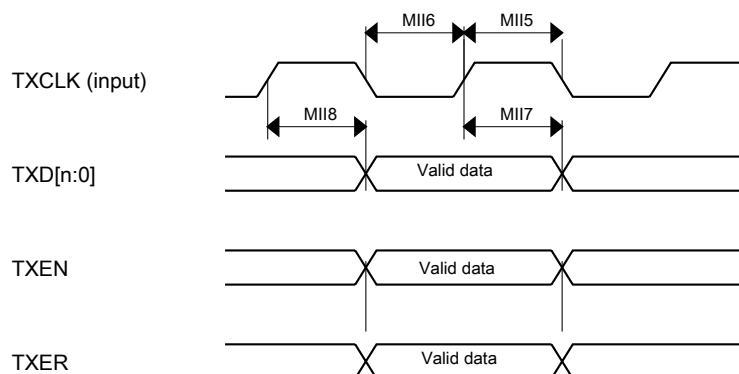


Figure 21. RMII/MII transmit signal timing diagram

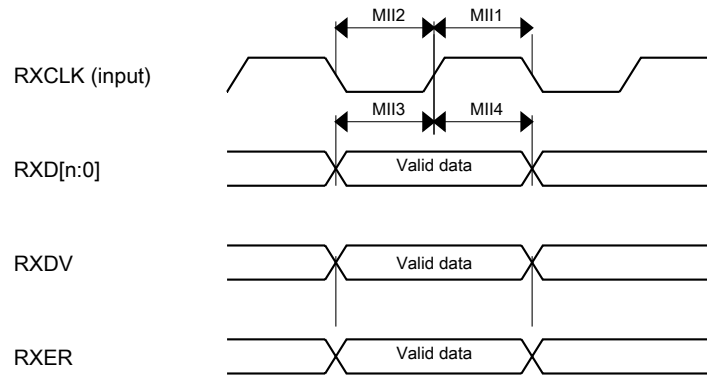


Figure 22. RMII/MII receive signal timing diagram

6.4.3.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 42. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

6.4.4 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

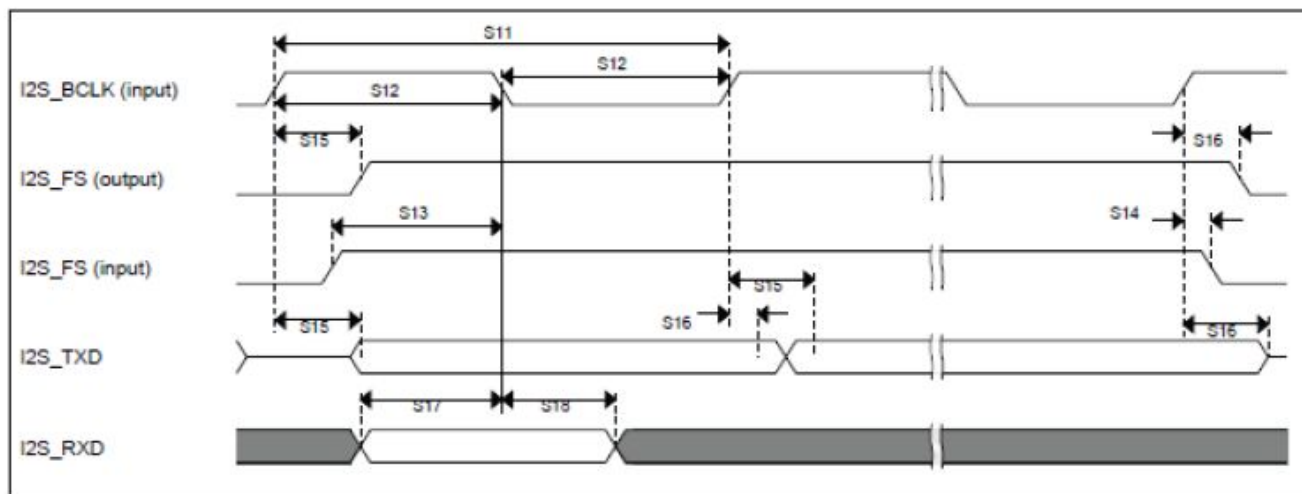
Table 43. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns

Table continues on the next page...

Table 44. Slave mode SAI Timing (continued)

No	Parameter	Value		Unit
		Min	Max	
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

**Figure 24. Slave mode SAI Timing**

6.5 Debug specifications

6.5.1 JTAG interface timing

Table 45. JTAG pin AC electrical characteristics ¹

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time ^{2, 2}	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20 ^{3, 3}	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600 ^{4, 4}	ns

Table continues on the next page...

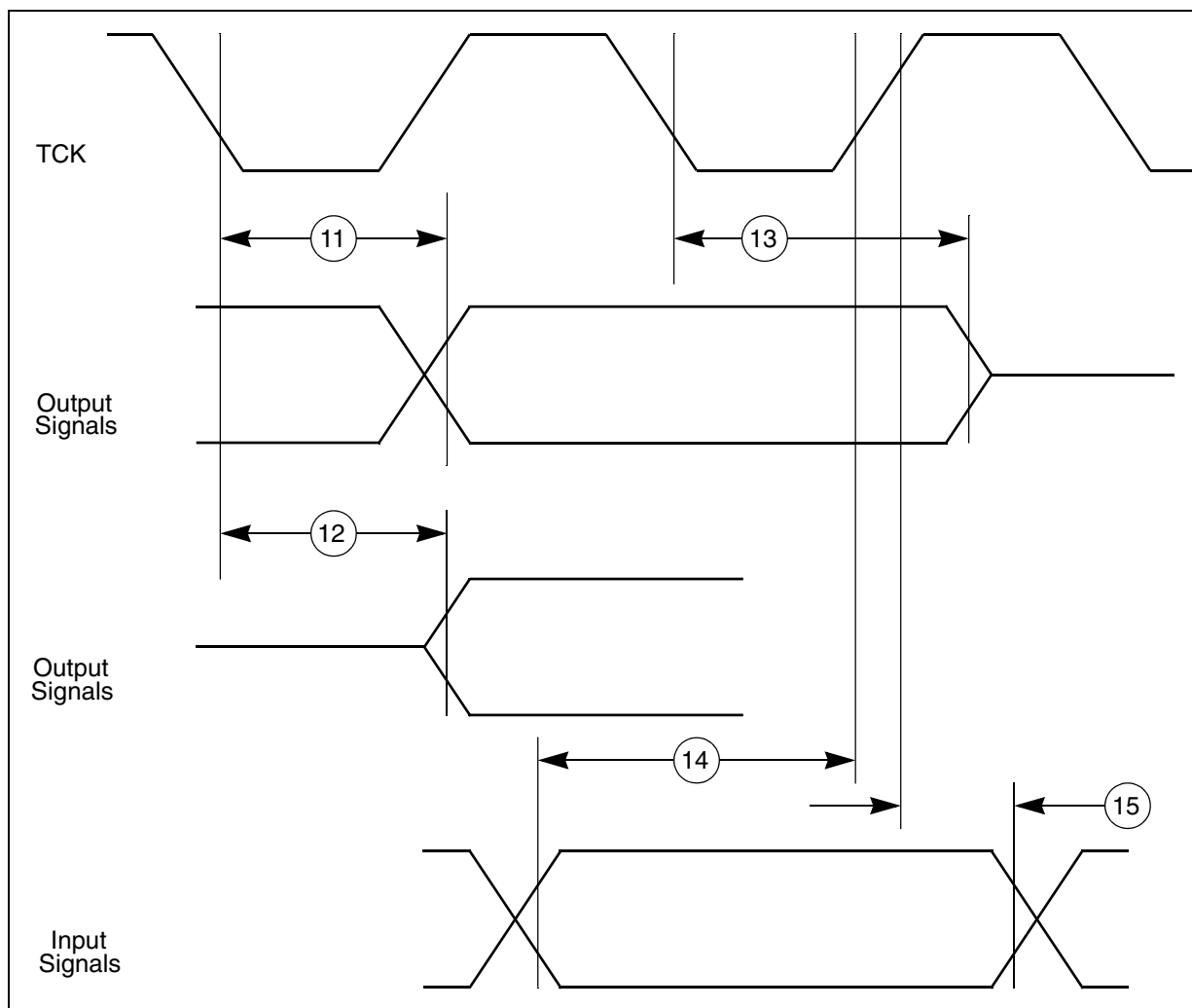


Figure 27. JTAG boundary scan timing

6.5.2 Nexus timing

Table 46. Nexus debug port timing ¹

No.	Symbol	Parameter	Condition s	Min	Max	Unit
1	t_{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	MCKO Low to MDO, MSEO, EVTO Data Valid ²	—	-0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	EVTI Pulse Width	—	4	—	t_{TCYC}
5	t_{EVTOPW}	EVTO Pulse Width	—	1	—	t_{MCYC}
6	t_{TCYC}	TCK Cycle Time ³	—	62.5	—	ns
7	t_{TDC}	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS} , t_{NTMSS}	TDI, TMS Data Setup Time	—	8	—	ns

Table continues on the next page...

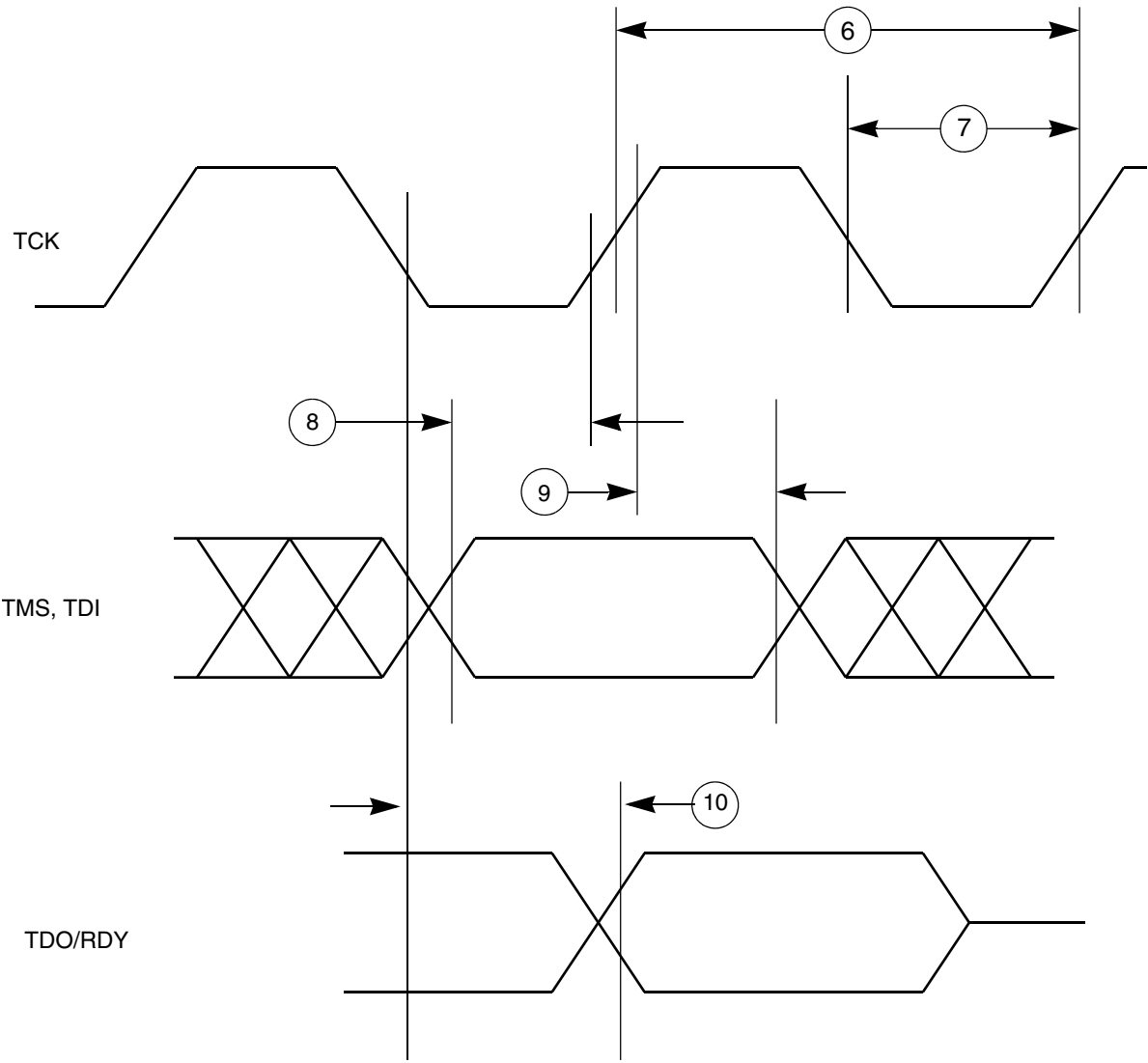


Figure 30. Nexus TDI, TMS, TDO timing

6.5.3 WKPU/NMI timing

Table 47. WKPU/NMI glitch filter

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
2	$W_{NFNMI}D$	NMI pulse width that is passed	400	—	—	ns

Reset sequence

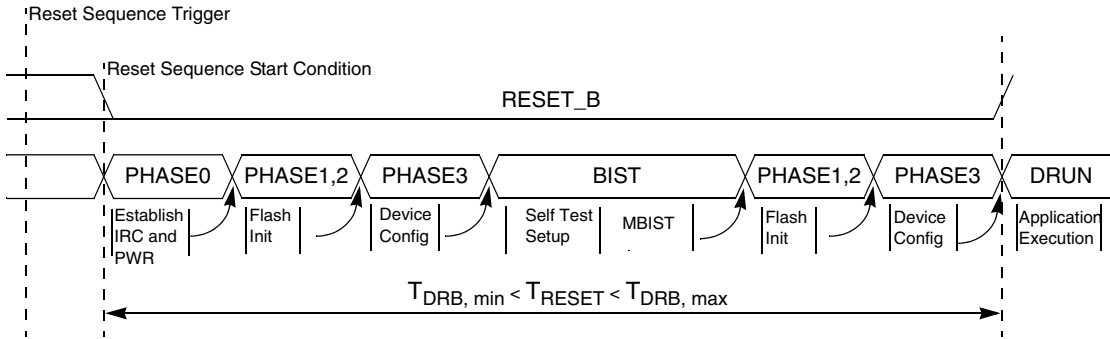


Figure 32. Destructive reset sequence, BIST enabled

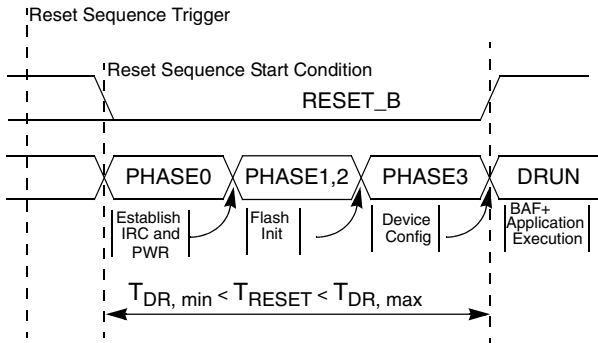


Figure 33. Destructive reset sequence, BIST disabled

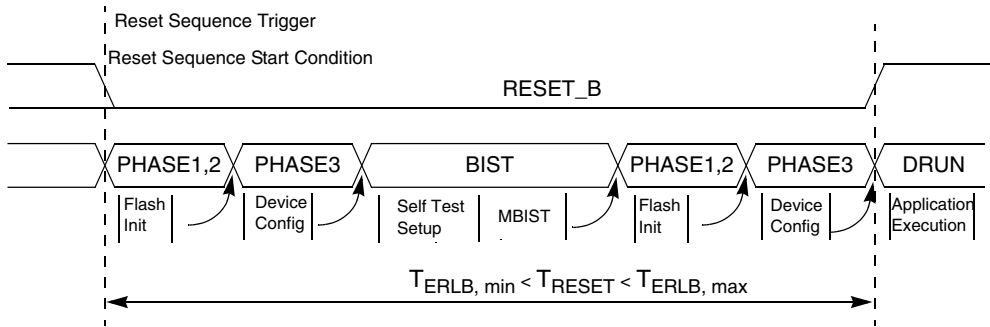


Figure 34. External reset sequence long, BIST enabled

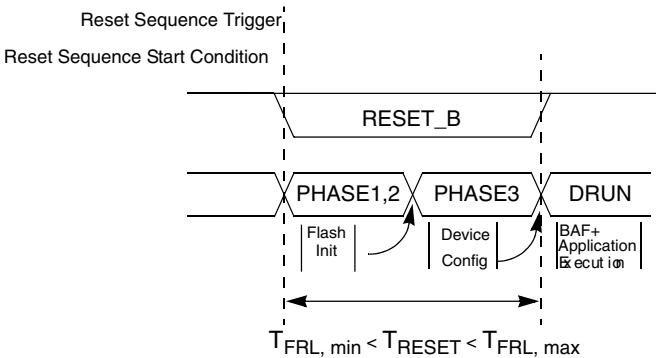


Figure 35. Functional reset sequence long

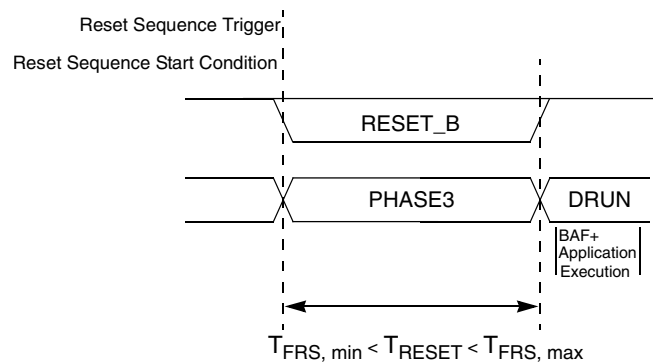


Figure 36. Functional reset sequence short

The reset sequences shown in [Figure 35](#) and [Figure 36](#) are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

11.1 Revision History

The following table provides a revision history for this document.

Table 51. Revision History

Rev. No.	Date	Substantial Changes
Rev 1	14 March 2013	Initial Release

Table continues on the next page...