



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5747cfk0amku6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table of Contents

1	Block	diagram	4
2	Fami	ly compa	rison4
3	Orde	ring parts	
	3.1	Determi	ning valid orderable parts8
	3.2	Ordering	g Information9
4	Gene	eral	9
	4.1	Absolute	e maximum ratings9
	4.2	Recom	nended operating conditions11
	4.3	Voltage	regulator electrical characteristics13
	4.4	Voltage	monitor electrical characteristics17
	4.5	Supply	current characteristics18
	4.6	Electros	tatic discharge (ESD) characteristics22
	4.7	Electror	nagnetic Compatibility (EMC) specifications23
5	I/O p	arameter	s23
	5.1	AC spec	cifications @ 3.3 V Range23
	5.2	DC elec	trical specifications @ 3.3V Range24
	5.3	AC spec	cifications @ 5 V Range25
	5.4	DC elec	trical specifications @ 5 V Range25
	5.5	Reset p	ad electrical characteristics26
	5.6	PORST	electrical specifications
6	Perip	heral ope	erating requirements and behaviours28
	6.1	Analog.	
		6.1.1	ADC electrical specifications
		6.1.2	Analog Comparator (CMP) electrical
			specifications
	6.2	Clocks a	and PLL interfaces modules34
		6.2.1	Main oscillator electrical characteristics34
		6.2.2	32 kHz Oscillator electrical specifications36
		6.2.3	16 MHz RC Oscillator electrical
			specifications
		6.2.4	128 KHz Internal RC oscillator Electrical
			specifications
		6.2.5	PLL electrical specifications
	6.3	Memory	interfaces
		6.3.1	Flash memory program and erase
			specifications

	6.3.2	Flash memory Array Integrity and Margin
		Read specifications
	6.3.3	Flash memory module life specifications40
	6.3.4	Data retention vs program/erase cycles40
	6.3.5	Flash memory AC timing specifications41
	6.3.6	Flash read wait state and address pipeline
		control settings42
6.4	Commu	ication interfaces43
	6.4.1	DSPI timing43
	6.4.2	FlexRay electrical specifications49
		6.4.2.1 FlexRay timing49
		6.4.2.2 TxEN49
		6.4.2.3 TxD50
		6.4.2.4 RxD51
	6.4.3	Ethernet switching specifications52
	6.4.4	SAI electrical specifications53
6.5	Debug s	pecifications55
	6.5.1	JTAG interface timing55
	6.5.2	Nexus timing58
	6.5.3	WKPU/NMI timing60
	6.5.4	External interrupt timing (IRQ pin)61
Ther	mal attribu	tes61
7.1	Thermal	attributes61
Dime	nsions	
8.1	Obtainin	g package dimensions65
Pinou	uts	
9.1	Package	pinouts and signal descriptions
Rese	t sequend	e66
10.1	Reset se	quence66
	10.1.1	Reset sequence duration
	10.1.2	BAF execution duration
	10.1.3	Reset sequence description
Revis	sion Histo	у69
11.1	Revision	History

MPC5746C Microcontroller Datasheet Data Sheet, Rev. 5.1, 05/2017.

1 Block diagram



Figure 1. MPC5746C block diagram

2 Family comparison

The following table provides a summary of the different members of the MPC5746C family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40030000	0x4003FFFF	64 KB	SRAM4	not available	available	available
0x40040000	0x4004FFFF	64 KB	SRAM5	not available	not available	available
0x40050000	0x4005FFFF	64 KB	SRAM6	not available	not available	available
0x40060000	0x4006FFFF	64 KB	SRAM7	not available	not available	optional
0x40070000	0x4007FFFF	64 KB	SRAM8	not available	not available	optional

 Table 4.
 MPC5746C Family Comparison - RAM Memory Map (continued)

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5746C.

3.2 Ordering Information

Example	Code	PC 57	4	6	С	Ş	К0	М	MJ	6	R
·	Qualification Status								1	1	1
	Automotive Platform										
	Core Version										
Flas	sh Size (core dependent)										
	Product										
	Optional fields										
	Fab and mask indicator										
	Temperature spec.										
	Package Code]		
	CPU Frequency										
R = Ta	pe & Reel (blank if Tray)										
	Due due 6 Manual au		-				D -	- 1	0		
Qualification Status	Product version	Fab and i	nask v Sab	versic	on indi	icator	Pa	CKage		ED	
S = Automotive qualified	B = Single core	#(0.1 etc.)) = Ver	sion o	f the		M.	J = 170 J = 250	6 MAPB	GA	
	C = Dual core	maskset.	like rev	v. 0=0	N65H		M	N = 32	4 MAPE	GA	
PC = Power Architecture		maeneeu,					Μ	H = 10	OMAPB	GA	
Automotive Platform		Temperat	ure sp	bec.			СР	U Fre	quency		
57 = Power Architecture in 55nm	Omtion of tiolds	C = -40.C	to +85	5.C Ta			2 =	- 74 0	nerates	unto	120 MHz
	Optional fields	V = -40.C	to +10)5.C T	a		6-	74 01	nerates	unto	160 MHz
Core Version	Blank = No optional feature	M = -40.C	to +12	25.0	a		0 -		sciales	upto	100 1012
4 = e200z4 Core version (highest	S = HSM (Security Module)										
cores)	F = CAN FD										
,	B = HSM + CAN FD						Sh	ipping	Metho	d	
Flash Memory Size	R = 512K RAM						H =	= lape	and ree		
4 = 1.5 MB	T = HSM + 512K RAM						Dia		lay		
5 = 2 MB	G* = CAN FD + 512K RAM										
6 = 3 MB	H* = HSM + CAN FD + 512K RAM										
	[•] G and H for 5746 B/C only										
Note: Not all part number con	nbinations are available as produ	ction produ	ıct								
		enon prout									

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in Table 5 for specific conditions

5.3 AC specifications @ 5 V Range

Table 16. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. D	elay (ns) ¹	Rise/Fal	l Edge (ns)	Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	L>I	H/H>L				
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv		4.5/4.5		1.3/1.2	25	11
(output)		6/6		2.5/2	50	
(Output)		13/13		9/9	200	
		5.25/5.25		3/2	25	10
		9/8		5/4	50	
		22/22		18/16	200	
		27/27		13/13	50	01 ^{2, 2}
		40/40		24/24	200	
		40/40		24/24	50	00 ²
		65/65		40/40	200	
pad_i_hv/ pad_sr_hv		1.5/1.5		0.5/0.5	0.5	NA
(input)						

1. As measured from 50% of core side input to Voh/Vol of the output

2. Slew rate control modes

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Va	Unit	
		Min	Max	
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V

Table continues on the next page...

I/O parameters









Table 18.	Functional reset	pad electrical s	pecifications
-----------	------------------	------------------	---------------

Symbol	Parameter	Conditions	Value			Unit
			Min	Тур	Мах	
V _{IH}	CMOS Input Buffer High Voltage	—	0.65*V _D	_	V _{DD_HV_x}	V
			D_HV_x		+0.3	
VIL	CMOS Input Buffer Low Voltage	—	V _{DD_HV_}	—	0.35*V _{DD_HV}	V
			_x -0.3		_x	

Table continues on the next page...

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
t _{conv}	Conversion time ⁴	80 MHz	550	—	—	ns
t _{total_conv}	Total Conversion time tsample + tconv (for standard channels)	80 MHz	1			μs
	Total Conversion time tsample + tconv (for extended channels)		1.5	_		
C _S ⁵	ADC input sampling capacitance	—	_	3	5	pF
C _{P1} ⁵	ADC input pin capacitance 1	—	_	—	5	pF
C _{P2} ⁵	ADC input pin capacitance 2	—		—	0.8	pF
R _{SW1} ⁵	Internal resistance of analog	V_{REF} range = 4.5 to 5.5 V	_	—	0.3	kΩ
	source	V_{REF} range = 3.15 to 3.6 V	_	—	875	Ω
R _{AD} ⁵	Internal resistance of analog source	_	_	_	825	Ω
INL	Integral non-linearity	—	-2	—	2	LSB
DNL	Differential non-linearity	—	-1	—	1	LSB
OFS	Offset error	—	-4	—	4	LSB
GNE	Gain error	—	-4	—	4	LSB
ADC Analog Pad	Max leakage (standard channel)	150 °C		—	2500	nA
(pad going to one	Max positive/negative injection		-5	—	5	mA
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Max leakage (standard channel)	105 °C _{TA}		5	250	nA
TUE _{standard/extended}	Total unadjusted error for standard	Without current injection	-4	+/-3	4	LSB
channels	channels	With current injection ⁶		+/-4		LSB
t _{recovery}	STOP mode to Run mode recovery time				< 1	μs

 Table 21. ADC conversion characteristics (for 10-bit) (continued)

- Active ADC Input, VinA < [min(ADC_ADV, IO_Supply_A,B,C)]. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO_supply_A, B, C and ADC_Supply.
- 2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal
 resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the
 sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample
 clock t_{sample} depend on programming.
- 4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
- 5. See Figure 65
- 6. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Memory interfaces

Symbol	Characteristic	Min	Typical	Max ^{1, 1}	Units 2, 2
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	_	_	8192 x Tperiod x Nread	_
t _{mr16kseq}	Margin Read time for sequential sequence on 16 KB block.	73.81	_	110.7	μs
t _{mr32kseq}	Margin Read time for sequential sequence on 32 KB block.	128.43	_	192.6	μs
t _{mr64kseq}	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	μs
t _{mr256kseq}	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	μs

Table 31. Flash memory Array Integrity and Margin Read specifications (continued)

- Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The
 equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and
 Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires
 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the
 address pipeline set to 2, Nread would equal 4 (or 6 2).)
- 2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

6.3.3 Flash memory module life specifications Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks. ^{1, 1}	—	250,000	_	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks. ^{2, 2}	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10		Years

1. Program and erase supported across standard temperature specs.

2. Program and erase supported across standard temperature specs.

6.3.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



6.3.5 Flash memory AC timing specifications Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t _{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	_	9.4 plus four system clock periods	11.5 plus four system clock periods	μs
t _{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	_	16 plus four system clock periods	20.8 plus four system clock periods	μs
t _{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	_	100	ns
t _{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	_	5	ns
t _{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.		16 plus four system clock periods	20.8 plus four system clock periods	μs

Table continues on the next page...

6.4 Communication interfaces

6.4.1 DSPI timing

Table 35. DSPI electrical specifications

No	Symbol	Parameter	Conditions	High Speed Mode		low Spe	ed mode	Unit
				Min	Max	Min	Max	1
1	t _{SCK}	DSPI cycle	Master (MTFE = 0)	25	—	50	_	ns
		time	Slave (MTFE = 0)	40	_	60	_	1
2	t _{csc}	PCS to SCK delay	_	16	_	_	-	ns
3	t _{ASC}	After SCK delay	_	16	_	_	_	ns
4	t _{SDC}	SCK duty cycle		t _{SCK} /2 - 10	t _{SCK} /2 + 10	_	_	ns
5	t _A	Slave access time	SS active to SOUT valid	_	40	—	_	ns
6	t _{DIS}	Slave SOUT disable time	_{SS} inactive to SOUT High-Z or invalid		10	_	_	ns
7	t _{PCSC}	PCSx to PCSS time	_	13		_	_	ns
8	t _{PASC}	PCSS to PCSx time	_	13		_	_	ns
9	t _{SUI}	Data setup	Master (MTFE = 0)	NA	—	20	—	ns
		time for	Slave	2	—	2	_	
		mpate	Master (MTFE = 1, CPHA = 0)	15		8 ^{1, 1}	_	
			Master (MTFE = 1, CPHA = 1)	15		20	-	
10	t _{HI}	Data hold	Master (MTFE = 0)	NA	—	-5	—	ns
		time for	Slave	4	—	4	—	
		mpate	Master (MTFE = 1, CPHA = 0)	0		11 ¹	-	
			Master (MTFE = 1, CPHA = 1)	0		-5	_	
11	t _{SUO}	Data valid	Master (MTFE = 0)	_	NA	—	4	ns
		(after SCK	Slave	_	15	_	23	1
			Master (MTFE = 1, CPHA = 0)	_	4	_	16 ¹	
			Master (MTFE = 1, CPHA = 1)	—	4	—	4	

Table continues on the next page...



Figure 8. DSPI classic SPI timing — master, CPHA = 0



Figure 9. DSPI classic SPI timing — master, CPHA = 1

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

6.4.2.2 TxEN



Figure 17. TxEN signal

Name	Description	Min	Max	Unit
dCCTxEN _{RISE25}	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN _{FALL25}	Fall time of TxEN signal at CC	_	9	ns
dCCTxEN ₀₁	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	_	25	ns
dCCTxEN ₁₀	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	_	25	ns

1. All parameters specified for $V_{DD_HV_IOx}$ = 3.3 V -5%, +±10%, TJ = -40 °C / 150 °C, TxEN pin load maximum 25 pF





6.4.2.3 TxD



Figure 19. TxD Signal

Table 39.	TxD outpu	it characteristics
-----------	-----------	--------------------

Name	Description ¹	Min	Max	Unit
dCCT _{xAsym}	Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns)	-2.45	2.45	ns
dCCTxD _{RISE25} +dCCTx D _{FALL25}	Sum of Rise and Fall time of TxD signal at the output		9 ²	ns

Table continues on the next page...

Name	Description ¹	Min	Max	Unit
dCCTxD ₀₁	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxD ₁₀	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	_	25	ns

Table 39. TxD output characteristics (continued)

1. All parameters specified for $V_{DD_HV_IOx}$ = 3.3 V -5%, +±10%, TJ = -40 °C / 150 °C, TxD pin load maximum 25 pF.

2. For $3.3 \text{ V} \pm 10\%$ operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 20. TxD Signal propagation delays

6.4.2.4 RxD

Table 40.	RxD	input	characteristic
-----------	-----	-------	----------------

Name	Description ¹	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
dCCRxD ₀₁	Sum of delay from actual input to the D input of the first FF, rising edge	_	10	ns
dCCRxD ₁₀	Sum of delay from actual input to the D input of the first FF, falling edge	_	10	ns

No	Parameter	Value		Unit
		Min	Max	
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

Table 44. Slave mode SAI Timing (continued)



Figure 24. Slave mode SAI Timing

6.5 Debug specifications

6.5.1 JTAG interface timing

Table 45. JTAG pin AC electrical characteristics ¹

#	Symbol	Characteristic	Min	Мах	Unit
1	t _{JCYC}	TCK Cycle Time ^{2, 2}	62.5	—	ns
2	t _{JDC}	TCK Clock Pulse Width	40	60	%
3	t _{TCKRISE}	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t _{TMSS} , t _{TDIS}	TMS, TDI Data Setup Time	5	_	ns
5	t _{TMSH} , t _{TDIH}	TMS, TDI Data Hold Time	5		ns
6	t _{TDOV}	TCK Low to TDO Data Valid	—	20 ^{3, 3}	ns
7	t _{TDOI}	TCK Low to TDO Data Invalid	0	_	ns
8	t _{TDOHZ}	TCK Low to TDO High Impedance		15	ns
11	t _{BSDV}	TCK Falling Edge to Output Valid		600 ^{4, 4}	ns

Table continues on the next page ...

Thermal attributes

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
—	R _{θJB}	Thermal resistance, junction to board	16.8	°C/W	44
	R _{0JC}	Thermal resistance, junction to case	7.4	°C/W	55
_	Ψ _{JT}	Thermal characterization parameter, junction to package top natural convection	0.2	°C/W	66
_	Ψ _{JB}	Thermal characterization parameter, junction to package bottom natural convection	7.3	°C/W	77

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
- 3. Per JEDEC JESD51-6 with the board horizontal
- 4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
- 7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
Single-layer (1s)	R _{eJA}	Thermal resistance, junction to ambient (natural convection)	42.6	°C/W	11, 22
Four-layer (2s2p)	R _{0JA}	Thermal resistance, junction to ambient (natural convection)	26.0	°C/W	1,2,33
Single-layer (1s)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	31.0	°C/W	1,3
Four-layer (2s2p)	R _{eJMA}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	21.3	°C/W	1,3
_	R _{θJB}	Thermal resistance, junction to board	12.8	°C/W	44

Table continues on the next page...

10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

BAF execution duration	Min	Тур	Мах	Unit
BAF execution time (boot header at first location)	_	200	_	μs
BAF execution time (boot header at last location)	_	_	320	μs

Table 50. BAF execution duration

10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

Reset sequence















Figure 35. Functional reset sequence long



Figure 36. Functional reset sequence short

The reset sequences shown in Figure 35 and Figure 36 are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

11.1 Revision History

The following table provides a revision history for this document.

Rev. No.	Date	Substantial Changes
Rev 1	14 March 2013	Initial Release

Table continues on the next page...

How to Reach Us:

Home Page: www.nxp.com

Web Support: www.nxp.com/support Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, C-5, CodeTest, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. ARM, AMBA, ARM Powered, Artisan, Cortex, Jazelle, Keil, SecurCore, Thumb, TrustZone, and µVision are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. ARM7, ARM9, ARM11, big.LITTLE, CoreLink, CoreSight, DesignStart, Mali, mbed, NEON, POP, Sensinode, Socrates, ULINK and Versatile are trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2017 NXP B.V.





Document Number: MPC5746C Rev. 5.1, 05/2017